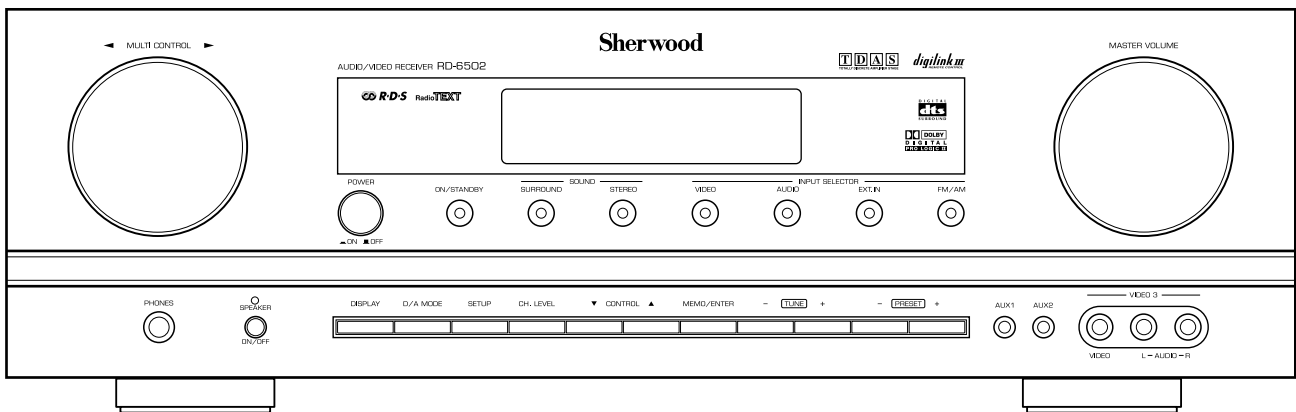


SERVICE MANUAL

RD-6502

AUDIO/VIDEO RECEIVER



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SAFETY PRECAUTIONS

WARNING

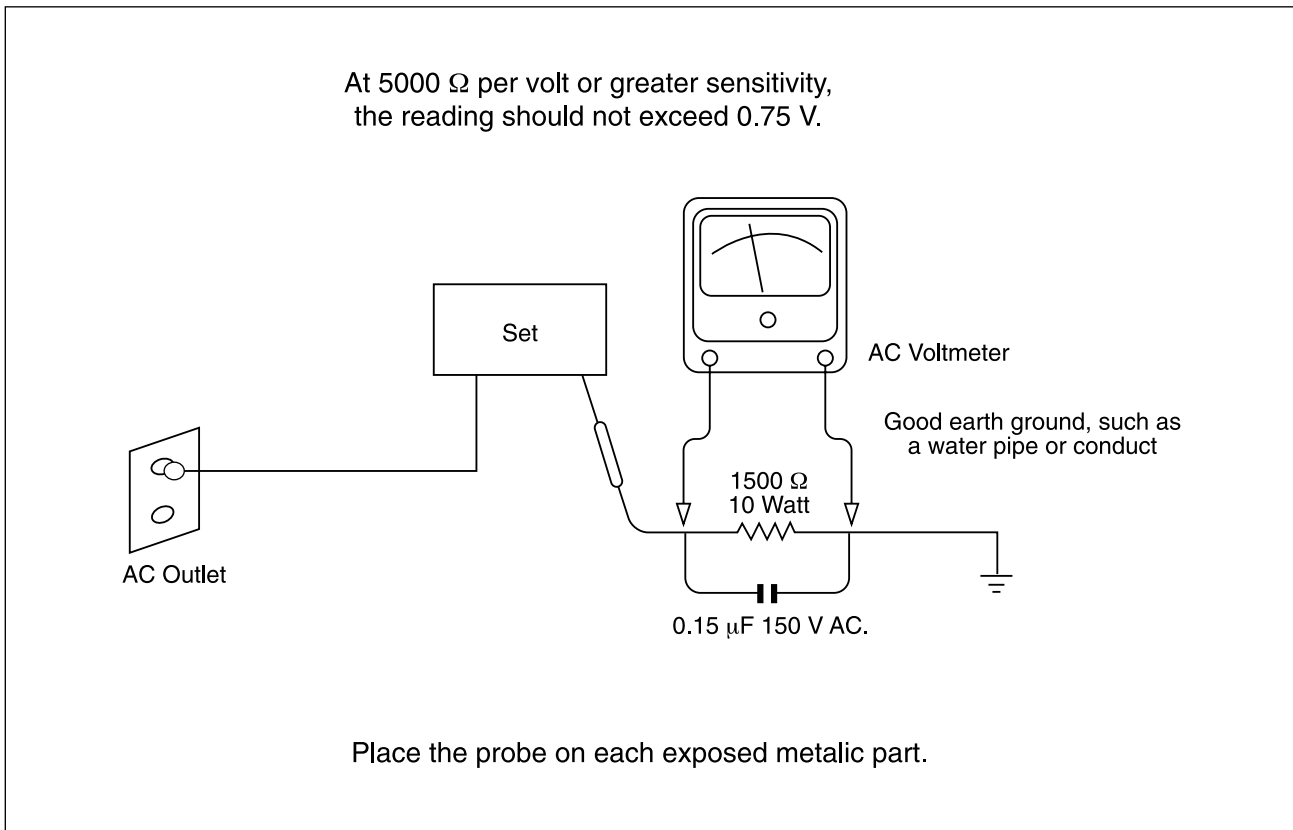
Before servicing this unit, familiarize yourself with the following precautions:

1. Many electrical and mechanical parts in this chassis have special safety characteristics that often pass unnoticed and the protection afforded by them cannot necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts that have these special safety characteristics are identified in this manual and its supplements: electrical components having such features are identified by  in the schematic diagram and the parts list.

Before replacing any of these components, read the parts list in this manual carefully. The use of substitute replacement parts that do not have the same safety characteristics as specified in the parts list may create shock, fire, or other hazards.

2. Before returning the set to the customer, always do an AC leakage current check on the

exposed metal parts of the cabinet, such as terminals, screw heads, and metal overlays, to be sure the set is safe to operate danger of electrical shock. Plug the AC line cord directly into a 120 V AC outlet(USA Version) or 230 V AC outlet(EU Version). (Do not use a line isolation transformer during this check.) Be sure your AC voltmeter has a sensitivity of 5000Ω per volt or greater. Then connect a 1500Ω 10 watt resistor, paralleled by a $0.15 \mu\text{F}$ 150 V AC capacitor, between a known good earth ground(such as a water pipe, or conduit) and the exposed metallic parts, one at a time. Measure the AC voltage across the combination of a 1500Ω resistor and a $0.15 \mu\text{F}$ capacitor. Reverse the AC plug at the AC outlet and repeat AC voltage measurements for each exposed metallic part. Voltage measured must not exceed 0.75 V RMS. This corresponds to 0.2 mA AC. Any value exceeding this limit constitutes a potential shock hazard and must be corrected immediately.



SPECIFICATIONS

Measuring methods are based on IHF and IEC standard 268-3

Measurements conditions, unless otherwise noted :

Output resistive load = (6) ohms / Both channel driven

Tone Direct ON , Other SW's : OFF

Nominal input level : 5mV for MM, 0.5mV for MC, 500mV for general purpose inputs

Power figures should be kept minimum 10min. between 15 and 35°C

Terminator : 100ohm for MC, 1kohm for MM and general purpose inputs

Filter : IHF-A filter

R/O = Rated Output

Power supply : 120V/60Hz (A), 230V/50Hz (D/E/RDS), 220V/50Hz (C), 220V/60Hz (K)

👉 FRONT AMP SECTION

* SUB-WOOFER SPKR : NO * SPKR LEVEL : ALL 0dB

* SPK SIZE : LLLN * EXT. IN * TONE OFF

No.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT L/R	NOMINAL L/R
1	INPUT SENSITIVITY	EXT. IN	1kHz	R/O	mV	280±30	280±50
2	TOTAL HARMONIC DISTORTION (STEREO IN)	EXT. IN	40Hz	R/O-3dB	%	≤0.08	≤0.12
			1kHz	"	%	≤0.08	≤0.12
			20KHz	"	%	≤0.12	≤0.2
3	CONTINUOUS AVERAGE POWER at 0.2% THD (STEREO IN)	EXT. IN	40Hz	(6)ohms	W	95	90
			1kHz	"	W	100	95
			20KHz	"	W	95	90
4	S/N RATIO, INPUT SHORT IHF-A FILTER	EXT. IN	1kHz	R/O	dB	≥90	≥85
5	FREQUENCY RESPONSE(-3dB)	EXT. IN		1W / 1kHz Ref.	Hz-kHz	10-55	10-50

👉 CENTER AMP SECTION

* SUB-WOOFER SPKR : NO * SPKR LEVEL : ALL 0dB

* SPK SIZE : LLLN * EXT. IN * TONE OFF

No.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT L/R	NOMINAL L/R
1	INPUT SENSITIVITY	EXT. IN	1kHz	R/O	mV	280±30	280±50
2	TOTAL HARMONIC DISTORTION	EXT. IN	40Hz	R/O-3dB	%	≤0.08	≤0.12
			1kHz	"	%	≤0.08	≤0.12
			20KHz	"	%	≤0.12	≤0.2
3	CONTINUOUS AVERAGE POWER at 0.2% THD	EXT. IN	40Hz	(6)ohms	W	95	90
			1kHz	"	W	100	95
			20KHz	"	W	95	90
4	S/N RATIO, INPUT SHORT IHF-A FILTER	EXT. IN	1kHz	R/O	dB	≥90	≥85
5	FREQUENCY RESPONSE(-3dB)	EXT. IN		1W / 1kHz Ref.	Hz-kHz	10-55	10-50

👉 SURROUND AMP SECTION

* SUB-WOOFER SPKR : NO * SPKR LEVEL : ALL 0dB

* SPK SIZE : LLLN * EXT. IN * TONE OFF

No.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT L/R	NOMINAL L/R
1	INPUT SENSITIVITY	EXT. IN	1kHz	R/O	mV	280±30	280±50

NO.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT L/R	NOMINAL L/R
2	TOTAL HARMONIC DISTORTION (STEREO IN)	EXT. IN	40Hz	R/O-3dB	%	≤0.08	≤0.12
			1kHz	"	%	≤0.08	≤0.12
			20KHz	"	%	≤0.12	≤0.2
3	CONTINUOUS AVERAGE POWER at 0.2% THD (STEREO IN)	EXT. IN	40Hz	(6)ohms	W	95	90
			1kHz	"	W	100	95
			20KHz	"	W	95	90
4	S/N RATIO, INPUT SHORT IHF-A FILTER	EXT. IN	1kHz	R/O	dB	≥90	≥85
5	FREQUENCY RESPONSE(-3dB)	EXT. IN		1W / 1kHz Ref.	Hz-kHz	10~55	10~50

 **STEREO SECTION**

* SUB-WOOFER SPKR : NO * STEREO MODE

* SOURCE DIRECT ON (TONE DIRECT) * CD FUNCTION

NO.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT L/R	NOMINAL L/R
1	INPUT SENSITIVITY	CD	1kHz		mV	280±30	280±50
2	CHANNEL BALANCE	CD	1kHz	R/O TO -40dB	dB	±2	±3
3	RESIDUAL NOISE	CD		VOL 1.	mV	≤3.0	≤5.0
4	TOTAL HARMONIC DISTORTION	CD	40Hz	R/O-3dB	%	≤0.08	≤0.12
			1kHz	"	%	≤0.08	≤0.12
			20KHz	"	%	≤0.12	≤0.2
5	CONTINUOUS AVERAGE POWER at 0.2% THD	CD	(40)Hz	(6)ohms	W	95	90
			1kHz	"	W	100	95
			(20)KHz	"	W	95	90
6	S/N RATIO, IHF-A FILTER	CD	1kHz	R/O	dB	≥90	≥85
7	CHANNEL SEPARATION	CD	100Hz	R/O-3dB	dB	≥55	≥50
			1kHz	"	dB	≥65	≥55
			10kHz	"	dB	≥50	≥45
8	FUNCTION CROSSTALK	CD→VIDEO2	1 kHz	"	dB	≥55	≥50
			10 kHz	"	dB	≥45	≥40
9	FREQUENCY RESPONSE (-3dB)	CD		1W	Hz-kHz	10~55	10~50
10	TONE CONTROL , ±(10)dB (TONE DIRECT OFF)	MAX	100Hz	1W	dB	+10(±2)	+10(±3)
		MIN	100Hz	"	dB	-10(±2)	-10(±3)
		MAX	100kHz	"		+10(±2)	+10(±3)
		MIN	100kHz	"		-10(±2)	-10(±3)
11	HEADPHONE OUTPUT H/P = 64ohms	CD	1kHz	R/O	V	3.0±0.3	3.0±0.5

 **SUBWOOFER SECTION**

* SUB-WOOFER SPKR : YES * SPKR LEVEL : ALL 0dB

* SPK SIZE : LLLN * EXT. IN * TONE OFF

No.	DESCRIPTION	INPUT	FREQ.	REMARK	UNIT	LIMIT	NOMINAL
1	PRE OUTPUT LEVEL	SUB-CH(280mV)	30Hz	VOL max	V	1.7±0.5	1.7±1.0

TUNER SECTION

Measuring methods in conformity with IEC standard 315

Measurements condition FM : Radio frequency = 98.1MHz, Audio frequency = 1kHz

Reference level = 1mV on (75ohms , 300ohms)

Deviation : MONO = $\pm 75\text{kHz}$, Stereo = $\pm 67.5\text{kHz} \pm 7.5\text{kHz}$ (A)

MONO = $\pm 40\text{kHz}$, Stereo = $\pm 40\text{kHz} \pm 7.5\text{kHz}$ (C/D/E/K/RDS)

Test Point : TP 1 = 90.1MHz, TP 2 = 98.1MHz, TP 3 = 106.1MHz

Filter = B.P.F at STEREO

Power supply : 120V/60Hz (A), 220V/50Hz (C), 230V/50Hz (D/E/RDS), 220V/60Hz (K)

👉 FM SECTION

NO.	DESCRIPTION	UNIT	LIMIT L/R	NOMINAL L/R	
1	TUNING RANGE	LOW ~ HIGH	MHz	87.5~108	
	STEP (A/K)	AUTO/Man.	kHz	100/100	
	STEP (C/D/E/RDS)	AUTO/Man.	kHz	50/50	
2	USABLE SENSITIVITY S/N = 30dB	TP 1	dBu	≤ 12	≤ 15
		TP 2	dBu	≤ 12	≤ 15
		TP 3	dBu	≤ 12	≤ 15
3	AUTO STOP LEVEL	TP 2	dBu	25 ± 6	25 ± 8
4	S/N RATIO IHF-A FILTER (A)	MONO	dB	≥ 60	≥ 50
		STEREO	dB	≥ 55	≥ 50
	S/N RATIO IHF-A FILTER (C/D/E/K/RDS)	MONO	dB	≥ 55	≥ 50
		STEREO	dB	≥ 50	≥ 45
5	TOTAL HARMONIC DISTORTION	MONO	%	≤ 0.7	≤ 1.2
		STEREO	%	≤ 1.0	≤ 1.5
6	OEVR LOAD DISTORTION(75KHz, 120dbu)	MONO	%	≤ 2.0	≤ 3.0
7	STEREO SEPARATION (MAIN 53.5%, PILOT 10%)	250Hz	dB	≥ 30	≥ 25
		1kHz	dB	≥ 30	≥ 25
		6.3kHz	dB	≥ 20	≥ 15
8	FREQUENCY RESPONSE,75us, -3dB (A)	TP2	Hz	50~10K	60~9K
	50us, -3dB (C/D/E/K/RDS)	TP2	Hz	50~8K	60~7K
9	IF REJECTION (A)	TP 1	dB	≥ 65	≥ 60
	IF REJECTION (C/D/E/K/RDS)	TP 1	dB	≥ 75	≥ 70
10	IMAGE REJECTION (A)	TP 3	dB	≥ 20	≥ 18
	IMAGE REJECTION (C/D/E/K/RDS)		dB	≥ 75	≥ 70
11	AM SUPPRESSION(AT AM 30% 1kHz)	TP 2	dB	≥ 40	≥ 35
12	OUTPUT LEVEL MONO (A)	TP 2	mV	600 ± 100	600 ± 150
	OUTPUT LEVEL MONO (C/D/E/K/RDS)		mV	200 ± 100	200 ± 150
13	RDS SENSITIVITY (RDS ONLY)	TP 2	dBu	≤ 30	≤ 35

AM SECTION

Measuring methods in conformity with IEC standard 315

Measurements condition AM - MW : Radio frequency = 1000/999kHz, Audio frequency = 400Hz

Reference level = 74dBu/m on 50ohms Modulation = 30%

Test Point : MW TP1 = (600)kHz TP2 = (1000)kHz TP3 = (1400)kHz → (A)

Test Point : MW TP1 = (603)kHz TP2 = (999)kHz TP3 = (1404)kHz → (C/D/E/K/RDS)

No.	DESCRIPTION	UNIT	LIMIT L/R	NOMINAL L/R
1	TUNING COVER RANGE (A)	LOW ~ HIGH MW	kHz	520~1710
	TUNING COVER RANGE (C/D/E/K/RDS)	LOW ~ HIGH MW	kHz	522~1611
	STEP (A)	AUTO/Man.	kHz	10
	STEP (C/D/E/K/RDS)	AUTO/Man.	kHz	9
2	USABLE SENSITIVITY S/N = 20dB	TP 1	dBu	≤ 63 ≤ 65
		TP 2	dBu	≤ 63 ≤ 65
		TP 3	dBu	≤ 63 ≤ 65
3	S/N RATIO(100dBu/m, 30% Mod)	TP 2	dB	≥ 38 ≥ 35
4	TOTAL HARMONIC DISTORTION (100dBu/m, 30% Mod)	TP2	%	≤ 2.0 ≤ 3.0
5	OVER LOAD DISTORTION	TP2	%	≤ 3.0 ≤ 5.0
	(100dBu 5mV 80% MOD)			
6	FREQUENCY RESPONSE	TP2	Hz	80~2K 100~1.8K
	(74dBu/m, 400Hz=0dB, at -6dB)			
7	SELECTIVITY ±10kHz S/N = 20dB (A)	990Hz	dB	≥ 20 ≥ 25
		1010Hz		
	SELECTIVITY ±9kHz S/N = 20dB (C/D/E/K/RDS)	990Hz	dB	≥ 20 ≥ 25
		1008Hz		
8	AGC FIGURE OF MERIT	Input=100mV, -10dB	dB	≥ 50 ≥ 40
9	IF REJECTION	TP 1	dB	≥ 40 ≥ 35
10	IMAGE REJECTION	TP 3	dB	≥ 28 ≥ 25
11	WHISTLE MODULATION INPUT = 1mV/m	2IF	%	≤ 8 ≤ 10
12	AUTO STOP LEVEL	TP 2	dBu	55(±10dB) 55(±15dB)
13	OUTPUT LEVEL (74dBu/m, 30% Mod) (A)	TP2	mV	200±100 200±50
	OUTPUT LEVEL (C/D/E/K/RDS)			

☞ DOLBY DIGITAL INPUT SECTION

- INPUT : CD COAXIAL
- SURROUND MODE : DOLBY DIGITAL
- VOLUME POSISTION : 55dB
- AT SPEAKER OUT Disc : LD VER 1.0

No.	DESCRIPTION	INPUT	FREQ.	CHAP	UNIT	SPEC	
						NOMI.	LIMIT
1	OUT PUT LEVEL Disc All CH 0dB SPK MODE:LLLY	FRONT	1KHz	38	V	9.5±1	9.5±2
		CENTER	1KHz	38	V	9.5±1	9.5±2
		SURR	1KHz	38	V	9.5±1	9.5±2
		S/W	30Hz	38	V	1.2±0.3	1.2±0.5
2	T.H.D Disc 0dB LPF(20KHz) SPK MODE:LLLY	FRONT	1KHz	38	%	≤0.3	≤0.5
		CENTER	1KHz	38	%	≤0.3	≤0.5
		SURR	1KHz	38	%	≤0.3	≤0.5
		S/W	30Hz	18	%	≤0.3	≤0.5
3	S/N LPF(20KHz) JIS-A FILTER,Disc -20dB SPK MODE:LLLY,BACK-NO	FRONT	1KHz	6	dB	≥65	≥60
		CENTER	1KHz	6	dB	≥65	≥60
		SURR	1KHz	6	dB	≥65	≥60
		S/W	30Hz	18	dB	≥65	≥60
4	DYNAMIC RANGE	FRONT	1KHz	38	dB	-11±1	-11±2
		CENTER	1KHz	38	dB	-11±1	-11±2
		SURR	1KHz	38	dB	-11±1	-11±2
		S/W	30Hz	18	dB	0±1	0±2
5	DIALOG NORMALIZATION	FRONT		43	dB	-10±0.5	-10±1
		CENTER		43	dB	-10±0.5	-10±1
		SURR		43	dB	-10±0.5	-10±1
		S/W		43	dB	-10±0.5	-10±1
6	OUT PUT CONFIG 1 SPK MODE : S,S,S,Y Ref : 1KHz 0dB	FRONT	1KHz	38(ref) 20	dB	-17±1	-17±3
		CENTER	1KHz	38(ref) 20	dB	-17±1	-17±3
		SURR	1KHz	38(ref) 20	dB	-17±1	-17±3

No.	DESCRIPTION	INPUT	FREQ.	CHAP	UNIT	SPEC	
						NOMI.	LIMIT
	Ref : 30Hz 0dB	S/W	30Hz	18(ref) 22	dB	5.5±1	5.5±2
7	OUT PUT CONFIG 2 SPK MODE : L,S,S,N	FRONT	1KHz	38(ref) 18	dB	5.5±1	5.5±2
8	DOWNMIXING TEST SPK MODE : L,S,S,Y	CENTER	1KHz	10(ref) C → NO	dB	-3±0.5	-3±1
		SURR.L	1KHz	14 LS → NO	dB	-3±0.5	-3±1
		SURR.R	1KHz	16 RS → NO	dB	-3±0.5	-3±1
		FRONT	1KHz	6(ref) ST:ON	dB	7.5±1	7.5±2

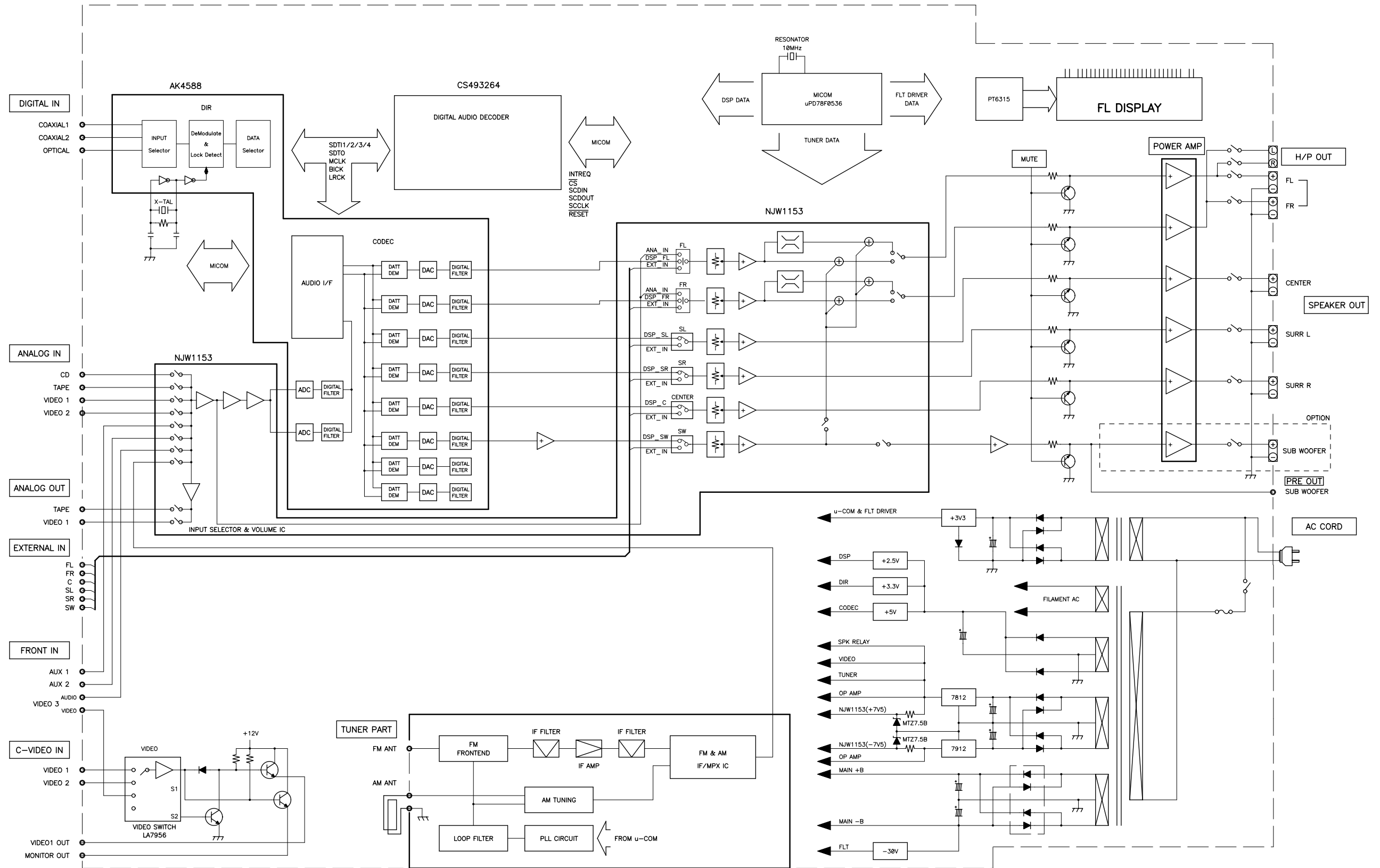
DTS INPUT SECTION

- INPUT : CD COAXIAL
- SURROUND MODE : DTS SURROUND
- VOLUME POSISTION : 55dB
- AT PRE OUT SPK MODE L,L,L,Y DTS TEST Disc(TRACK 9,10,11,12,13,14,15)

No.	DESCRIPTION	INPUT	FREQ.	TRACK	UNIT	SPEC	
						NOMI.	LIMIT
1	OUT PUT LEVEL Disc : DTS 0dB LLLY	FRONT	1KHz	10,11	V	9.5±1	9.5±2
		CENTER	1KHz	14	V	9.5±1	9.5±2
		SURR	1KHz	12,13	V	9.5±1	9.5±2
		S/W	30Hz	15	V	1.2±0.3	1.2±0.5
2	THD Disc : DTS 0dB LPF(20KHz) LLLY	FRONT	1KHz	10,11	%	≤0.3	≤0.5
		CENTER	1KHz	14	%	≤0.3	≤0.5
		SURR	1KHz	12,13	%	≤0.3	≤0.5
		S/W	30Hz	15	%	≤0.3	≤0.5
3	S/N Disc 0dB,JIS "A" LPF(20KHz) LLLY	FRONT	1KHz	10,11	dB	≥65	≥60
		CENTER	1KHz	14	dB	≥65	≥60
		SURR	1KHz	12,13	dB	≥65	≥60
		S/W	30Hz	15	dB	≥65	≥60

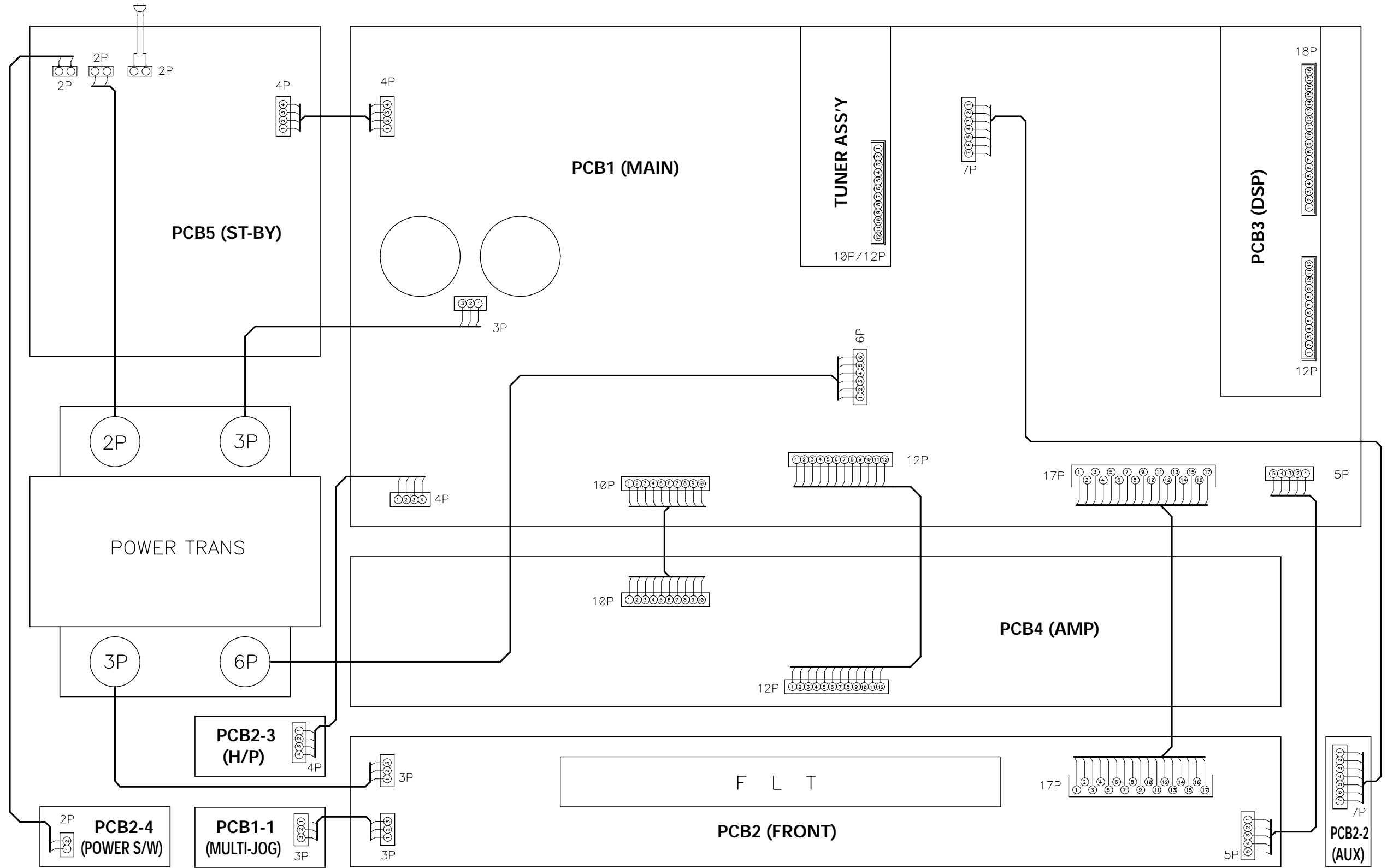
BLOCK DIAGRAM

Model No.: RD-6502



WIRING DIAGRAM

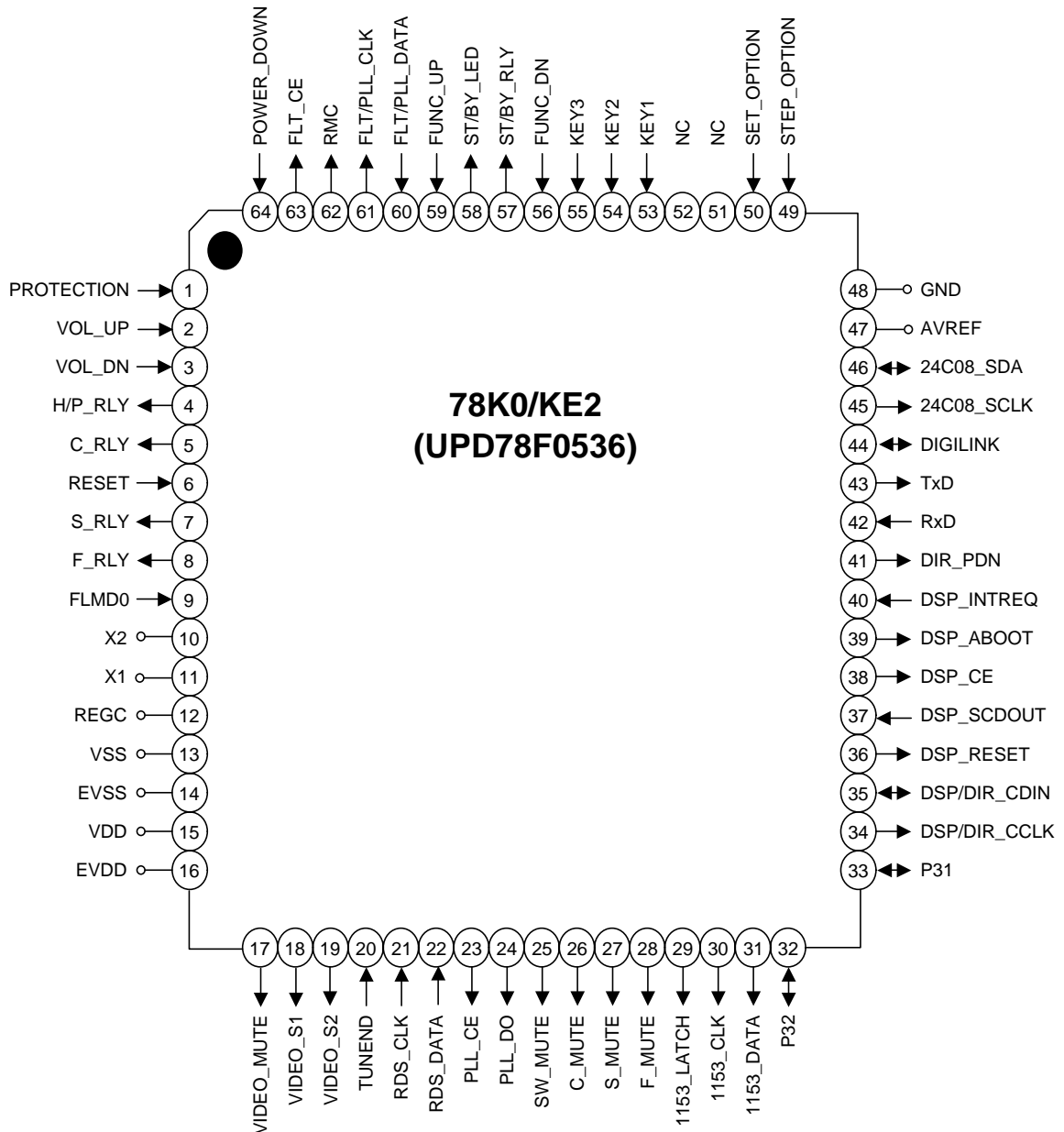
Model No.: RD-6502



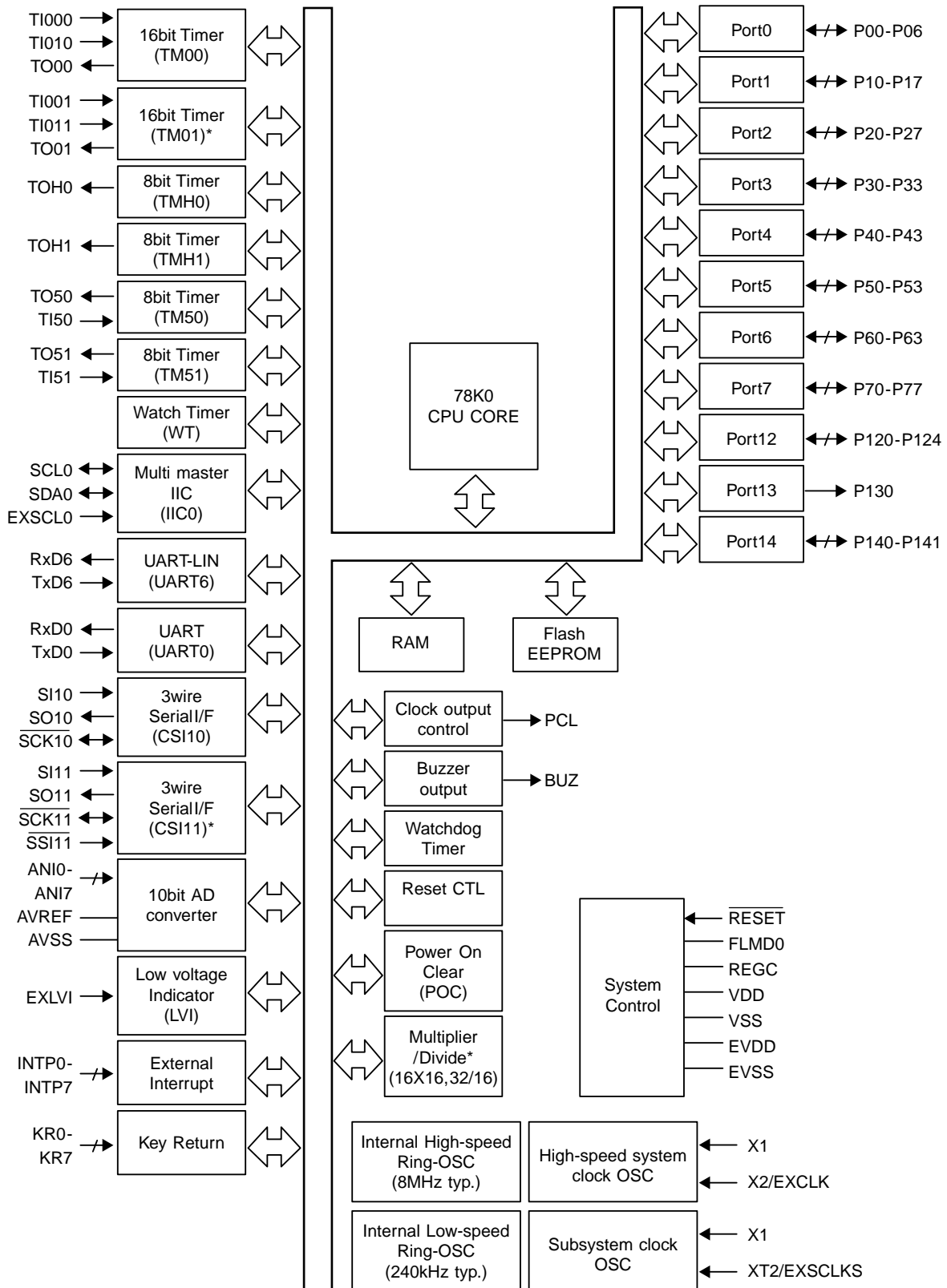
CIRCUIT DESCRIPTION

UPD78F0536 : IC101

1. Pin Description



2. Block Diagram



*:μPD78F0537/0536/0535/0534 only

3. Pin Function

No.	Pin Name	Pin Symbol	I/O	Pin Description
1	P120/INTP0/EXLVI	PROTECTION	I	Input for protection
2	P43	VOL_UP	I	Input for volume up
3	P42	VOL_DN	I	Input for volume down
4	P41	H/P_RLY	O	Output for headphone relay
5	P40	C_RLY	O	Output for center speaker relay
6	RESET	RESET	I	Input for u-com reset
7	P124/XT2/EXCLKS	S_RLY	O	Output for surround speaker relay
8	P123/XT1	F_RLY	O	Output for front speaker relay
9	IC/FLMD0	FLMD0	O	Port for flash mode setting
10	P122/X2/EXCLK	X2	O	Output for 10MHz crystal oscillator.
11	P121/X1	X1	I	Input for 10MHz crystal oscillator.
12	REGC			Connect to ground via 0.47uF/50V E.Cap
13	VSS	VSS		Ground
14	EVSS	EVSS		Ground
15	VDD	VDD		3V3
16	EVDD	EVDD		3V3
17	P60/SCLO	VIDEO_MUTE	O	Output for video mute
18	P61/SDA0	VIDEO_S1	O	Output for video function IC switching
19	P62/EXSCLO	VIDEO_S2	O	Output for video function IC switching
20	P63	TUNED	I	Input for tuner "TUNED" condition (L is active)
21	P33/TI51/TO51/INTP4	RDS_CLK	I	Clock signal input from tuner pack
22	P77/KR7	RDS_DATA	I	Input for RDS data from tuner pack
23	P76/KR6	PLL_CE	O	Chip select output for tuner pack
24	P75/KR5	PLL_DO	O	Data output for tuner pack
25	P74/KR4	SW_MUTE	O	Output for subwoofer channel mute
26	P73/KR3	C_MUTE	O	Output for center channel mute
27	P72/KR2	S_MUTE	O	Output for surround channel mute
28	P71/KR1	F_MUTE	O	Output for front channel mute
29	P70/KR0	1153_LATCH	O	Chip select output for NJW1153
30	P06/TI011/TO01	1153_CLK	O	Clock signal output for NJW1153
31	P05/TI001/SSI11	1153_DATA	O	Output for NJ W1153 control data
32	P32/INTP3	P32		Port for flash upgrade

No.	Pin Name	Pin Symbol	I/O	Pin Description
33	P31/INTP2	P31		Port for flash upgrade
34	P50	DSP/DIR_CCLK	O	Clock signal output for DIR/DSP
35	P51	DSP/DIR_CDIN	I/O	Input & output for DIR/DSP control data
36	P52	DSP_RESET	O	Output for DSP reset
37	P53	DSP_SCDOUT	I	Output for DSP control data
38	P30/INTP1	DSP_CE	O	Chip select output for NJW1153
39	P17/TI50/TO05	DSP_ABOOT	O	Output for DSP Auto boot
40	P16/TOH1/INTP5	DSP_INTREQ	I	Interrupt signal output to DSP
41	P15/TOH0	DIR_PDN	O	Output for DIR power down
42	P14/RXD6	RxD	I	Input for flash upgrade
43	P13/TXD6	TxD	O	Output for flash upgrade
44	P12/SO10	DIGILINK	I/O	Input & output for DIGILINK
45	P11/SI10/RXD0	24C08_SCLK	O	Clock signal output for 24C08
46	P10/SCK10/TXD0	24C08_SDA	I/O	Input & output for 24C08 control data
47	AVREF	AVREF		3V3
48	AVSS	AVSS		GROUND
49	P27/ANI7	STEP_OPTION	I	Input for step option
50	P26/ANI6	SET_OPTION	I	Input set option
51	P25/ANI5	NC	-	Not used
52	P24/ANI4	NC	-	Not used
53	P23/ANI3	KEY1	I	Input for KEY1 scan
54	P22/ANI2	KEY2	I	Input for KEY2 scan
55	P21/ANI1	KEY3	I	Input for KEY3 scan
56	P20/ANI0	FUNC_DN	I	Input for function encoder down
57	P130	ST/BY_LED	O	Output for standby led
58	P04/SCK11	ST/BY_RLY	O	Output for standby relay
59	P03/S111	FUNC_UP	I	Input for function encoder up
60	P02/S011	FLT/PLL_DATA	O	Output for FLT/PLL control data
61	P01/TI010/TO00	FLT/PLL_CLK	O	Clock signal output for FLT/PLL
62	P00/TI000	RMC	I	Input for remote data
63	P141/BUZ/INTP7	FLT_CE	O	Chip select output for FLT
64	P140/PCL/INTP6	POWER_DOWN	I	Input for power down

TUNER ALIGNMENT

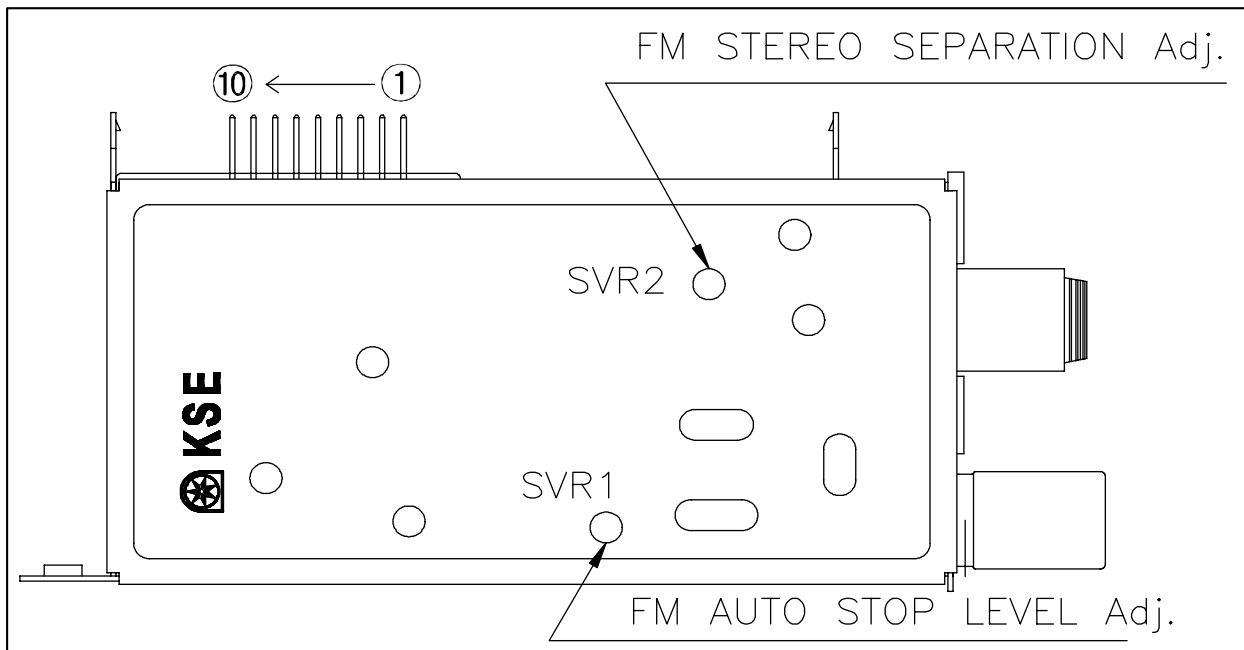
1. Electrical specification.

No.	ITEMS	SPECIFICATION	
		M W	F M
1-1	Local OSC	Above the receiving Frequency	
1-2	Frequency cover range	522 ~1620kHz	87.5 ~ 108.0MHz
1-3	Standard supply voltage	12 +/-0.5V	
1-4	FM Antenna Impedance	75 ohm unbalance	
1-5	AM Loop Antenna	9.5uH (1kHz) : S0160BL-25	

2. Electrical Characteristics.

No.	TEST ITEMS	TEST CONDITION	T.P.	T.L.	MOD.	Specification	UNIT	Adjustment
				dBu	kHz,%			
FM	AF Output Level	47kΩ Load	98.1	60	40	280±100	mV	Non Adjust
	Auto Stop Level		98.1	--		25 ±6	dBu	SVR01
	Stereo Separation	1kHz	98.1	60		25 min	dB	SVR02
MW	AF Output Level	47kΩ Load	999	74	30	180 ±60	mV	Non Adjust
	Auto Stop Level		999	--	30	55 ±15	dBu	Non Adjust

3. Adjust Point.



TROUBLESHOOTING

Symptom	Cause and Remedy	Ref No.
Power On Failure 1. FLT does not light up. 2. ST-BY LED does not light up.	A) AC-Cord check. B) Power Trans (Main/ST-BY) check. C) Fuse's disconnection check. D) Connector's disconnection or disjunction. Change or close insertion of the connector. E) Inferior ST-By switch. F) VFD Driver IC & Resonator check. 1. VFD Driver IC VCC(+3.3)V check. 2. VFD Driver clock pulse check.	F300, 301 (STBY) CN301 (STBY), CP103 (MAIN) SW700 (POWER SW) IC701 (FRONT) IC701 Pin #13 (FRONT) IC701 Pin #5 (FRONT)
Fuse Disconnection. (Power On)	A) Inferior transformer. B) AMP drive transistor out. (POWER TR) C) AMP bias transistor out. (BIAS TR) D) voltage check. 1. B+ (35 ~ 45)V, B- (- 45 ~ -35) V	Q205, Q206 (FL, FR, C, SL, SR) (AMP) Q204 (FL, FR, C, SL, SR) (AMP)
Key Disorder.	A) Key's being pushed check. B) Key signal input components inferior. C) Key data check. D) μ -COM IC or Resonator inferior. 1. μ -COM IC 3.3V check. 2. μ -COM clock pulse check.	SW700 (POWER SW) IC101 Pin #53,54,55 (MAIN) IC101 Pin #15, 16, 47 (MAIN) IC101 Pin #10, 11 (MAIN)
Power Off in 2~3 sec. after Power On.	A) Regulator IC out. 1. Signal IN/OUT check. B) Drive transistor out. (POWER TR) C) Protection circuit check. 1. Output DC check. 2. μ -COM IC protection terminal check. D) Connector's disconnection or disjunction E) SLEEP MODE cancellation.	IC103, 104 (MAIN) Q205, Q206 (FL, FR, C, SL, SR) (AMP) IC103, 104 (MAIN), IC403, 404, 405 (DSP) IC101 Pin #1 (MAIN) CP101, CP102 (MAIN)
Bump Sound (During input-select switch's change.)	A) FRONT Mute transistor's out and inferior. μ -Com front mute control PORT check. B) CENTER Mute transistor's out and inferior. μ -Com center mute control PORT check. C) SURROUND Mute transistor's out and inferior. μ -Com surround mute control PORT check. D) SUBWOOFER Mute transistor's out and inferior. μ -Com surround mute control PORT check.	Q105 (MAIN) IC101 Pin #28 (MAIN) Q107 (MAIN) IC101 Pin #26 (MAIN) Q109 (MAIN) IC101 Pin #27 (MAIN) Q114 (MAIN) IC101 Pin #25 (MAIN)
Sounds from Speaker when Headphone's connected.	A) HEADPHONE JACK connection inferior.	CP112 (MAIN)

Symptom	Cause and Remedy	Ref No.
Bass / Treble Control Failure.	<p>A) Bass volume check.</p> <ol style="list-style-type: none"> 1. Resister/Capacitor correction figure check. 2. BASS VR's property inferior. <p>B) TONE IC check.</p> <ol style="list-style-type: none"> 1. Signal IN/OUT terminal check. 2. IC voltage check. (+7.5)V, (-7.5)V 3. IC CLK/DATA/STB 	<p>IC102 (MAIN)</p> <p>IC102 Pin #1, 47, 48, 64 (MAIN)</p> <p>IC102 (MAIN)</p> <p>IC102 Pin #55, 57 (MAIN)</p> <p>IC102 Pin #29, 30, 31 (MAIN)</p>
<p>AMP Sound Dead.</p> <ol style="list-style-type: none"> 1. "LEFT" Channel dead. 2. "RIGHT" Channel dead. 3. "CENTER" Channel dead. 4. "REAR" Channel dead. 5. "REAR CENTER" Channel dead. 	<p>A) Signal Mute TR's inferior.</p> <p>B) Connector disconnection & disjunction.</p> <p>Change or close insertion of the connector.</p> <p>C) Speaker wire's disjunction.</p> <p>Close insertion of the speaker wire.</p> <p>D) Signal switching IC check.</p> <ol style="list-style-type: none"> 1. IC voltage check (+7.5)V, (-7.5)V 2. Switching IC control data check. 3. Switching IC signal IN/OUT check. 	<p>Q105, 107, 109, 111 9MAIN)</p> <p>CP110 (MAIN)</p> <p>IC102 (MAIN)</p> <p>IC102 Pin #55, 57 (MAIN)</p> <p>IC102 Pin #29, 30, 31 (MAIN)</p>
<p>AC-3/DTS Failure.</p> <p>(DSP Sound Mode)</p>	<p>A) IC Regulator check.</p> <p>IN +7.5~9V, OUT +3.3V</p> <p>IN +7.5~9V, OUT +2.5V</p> <p>IN +7.5~9V, OUT +5V</p> <p>B) DIR check.</p> <ol style="list-style-type: none"> 1. OSC check. 2. RMCK, RBCK, RLRCK, RDATA Check. 3. Micom Interface Port Check. <p>C) DSP Check.</p> <ol style="list-style-type: none"> 1. INTREQ Check. 2. LRCK Check. 3. Micom Interface Port Check. 4. SDATA Check. <p>D) D/A Check.</p> <ol style="list-style-type: none"> 1. LRCK/BCK/SDATA check. 2. Signal out check. 	<p>IC403 (DSP)</p> <p>IC404 (DSP)</p> <p>IC405 (DSP)</p> <p>IC401 (DSP)</p> <p>XTAL401 (DSP)</p> <p>IC401 Pin #10, 15, 16, 17 (DSP)</p> <p>IC401 PIN #21, 22, 31 (DSP)</p> <p>IC402 (DSP)</p> <p>IC402 Pin #20 (DSP)</p> <p>IC402 Pin #26 (DSP)</p> <p>IC402 Pin #6, 7, 18, 19, 36 (DSP)</p> <p>IC402 Pin #22 (DSP)</p> <p>IC401 (DSP)</p> <p>IC401 Pin #15, 16, 22</p> <p>IC401 Pin #39, 41, 43, 45, 47, 49, 51, 52(DSP)</p>
Video Output Dead.	<p>A) Video voltage check.</p> <ol style="list-style-type: none"> 1. DC voltage check. +12V <p>B) Video selector control IC check.</p> <ol style="list-style-type: none"> 1. DC voltage check. +12V 2. Micom control data check. 	<p>IC201 (MAIN)</p> <p>IC201 Pin #7 (MAIN)</p> <p>IC201 Pin #2, 3 (MAIN)</p>
Digi-Link Failure.	<p>A) Digi-link line disconnection check.</p> <p>Digi-Link IN/OUT circuit check.</p> <p>B) Micom Interface Port Check.</p> <ol style="list-style-type: none"> 1. μ-COM IC 3.3V check. 2. Digi-link data I/O data check. 	<p>R233, D125 (MAIN)</p> <p>IC101 Pin #44 (MAIN)</p>

Symptom	Cause and Remedy	Ref No.
Remote Controller Failure.	A) Battery check. B) RMC IC & Resonator inferior. 1. μ -COM IC 3.3V check. 2. REMOCON data check.	IC101 PIN #62 (MAIN), RMC701 (FRONT)
FM Failure.	A) FM MUTE adjustment inferior. B) FRONT-END inferior. C) FM DET COIL inferior. D) TUNER PACK check. 1. TUNER PACK +12V check. 2. PLL control data check. (Data/CE/Clock) E) TUNER B+ voltage inferior. F) μ -COM IC & Resonator inferior. 1. μ -COM IC 3.3V check. 2. Micom control data check.	PACK101 Pin #4 (MAIN) PACK101 Pin #5, 6, 7, 8, 9, 11, 12 (MAIN) IC101 (MAIN) IC101 Pin #21, 22, 23, 24, 60, 61 (MAIN)
AM Failure.	A) AM V.T voltage inferior. B) TUNER PACK check. 1. TUNER PACK +12V check. 2. PLL control data check. (Data/CE/Clock) C) TUNER B+ voltage inferior. D) AM OSC COIL inferior. E) μ -COM IC & Resonator inferior. 1. μ -COM IC 3.3V check. 2. Micom control data check.	IC101 (MAIN) IC101 Pin #21, 22, 23, 24 (MAIN)
Stereo Effect Failure. Stereo does not light up.	A) FM DET COIL Inferior. B) TUNER PACK inferior. 1. TUNER PACK +12V check. 2. PLL control data check. (Data/CE/Clock) C) STEREO adjustment inferior. D) FM MUTE adjustment inferior. E) μ -COM IC & Resonator inferior. 1. μ -COM IC 3.3V check. 2. Micom control data check.	IC101 (MAIN) IC101 Pin #21, 22, 23, 24, 60, 61 (MAIN)
Tuner Sound Dead. 1. "L / R" Channel dead. 2. "LEFT" Channel dead. 3. "RIGHT" Channel dead.	A) Connector's disconnection or disjunction. Change or Close insertion of the connector. B) AM/FM IF IC check . 1. Signal IN/OUT terminal. 2. IC driving voltage check. (+12V) C) FM DET COIL inferior. D) AM IFT COIL inferior. E) TUNER PACK check. 1. Signal IN/OUT terminal. 2. IC driving voltage check. (+12V)	

EXPLODED VIEW

Model No.: RD-6502

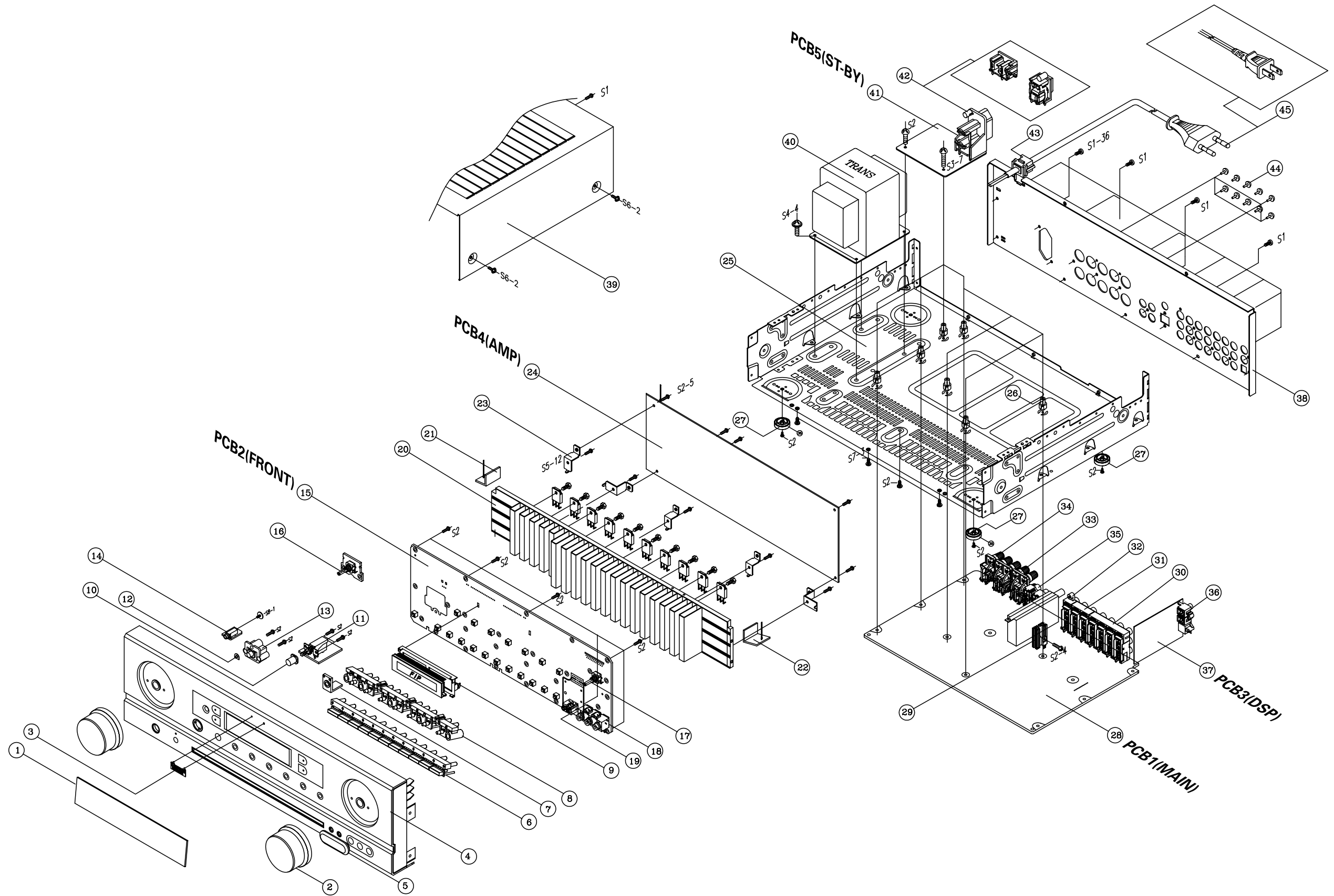


Table with 5 columns: REF No., DESCRIPTION, Q'TY, PARTS No., VER. Contains parts like BEAD COIL, INDUCTOR COIL, CONNECTORS, DIODES, TRANSISTORS, RESISTORS, MISCELLANEOUS, and ASSEMBLY P.C.BOARD MULTI JOG.

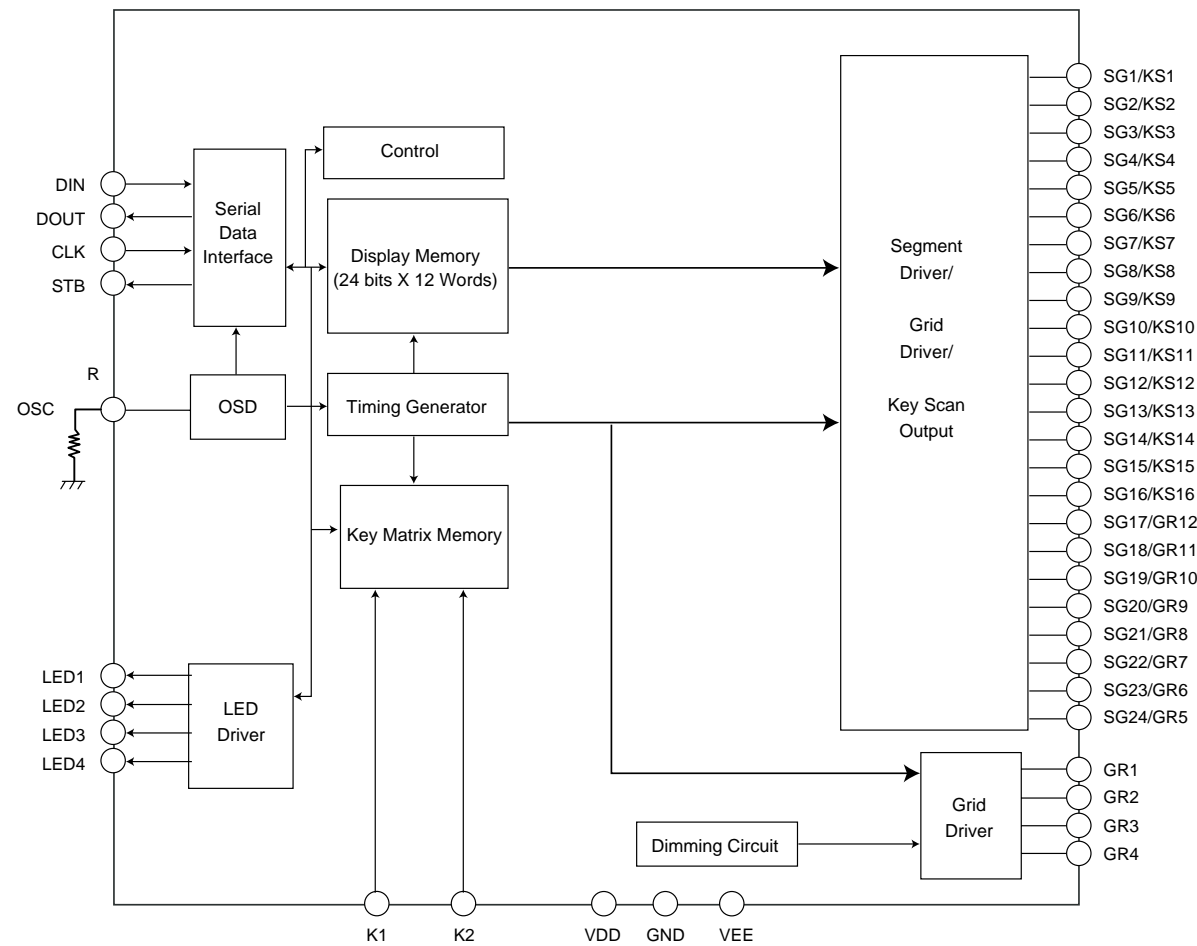
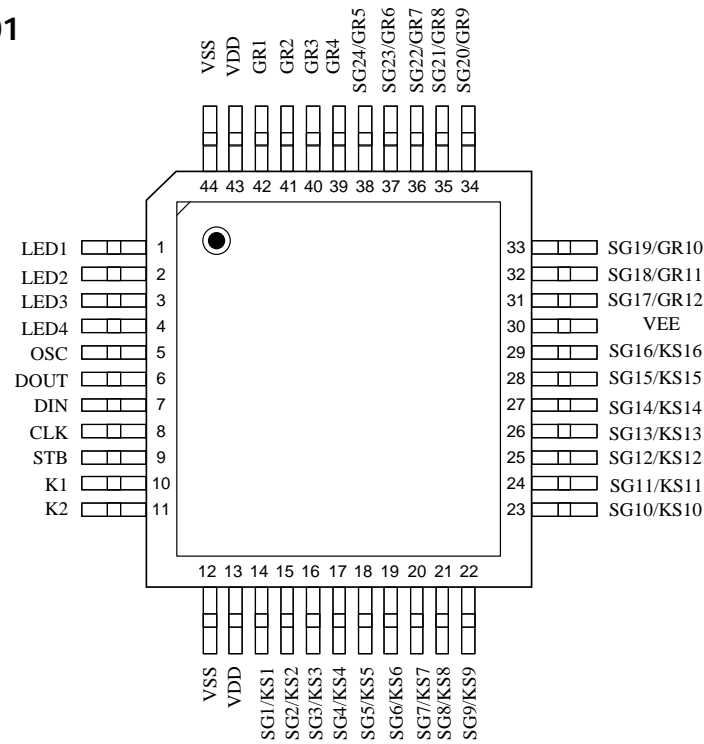
Table with 5 columns: REF No., DESCRIPTION, Q'TY, PARTS No., VER. Contains sub-assembly sections: PCB2-2 ASSEMBLY P.C.BOARD AUX, PCB2-3 ASSEMBLY P.C.BOARD HEAD PHONE, PCB2-4 ASSEMBLY P.C.BOARD POWER SW, PCB3 ASSEMBLY P.C.BOARD DSP, CAPACITORS.

Table with 5 columns: REF No., DESCRIPTION, Q'TY, PARTS No., VER. Contains parts like CERAMIC CHIP HIK, ELECT GE 85C, CERAMIC CHIP T.C, COILS, CONNECTORS, DIODES, INTEGRATED CIRCUITS, RESISTORS.

IC'S FUNCTIONAL BLOCK DIAGRAMS

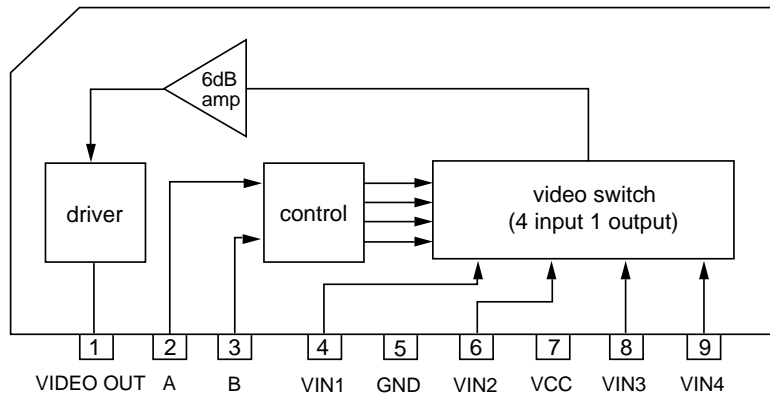
Model No.: RD-6502

PT6315 : IC701

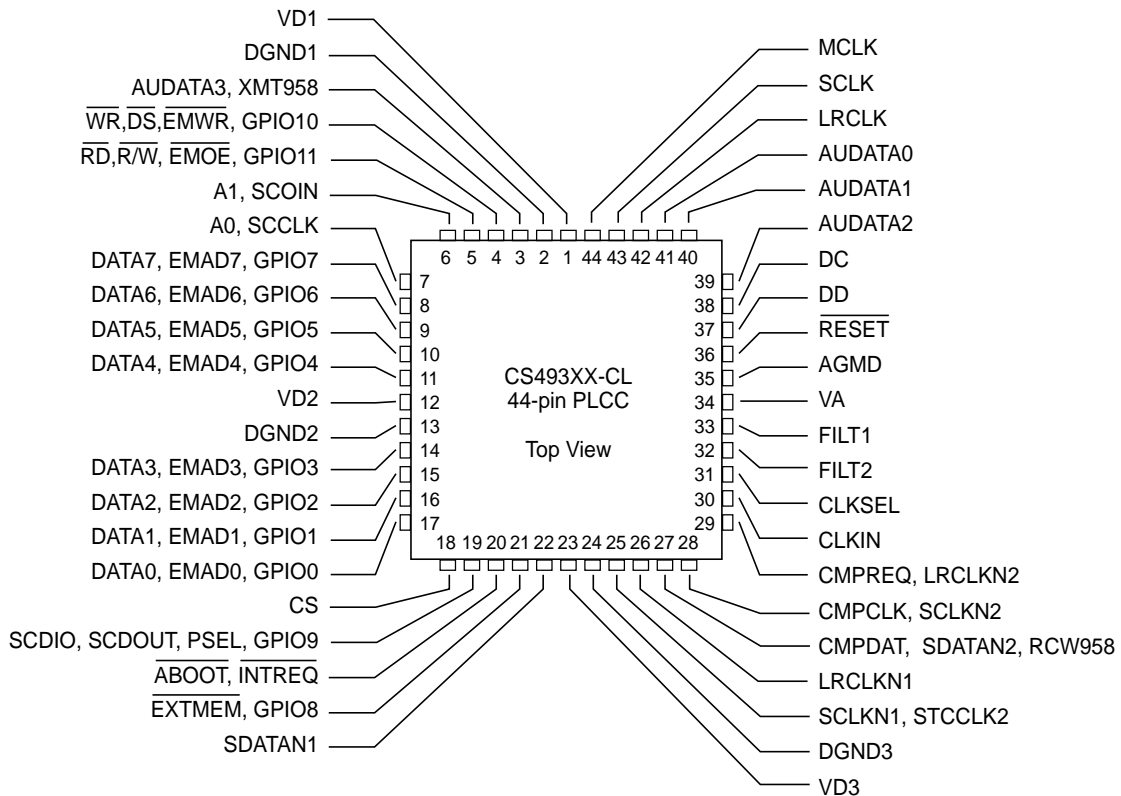


Pin Name	I/O	Description	Pin No.
LED1 to LED4	O	LED Output Pin	1 to 4
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency	5
DOUT	O	Data Output Pin (N-Channel, Open-Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	6
DIN (Schmitt Trigger)	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bit)	7
CLK (Schmitt Trigger)	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	8
STB (Schmitt Trigger)	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	9
K1 to K2	I	Key Data Input Pins The data inputted to these pins are latched at the end of the display cycle.	10, 11
VSS	-	Logic Ground Pin	12, 44
VDD	-	Logic Power Supply	13, 43
SG1/KS1 to SG16/KS16	O	High-Voltage Segment Output Pins Also acts as the Key Source	14 to 29
VEE	-	Pull-Down Level	30
SG17/GR12 to SG24/GR5	O	High Voltage Segment/Grid Output Pins	31 to 38
GR4 to GR1	O	High-Voltage Grid Output Pins	39 to 42

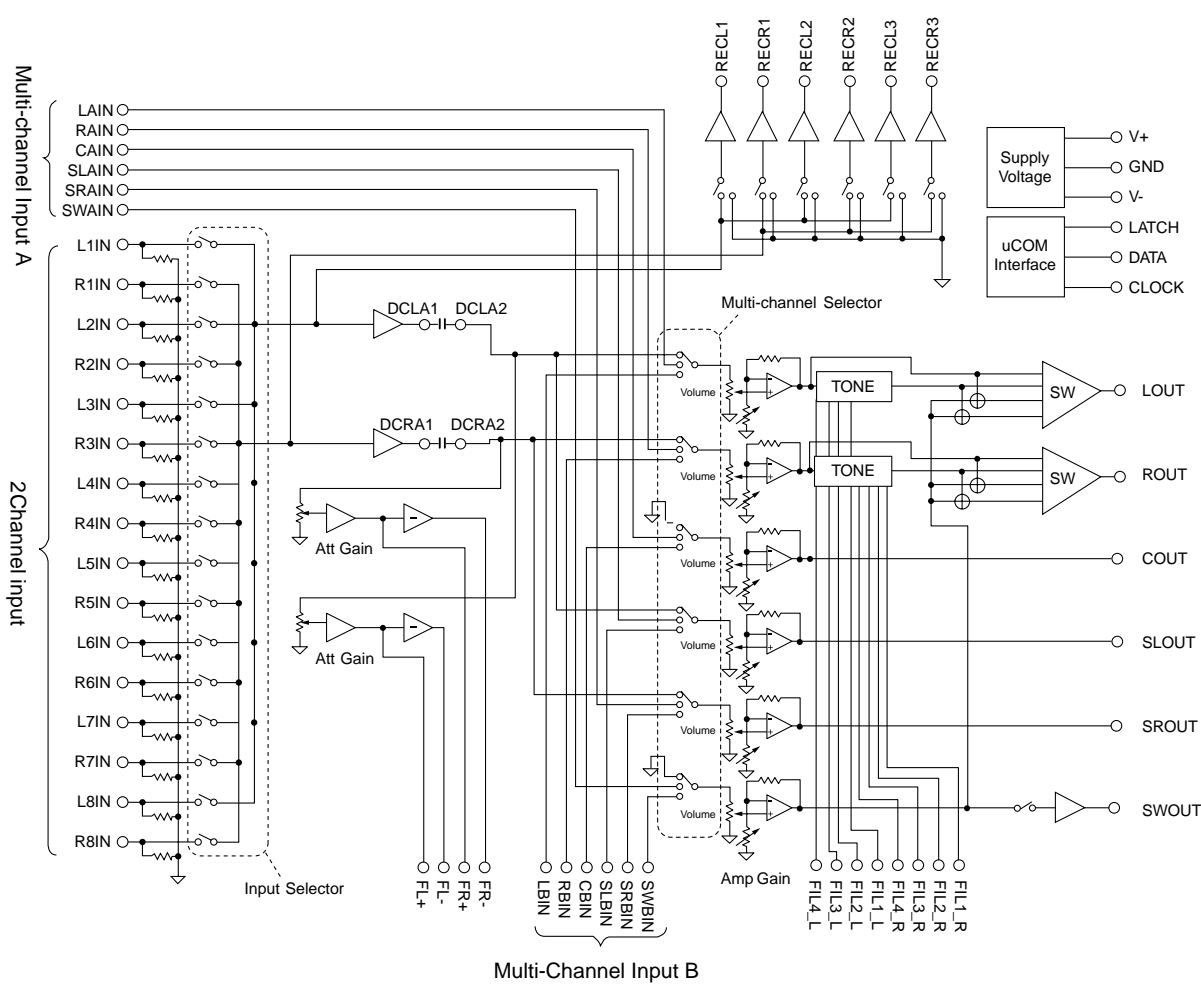
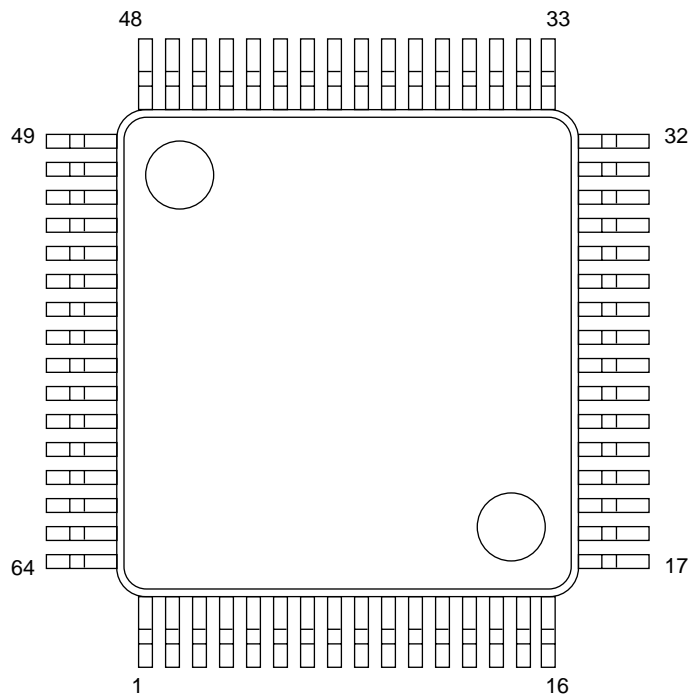
LA7956 : IC201



CS49326 : IC402

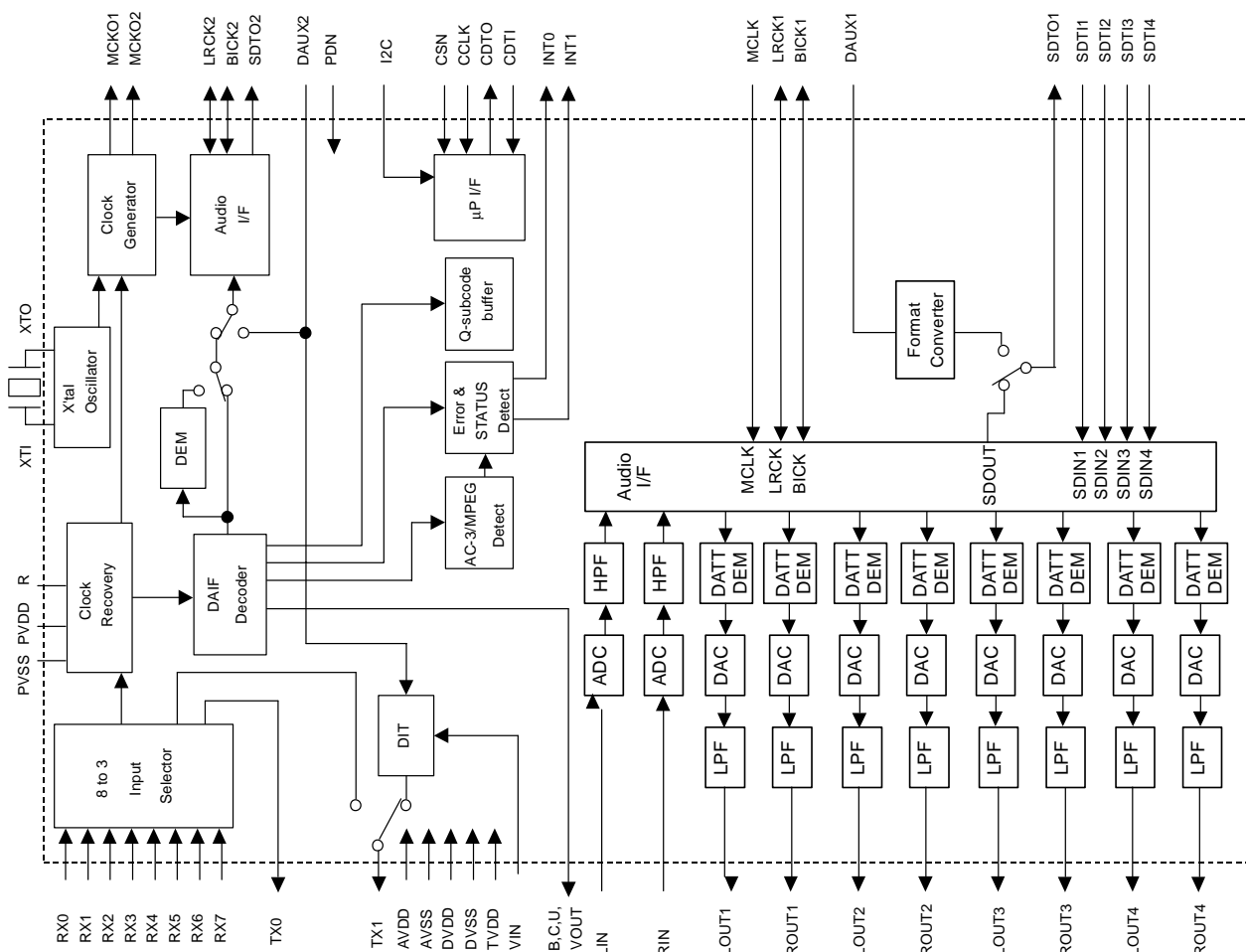
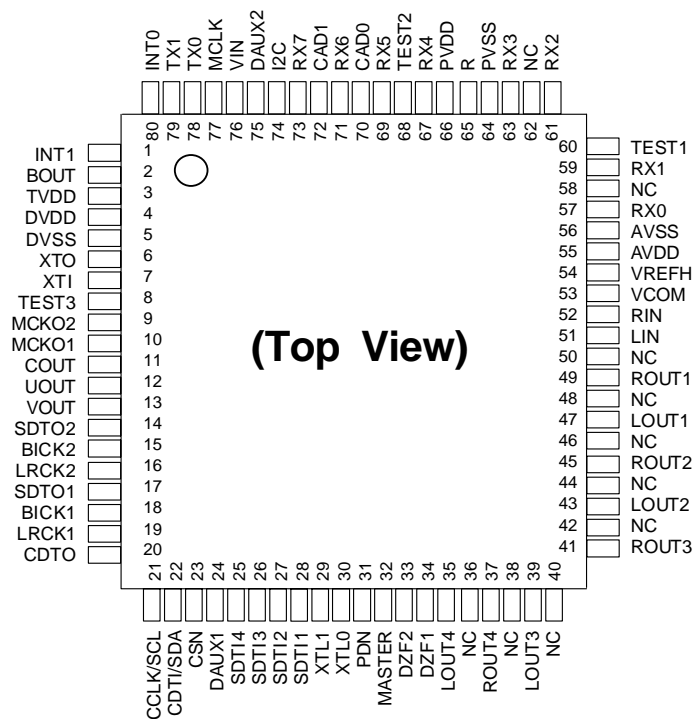


NJW1153 : IC102



No.	SYMBOL	FUNCTION
1	FIL2_R	Rch Bass Filter terminal
2	FIL3_R	Rch Bass Filter DC cut capacitor output terminal
3	FIL4_R	Rch Bass Filter DC cut capacitor input terminal
4	GND	Ground
5	FL+	"Input selector gain control" Lch no-inverted output
6	FL-	"Input selector gain control" Lch inverted output
7	FR+	"Input selector gain control" Rch no-inverted output
8	FR-	"Input selector gain control" Rch inverted output
9	DCLA1	"Input selector" Lch output
10	DCLA2	"Multi-channel selector" Lch input
11	DCRA1	"Input selector" Rch output
12	DCRA2	"Multi-channel selector" Rch input
13	L1IN	"Input selector" Lch input1
14	R1IN	"Input selector" Rch input1
15	L2IN	"Input selector" Lch input2
16	L2IN	"Input selector" Rch input2
17	L3IN	"Input selector" Lch input3
18	R3IN	"Input selector" Rch input3
19	L4IN	"Input selector" Lch input4
20	R4IN	"Input selector" Rch input4
21	L5IN	"Input selector" Lch input5
22	R5IN	"Input selector" Rch input5
23	L6IN	"Input selector" Lch input6
24	R6IN	"Input selector" Rch input6
25	L7IN	"Input selector" Lch input7
26	R7IN	"Input selector" Rch input7
27	L8IN	"Input selector" Lch input8
28	R8IN	"Input selector" Rch input8
29	DATA	Control data signal input
30	CLOCK	Clock signal input
31	LATCH	Latch signal input
32	LAIN	Multi-channel Lch inputA
33	RAIN	Multi-channel Rch inputA
34	CAIN	Multi-channel Cch inputA
35	SLAIN	Multi-channel SLch inputA
36	SRAIN	Multi-channel SRch inputA
37	SWAIN	Multi-channel SWch inputA
38	LBIN	Multi-channel Lch inputB
39	RBIN	Multi-channel Rch inputB
40	CBIN	Multi-channel Cch inputB
41	SLBIN	Multi-channel SLch inputB
42	SRBIN	Multi-channel SRch inputB
43	SWBIN	Multi-channel SWch inputB
44	SurTC	Switching noise rejection capacitor
45	FIL4_L	Lch Bass filter DC cut capacitor input terminal
46	FIL3_L	Lch Bass filter DC cut capacitor output terminal
47	FIL2_L	Lch Bass filter terminal
48	FIL1_L	Lch Treble filter terminal
49	LOUT	Lch output
50	ROUT	Rch output
51	COUT	Cch output
52	SLOUT	SLch output
53	SROUT	SRch output
54	SWOUT	SWch output
55	V+	+ Power supply voltage input
56	GND	Ground
57	V-	- Power supply voltage input
58	RECL1	"Input selector" Lch REC output1
59	RECR1	"Input selector" Rch REC output1
60	RECL2	"Input selector" Lch REC output2
61	RECR2	"Input selector" Rch REC output2
62	RECL3	"Input selector" Lch REC output3
63	RECR3	"Input selector" Rch REC output3
64	FIL1_R	Rch Treble filter terminal

AK4588 : IC401



No.	Pin Name	I/O	Function
1	INT1	O	Interrupt 1 Pin
2	BOUT	O	Block-Start Output Pin for Receiver Input “H” during first 40 frames.
3	TVDD	-	Output Buffer Power Supply Pin, 2.7V~5.5V
4	DVDD	-	Digital Power Supply Pin, 4.5V~5.5V
5	DVSS	-	Digital Ground Pin
6	XTO	O	X'tal clock Output Pin
7	XTI	I	X'tal / External clock Input Pin
8	TEST3	I	Test 3 Pin This pin should be connected to DVSS.
9	MCKO2	O	Master Clock Output 2 Pin
10	MCKO1	O	Master Clock Output 1 Pin
11	COUT	O	C-bit Output Pin for Receiver Input
12	UOUT	O	U-bit Output Pin for Receiver Input
13	VOUT	O	V-bit Output Pin for Receiver Input
14	SDTO2	O	Audio Serial Data Output Pin (DIR/DIT part)
15	BICK2	I/O	Audio Serial Data Clock Pin (DIR/DIT part)
16	LRCK2	I/O	Channel Clock Pin (DIR/DIT part)
17	SDTO1	O	Audio Serial Data Output Pin (ADC/DAC part)
18	BICK1	I/O	Audio Serial Data Clock Pin (ADC/DAC part)
19	LRCK1	I/O	Input Channel Clock Pin
20	CDTO	O	Control Data Output Pin in Serial Mode, I2C pin= “L”.
21	CCLK	I	Control Data Clock Pin in Serial Mode, I2C pin= “L”
	SCL	I	Control Data Clock Pin in Serial Mode, I2C pin= “H”
22	CDTI	I	Control Data Input Pin in Serial Mode, I2C pin= “L”.
	SDA	I/O	Control Data Pin in Serial Mode, I2C pin= “H”.
23	CSN	I	Chip Select Pin in Serial Mode, I2C pin=“L”.
		I	This pin should be connected to DVSS, I2C pin=“H”.
24	DAUX1	I	AUX Audio Serial Data Input Pin (ADC/DAC part)
25	SDTI4	I	DAC4 Audio Serial Data Input Pin
26	SDTI3	I	DAC3 Audio Serial Data Input Pin
27	SDTI2	I	DAC2 Audio Serial Data Input Pin
28	SDTI1	I	DAC1 Audio Serial Data Input Pin
29	XTL1	I	X'tal Frequency Select 0 Pin
30	XTL0	I	X'tal Frequency Select 1 Pin
31	PDN	I	Power-Down Mode Pin When “L”, the AK4588 is powered-down, all output pin goes “L”, all registers are reset. When CAD1-0 pins are changed, the AK4588 should be reset by PDN pin.
32	MASTER	I	Master Mode Select Pin “H”: Master mode, “L”: Slave mode
33	DZF2	O	Zero Input Detect 2 Pin (Table 13) When the input data of the group 1 follow total 8192 LRCK cycles with “0” input data, this pin goes to “H”. When RSTN1 bit is “0” or PWDAN bit is “0”, this pin goes to “H”.
	OVF	O	Analog Input Overflow Detect Pin This pin goes to “H” if the analog input of Lch or Rch overflows. This pin becomes OVF pin if OVFE bit is set to 1.
34	DZF1	O	Zero Input Detect 1 Pin (Table 13) When the input data of the group 1 follow total 8192 LRCK cycles with “0” input data, this pin goes to “H”. When RSTN1 bit is “0” or PWDAN bit is “0”, this pin goes to “H”.
35	LOUT4	O	DAC4 Lch Analog Output Pin
36	NC	-	No Connect pin No internal bonding. This pin should be opened.
37	ROUT4	O	DAC4 Rch Analog Output Pin
38	NC	-	No Connect pin No internal bonding. This pin should be opened.
39	LOUT3	O	DAC3 Lch Analog Output Pin

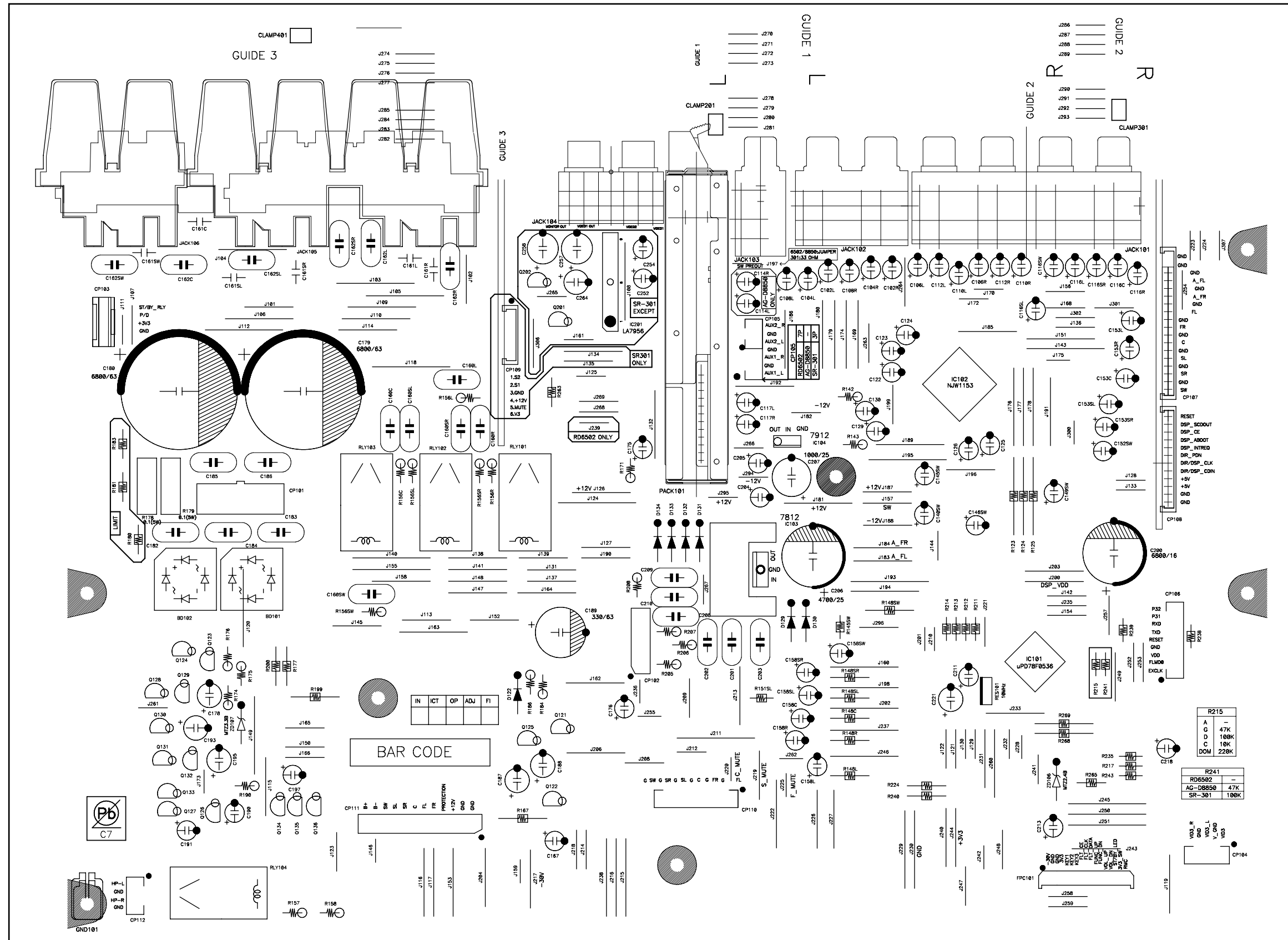
No.	Pin Name	I/O	Function
40	NC	-	No Connect pin No internal bonding. This pin should be opened.
41	ROUT3	O	DAC3 Rch Analog Output Pin
42	NC	-	No Connect pin No internal bonding. This pin should be opened.
43	LOUT2	O	DAC2 Lch Analog Output Pin
44	NC	-	No Connect pin No internal bonding. This pin should be opened.
45	ROUT2	O	DAC2 Rch Analog Output Pin
46	NC	-	No Connect pin No internal bonding. This pin should be opened.
47	LOUT1	O	DAC1 Lch Analog Output Pin
48	NC	-	No Connect pin No internal bonding. This pin should be opened.
49	ROUT1	O	DAC1 Rch Analog Output Pin
50	NC	-	No Connect pin No internal bonding. This pin should be opened.
51	LIN	I	Lch Analog Input Pin
52	RIN	I	Rch Analog Input Pin
53	VCOM	-	Common Voltage Output Pin 2.2 μ F capacitor should be connected to AVSS externally.
54	VREFH	-	Positive Voltage Reference Input Pin, AVDD
55	AVDD	-	Analog Power Supply Pin, 4.5V~5.5V
56	AVSS	-	Analog Ground Pin, 0V
57	RX0	I	Receiver Channel 0 Pin (Internal biased pin. Internally biased at PVDD/2)
58	NC	-	No Connect pin No internal bonding. This pin should be connected to PVSS.
59	RX1	I	Receiver Channel 1 Pin (Internal biased pin. Internally biased at PVDD/2)
60	TEST1	I	Test 1 Pin This pin should be connected to PVSS.
61	RX2	I	Receiver Channel 2 Pin (Internal biased pin. Internally biased at PVDD/2)
62	NC	-	No Connect pin No internal bonding. This pin should be connected to PVSS.
63	RX3	I	Receiver Channel 3 Pin (Internal biased pin. Internally biased at PVDD/2)
64	PVSS	-	PLL Ground pin
65	R	-	External Resistor Pin 12k Ω +/-1% resistor should be connected to PVSS externally.
66	PVDD	-	PLL Power supply Pin, 4.5V~5.5V
67	RX4	I	Receiver Channel 4 Pin (Internal biased pin. Internally biased at PVDD/2)
68	TEST2	I	Test 2 Pin This pin should be connected to PVSS.
69	RX5	I	Receiver Channel 5 Pin (Internal biased pin. Internally biased at PVDD/2)
70	CAD0	I	Chip Address 0 Pin (ADC/DAC part)
71	RX6	I	Receiver Channel 6 Pin (Internal biased pin. Internally biased at PVDD/2)
72	CAD1	I	Chip Address 1 Pin (ADC/DAC part)
73	RX7	I	Receiver Channel 7 Pin (Internal biased pin. Internally biased at PVDD/2)
74	I2C	I	Control Mode Select Pin. “L”: 4-wire Serial, “H”: I ² C Bus
75	DAUX2	I	Auxiliary Audio Data Input Pin (DIR/DIT part)
76	VIN	I	V-bit Input Pin for Transmitter Output
77	MCLK	I	Master Clock Input Pin
78	TX0	O	Transmit Channel (Through Data) Output 0 Pin
79	TX1	O	Transmit Channel Output1 pin When TX bit = “0”, Transmit Channel (Through Data) Output 1 Pin. When TX bit = “1”, Transmit Channel (DAUX2 Data) Output Pin (Default).
80	INT0	O	Interrupt 0 Pin

Note : All input pins except internal biased pins and internal pull-down pin should not be left floating.

PRINTED CIRCUIT BOARDS (I)

Model No.: RD-6502

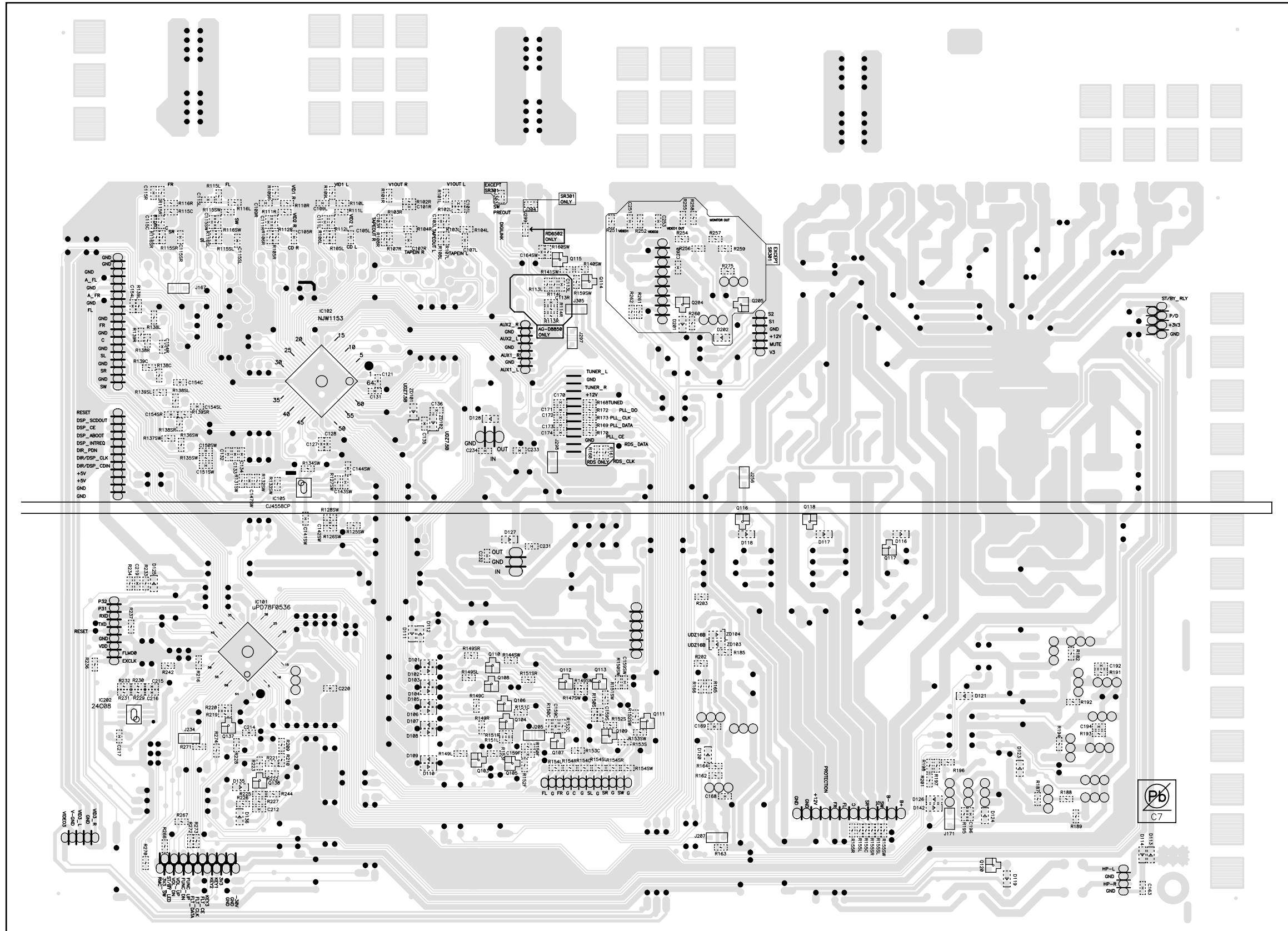
PCB1 (MAIN-TOP)



PRINTED CIRCUIT BOARDS (II)

Model No.: RD-6502

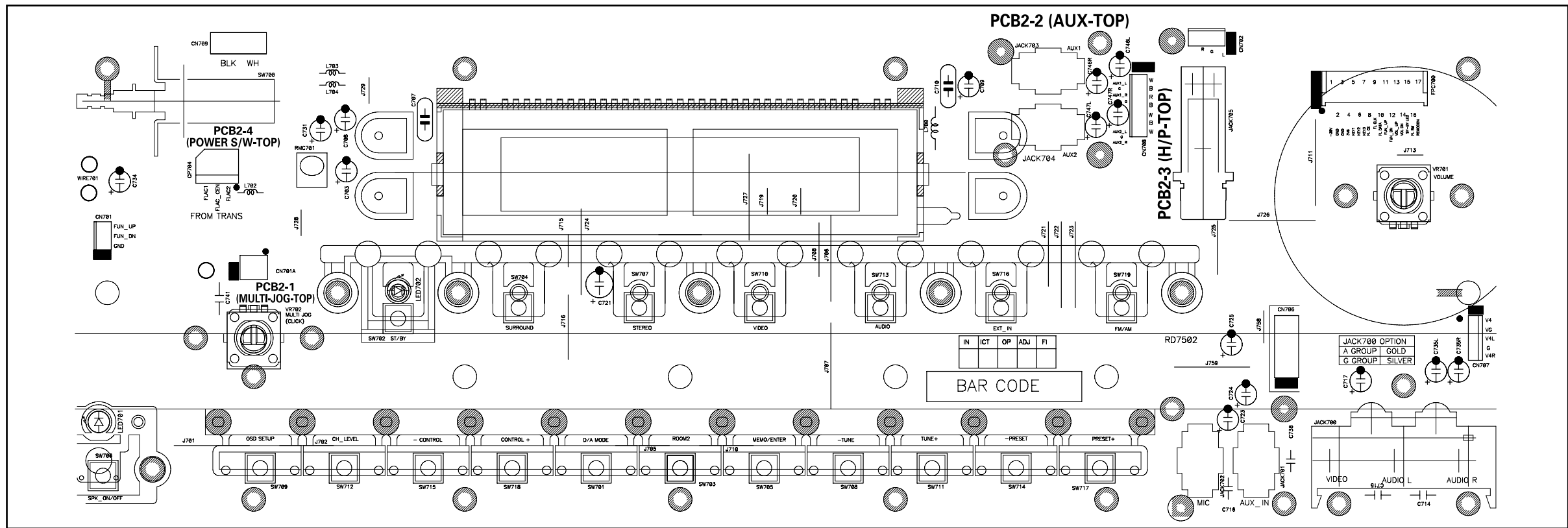
PCB1 (MAIN-BOTTOM)



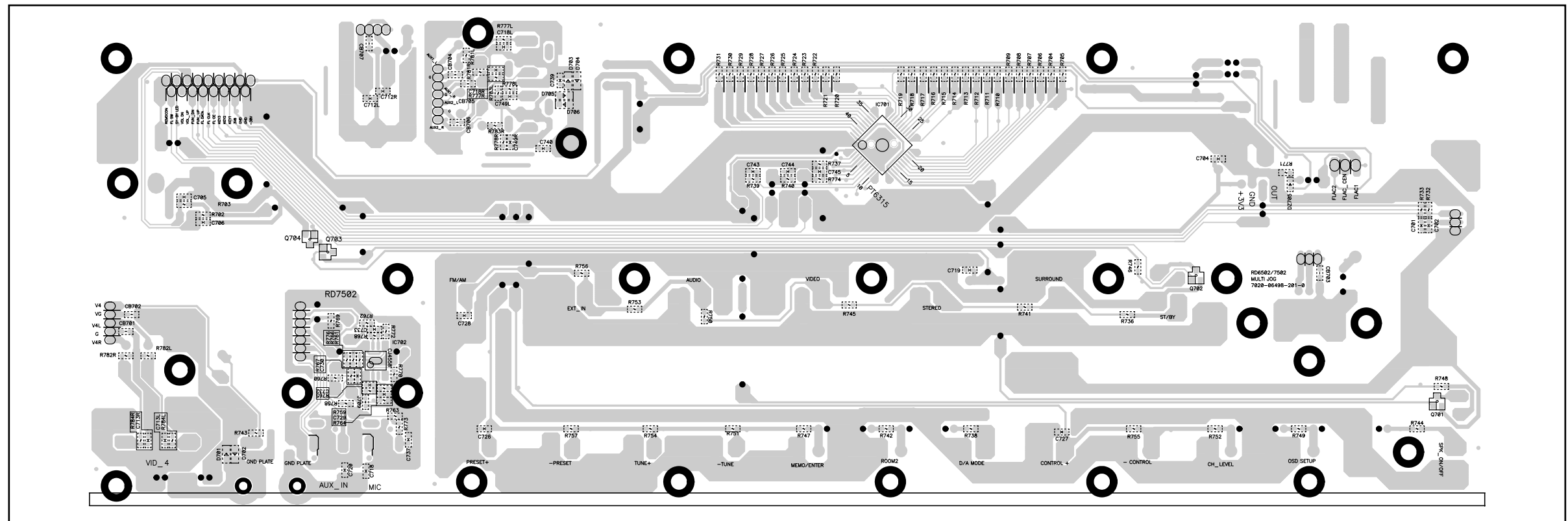
PRINTED CIRCUIT BOARDS (III)

Model No.: RD-6502

PCB2 (FRONT-TOP)



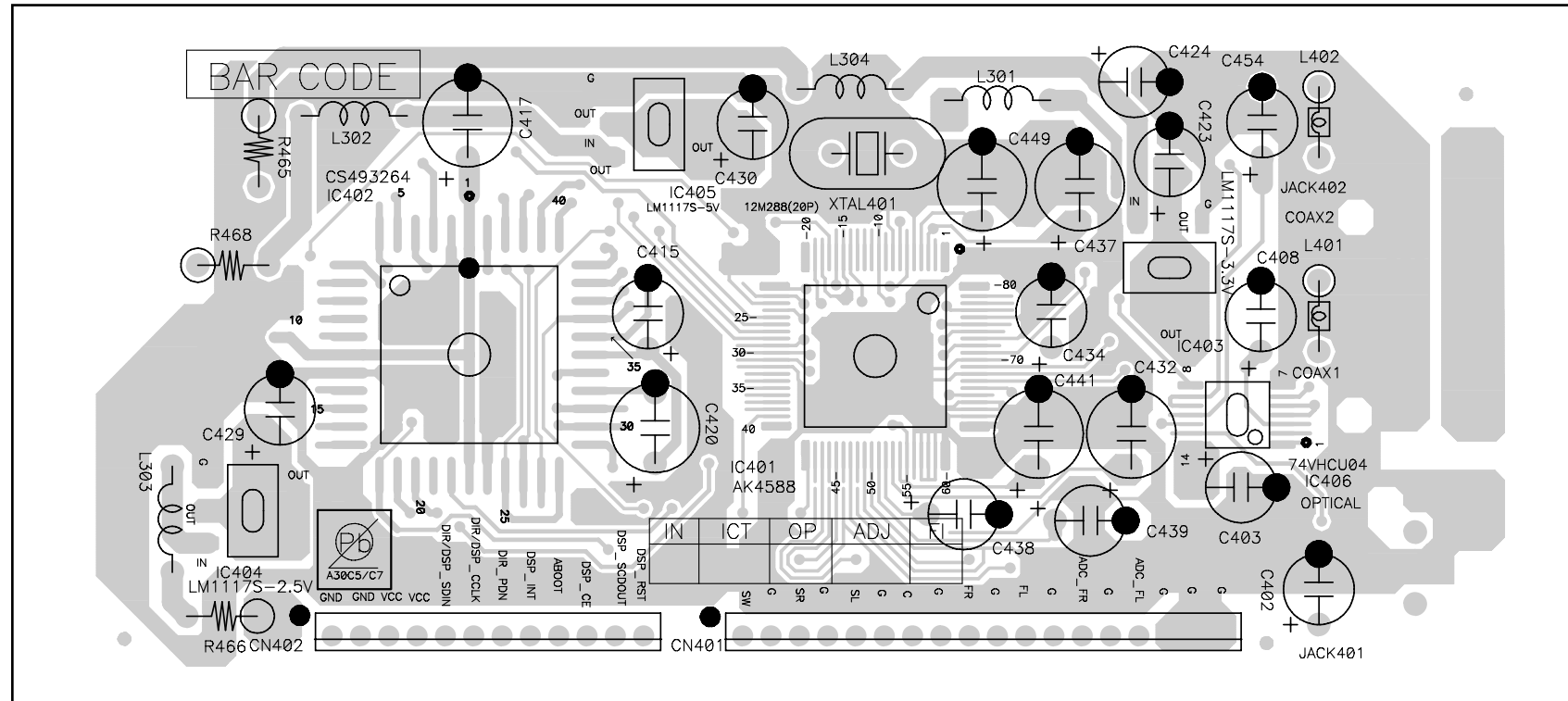
PCB2 (FRONT-BOTTOM)



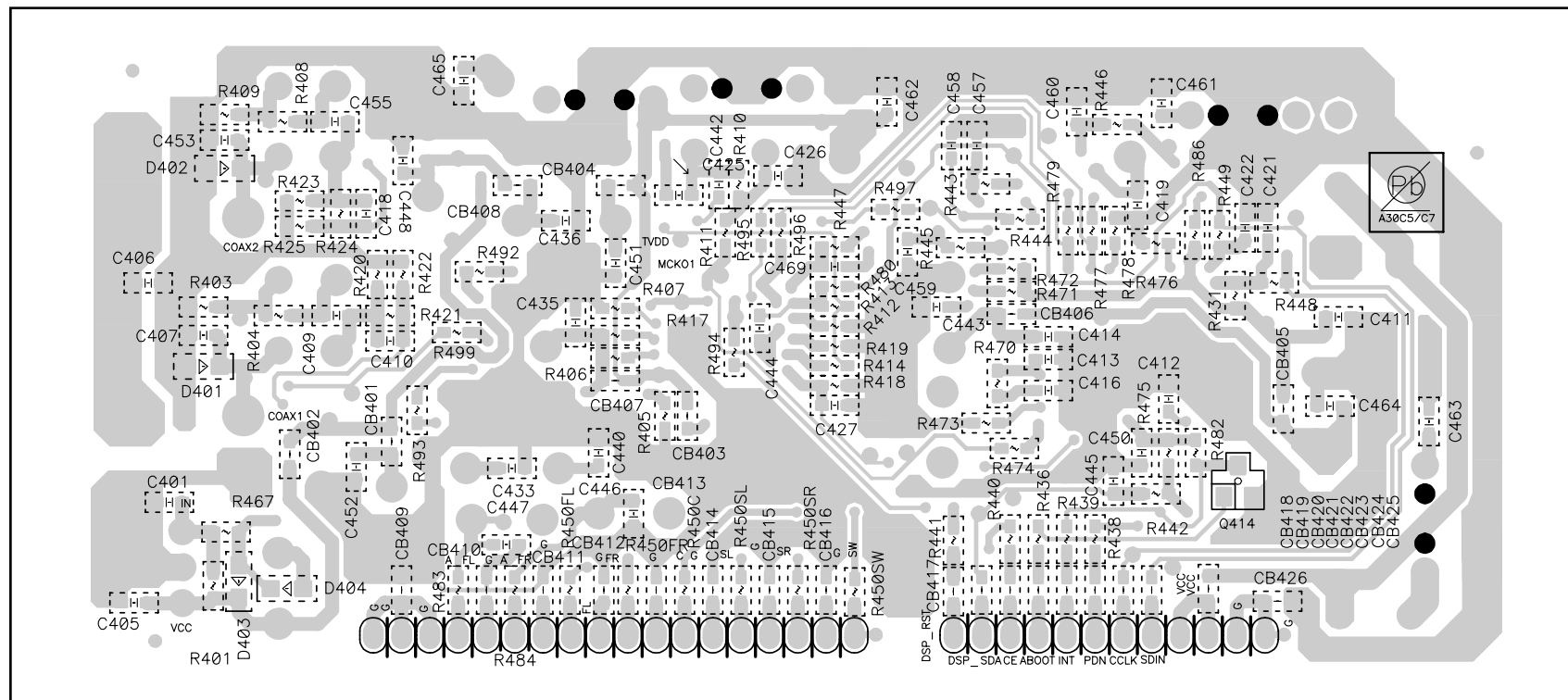
PRINTED CIRCUIT BOARDS (IV)

Model No.: RD-6502

PCB3 (DSP-TOP)



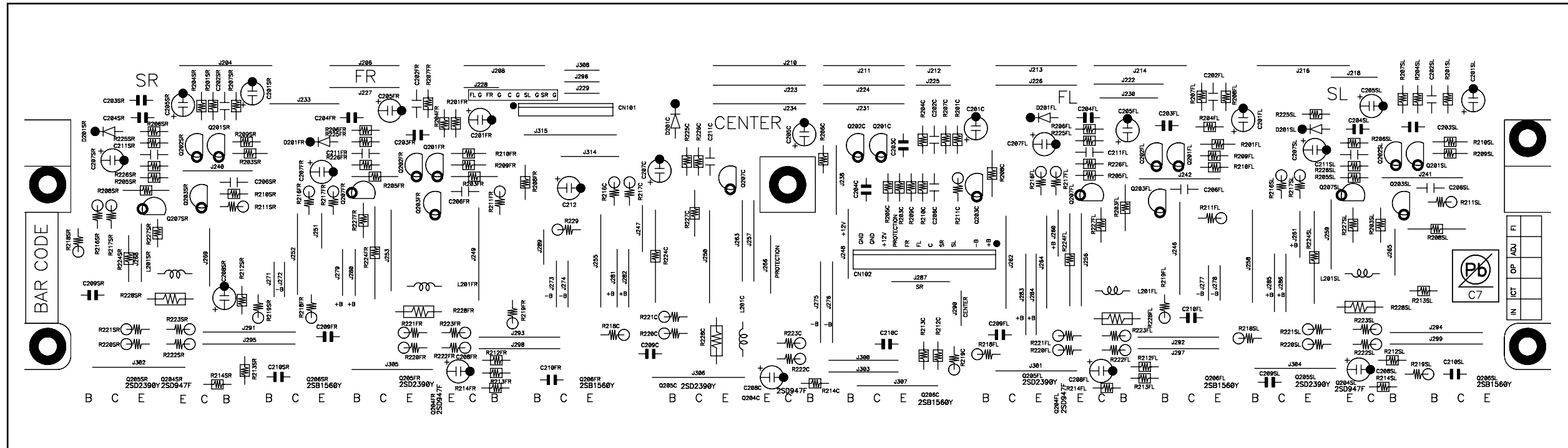
PCB3 (DSP-BOTTOM)



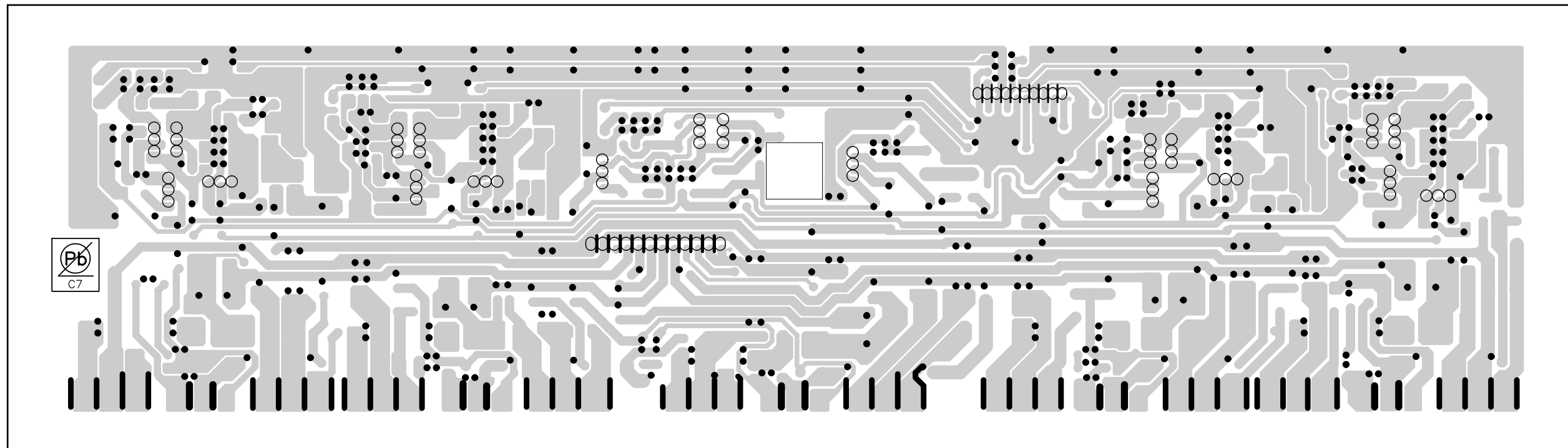
PRINTED CIRCUIT BOARDS (V)

Model No.: RD-6502

PCB4 (AMP-TOP)



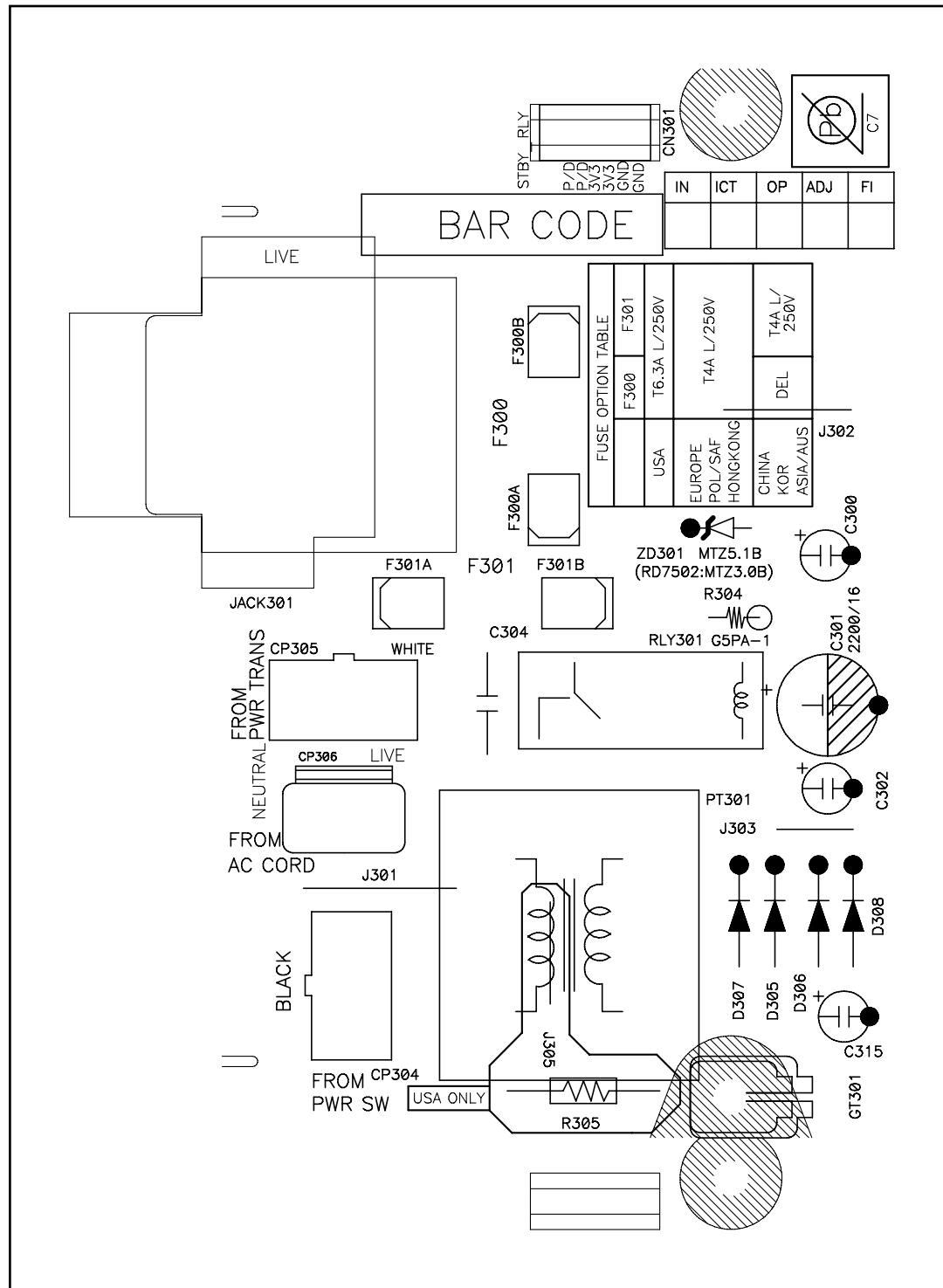
PCB4 (AMP-BOTTOM)



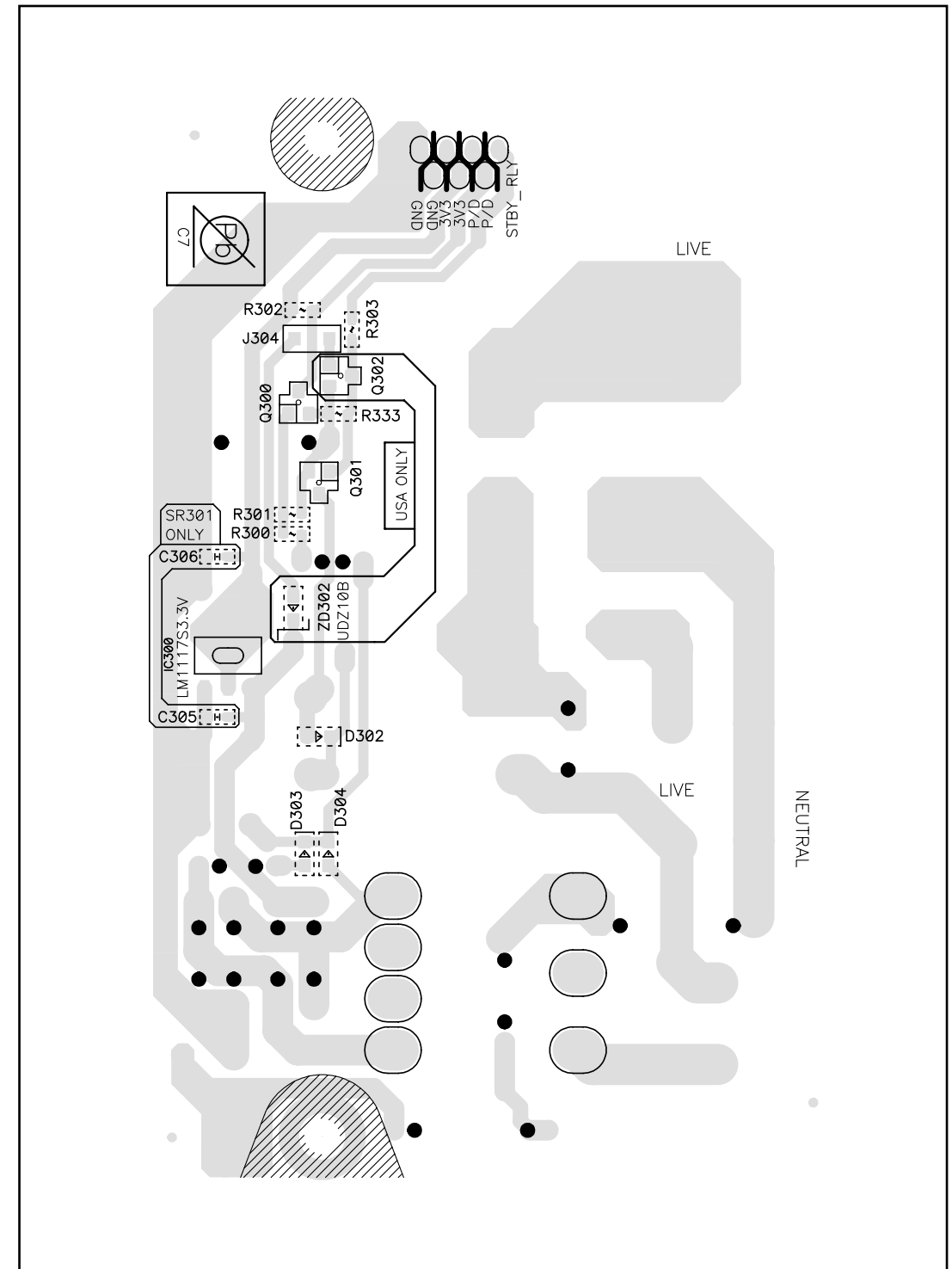
PRINTED CIRCUIT BOARDS (VI)

Model No.: RD-6502

PCB5 (ST-BY-TOP)

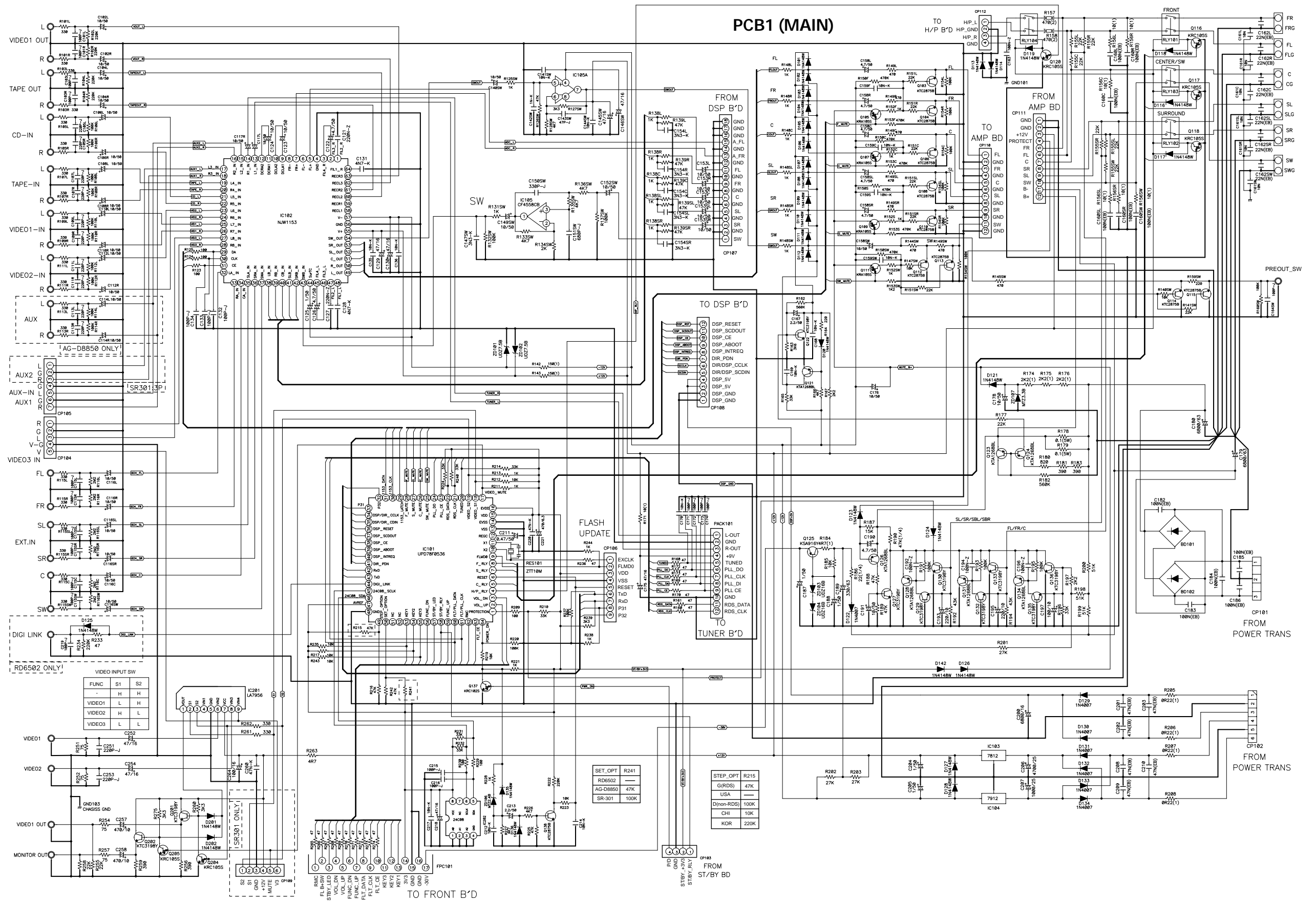


PCB5 (ST-BY-BOTTOM)



SCHEMATIC DIAGRAMS (I)

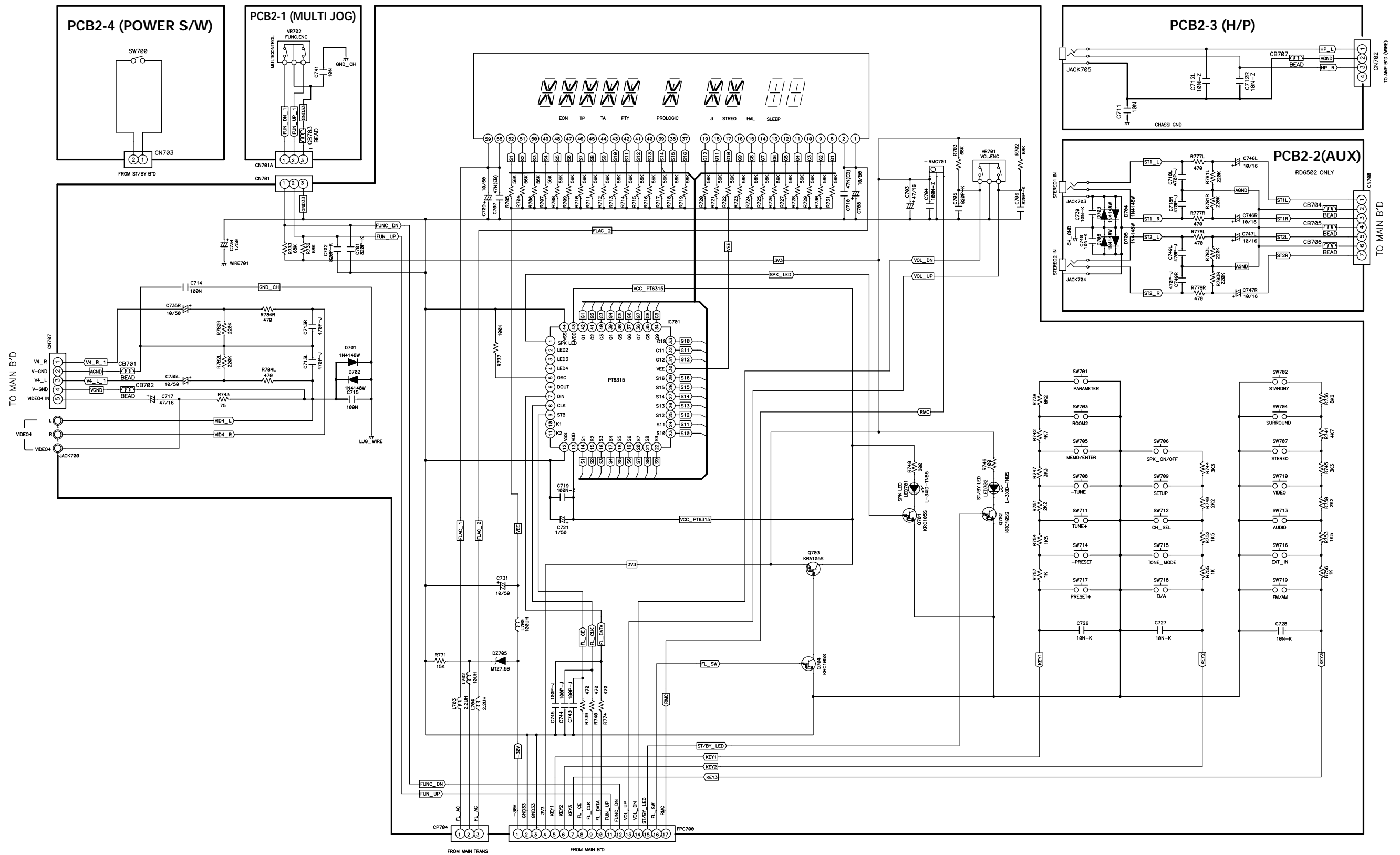
Model No.: RD-6502



SCHEMATIC DIAGRAMS (II)

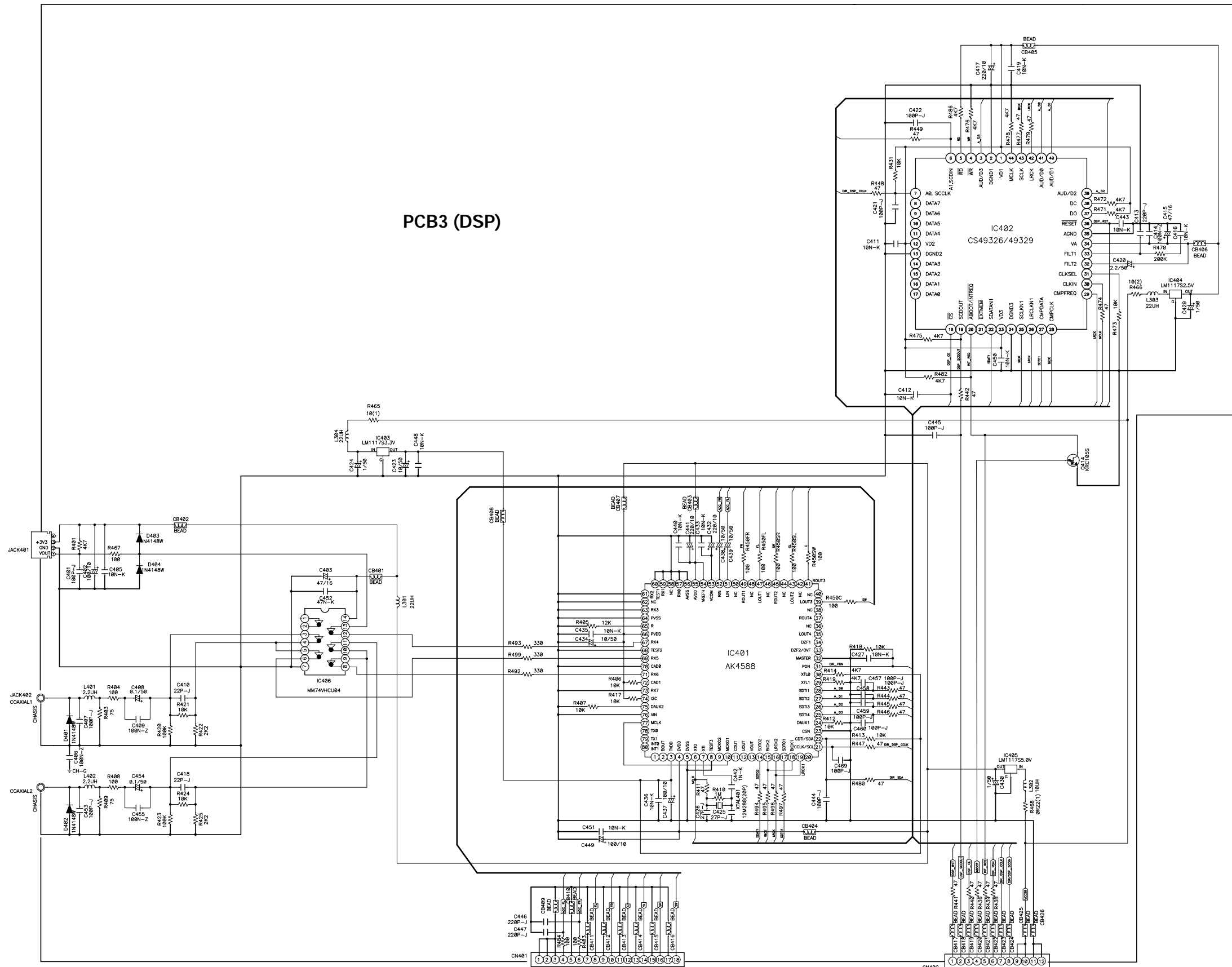
Model No.: RD-6502




PCB2 (FRONT)



SCHEMATIC DIAGRAMS (III)

Model No.: RD-6502

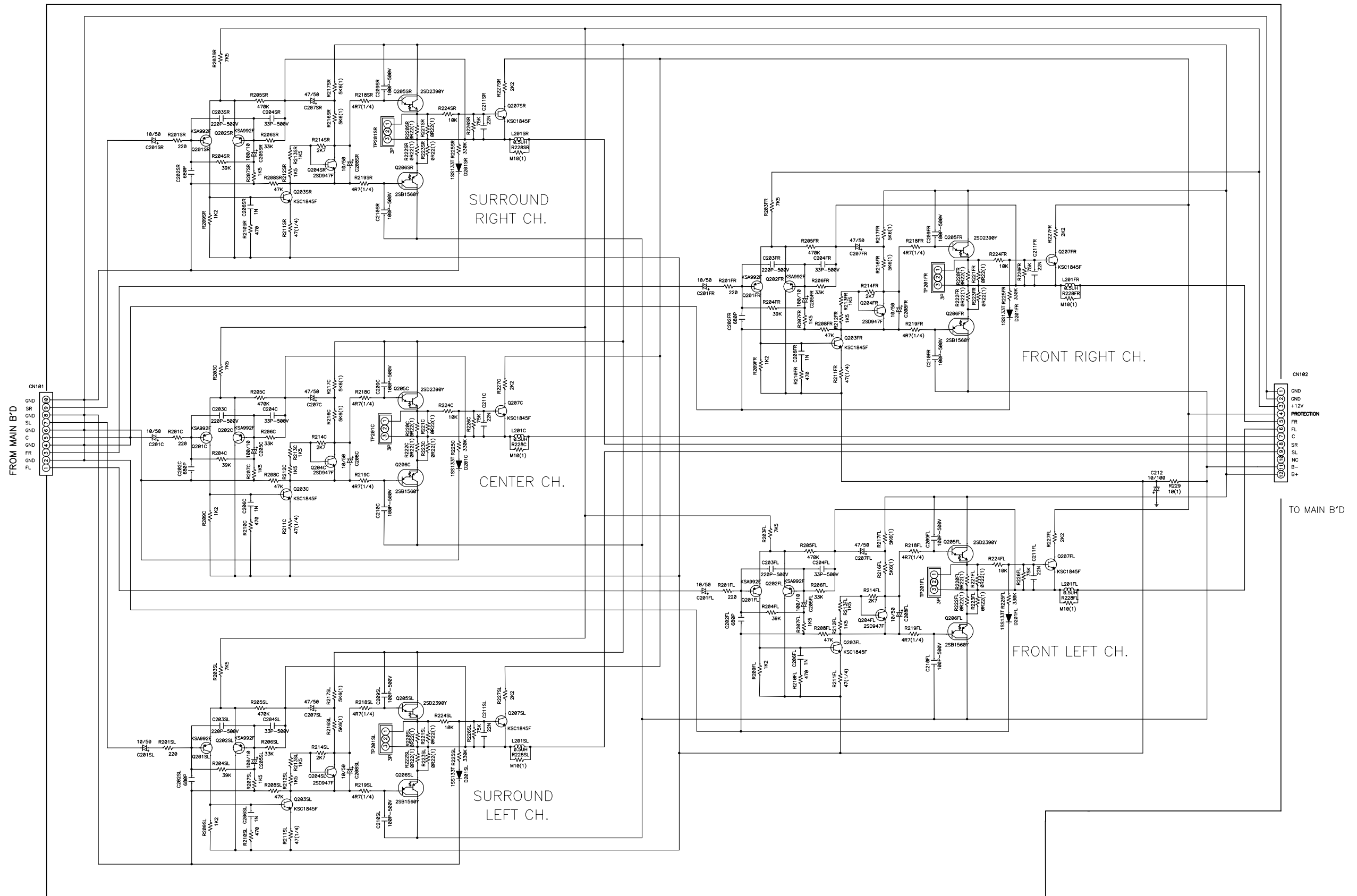


- NOTES**
1. Resistor values are indicated in ohms unless otherwise specified
[k = 1.000 m = 1.000.000]
 2. Capacitor values are indicated in microfarads unless otherwise specified.
[p = micro-microfarads]
 3.  : These resistor are to be segregated from printed wiring board or other accessible parts.
- CAUTION**
Safety precaution to be followed during servicing 
- 1] Since those parts marked with  are critical parts for safety, use only the one described in the parts list.
 - 2] Before returning the set to the customer make appropriate leakage current or resistance measurements to determine the exposed parts are properly insulated from the supply circuit.

SCHEMATIC DIAGRAMS (IV)

PCB4 (AMP)

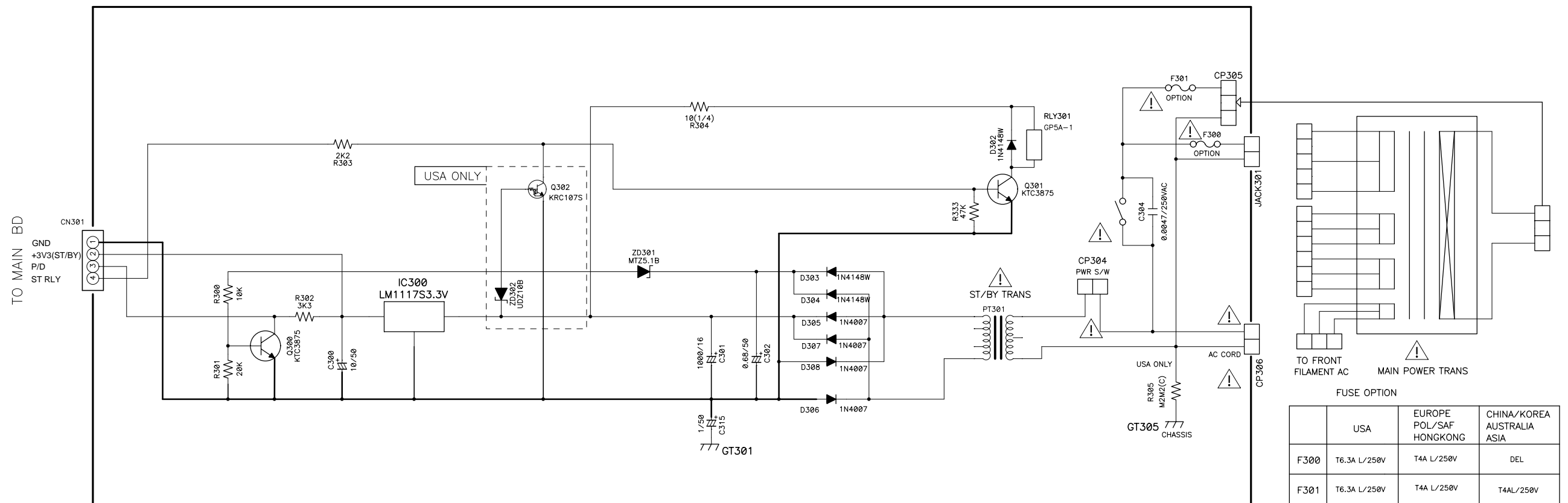
Model No.: RD-6502



SCHEMATIC DIAGRAMS (V)

Model No.: RD-6502

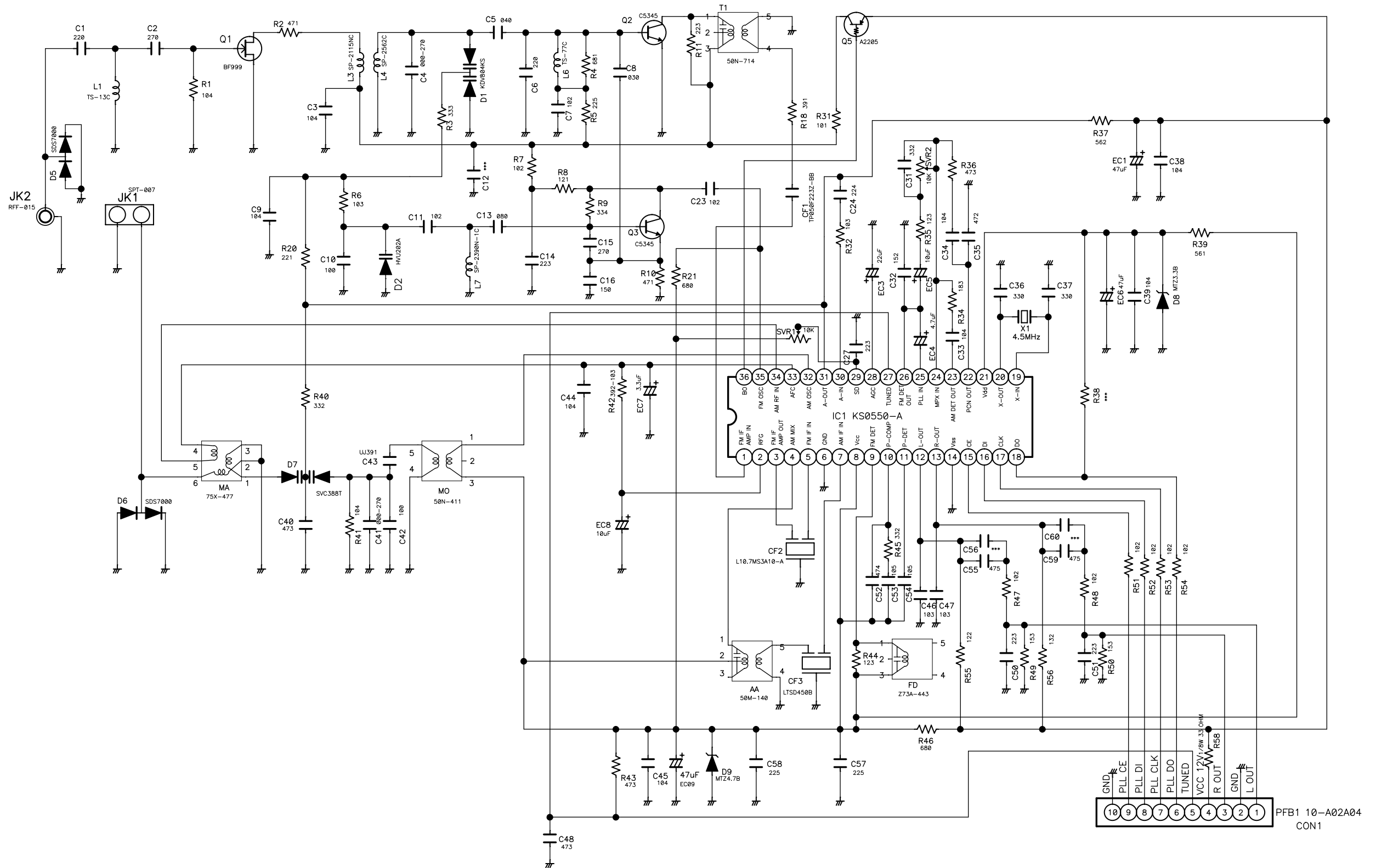
PCB5 (ST-BY)



SCHEMATIC DIAGRAMS (VI)

Model No.: RD-6502

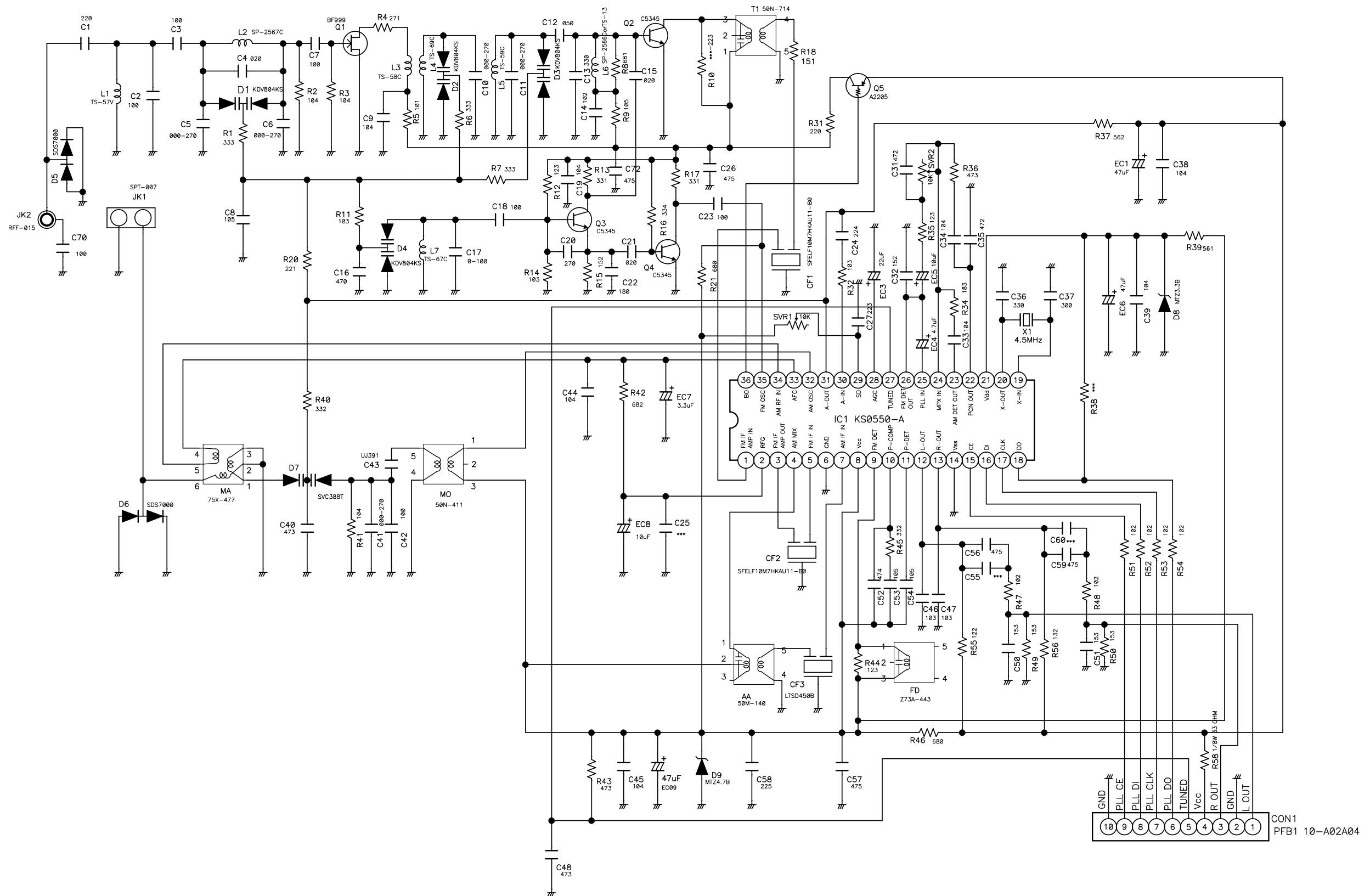
TUNER ASS'Y(A ONLY)



SCHEMATIC DIAGRAMS (VII)

Model No.: RD-6502

TUNER ASS'Y(C/D/E/K ONLY)



SCHEMATIC DIAGRAMS (VIII)

Model No.: RD-6502

TUNER ASS'Y(RDS ONLY)

