MITEL Technical Data

MT8820

CMOS/LSI DUAL-TONE MULTI-FREQUENCY (DTMF) RECEIVER/DECODER

(ADVANCED INFORMATION) 11/78

FEATURING:

- CENTRAL OFFICE QUALITY DETECTION
- EXCELLENT VOICE TALK-OFF
- DETECT TIMES DOWN TO 20MS
- 5V to 15V OPERATION
- LATCHED 3-STATE BUFFERED OUTPUTS
- STD. 24 PIN PACKAGES
- DETECTS ALL 16 DTMF COMBINATIONS
- 3 OUTPUT CODES AVAILABLE
- USES STD. 3.58 MHz TV CRYSTAL
- BUILT-IN POWER-ON RESET
- LOW POWER CMOS CIRCUITRY
- ADJUSTABLE ACQUISITION & RELEASE TIMES

DESCRIPTION:

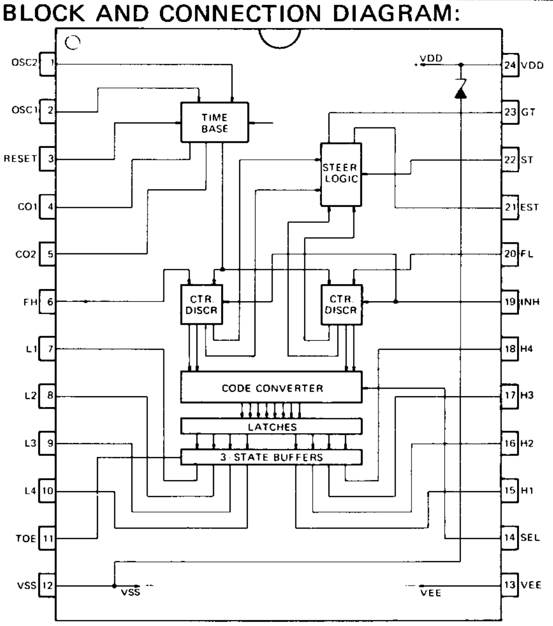
The MT8820 is a CMOS/LSI circuit designed to detect all 16 DTMF combinations of mixed tones using digital circuit techniques. The circuit accepts the tones after filtering, separating and squaring of the high and low frequency groups. It then converts the input signals into digital output codes which represents the number that was originated at the transmitting unit. The circuit will accurately discriminate between adjacent frequencies in both the high and low bands in the presence of noise and normal voices. The actual algorithm used was developed imperically in actual telecommunication environments and by using the statistical differences between noise, tone and speech.

The internal timing base uses a 3.58 MHz TV crystal to provide accurate detection. A built-in "Power-On Reset" ensures proper start-up whenever power is applied or reapplied to the circuit. Either 5 volt or 12 to 15 volt operation is offered as a result of an on-chip power supply regulator circuit.

The output code converter consists of a ROM which provides two different 8-bit code formats. These are; a 2-of-8 (4 rows & 4 columns) or 4-bit hexadecimal and a 4-bit code compatable with the GI AY5-9100 Dial Pulse Converter circuit. The 8 outputs are latched and buffered 3-state circuitry.

Steering logic and a guard time input are provided to offer adjustable "acquire time" and "release time" of circuit.

BLOCK AND CONNECTION DIAGRAM:



PART NUMBERS:

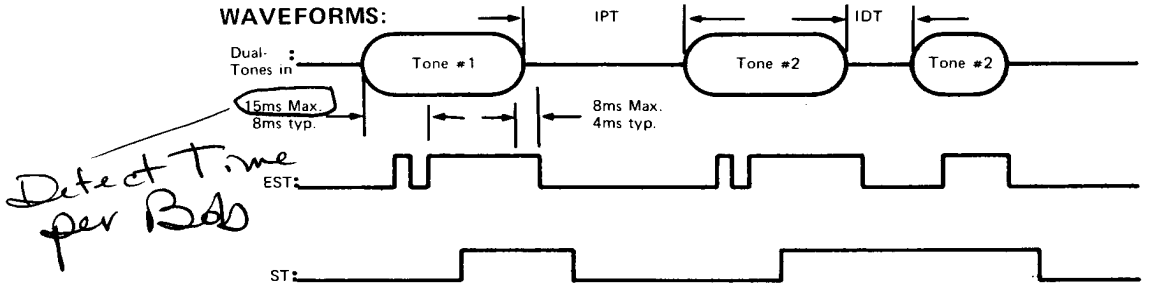
MT8820 AE	– 24 PIN PLASTIC DIP,	– 40° C to 85° C
MT8820 AC	– 24 PIN CERAMIC DIP,	– 40° C to 85° C
MT8820 AD	– 24 PIN CERAMIC DIP,	– 55° C to 125° C

PIN	NAME	DESCRIPTION
1 2	OSC 2 OSC 1	**Oscillator Inputs.** Input and output of inverter circuit, to which a 3.57954S MHz TV color-burst crystal is connected.
3	RESET	**Reset Input.** A logic HIGH on this pin causes the circuit to be reset to start of detect mode.
4 5	CO 1 CO 2	**18.2KHz Clock Outputs.** Non-overlapping active-level HIGH signals for use with external circuits.
6	FH	**High Frequency Group (active HIGH) Input.** Accepts and detects the high band frequencies of 1209Hz, 1336Hz, 1477Hz and 1633Hz.
7 8 9 10	L 1 L 2 L 3 L 4	**Low-Group (active HIGH) Outputs.** With a logic HIGH on the SEL Input (pin 14), this low-group output will provide the low end of the 2-of-8 code format when combined with the high-group outputs. A logic LOW on SEL (pin 14) will cause these to provide a hexadecimal code format output.
11	TOE	**3-State Output Enable Input.** A logic HIGH on this input pin will cause the 8 buffered outputs to remain in their high-impedance state.
12	VSS	Negative Logic Voltage Input Terminal.
13	VEE	Negative Voltage Input Terminal.
14	SEL	**Select Code Input.** A logic HIGH on this input selects the 2-of-8 code output on L1, L2, L3, L4, H1, H2, H3, H4 pins. While a logic LOW on this pin causes L1, L2, L3, L4 to be a hexadecimal code, and H1, H2, H3, H4 to be in a code format compatable for the G.I. AY5-9100 device.
15 16 17 18	H1 H2 H3 H4	**High-Group (active HIGH) outputs.** A logic HIGH on the SEL input (pin 14) cause these outputs to provide the high end of a 2-of-8 code format when combined with the low-group outputs. When a logic LOW is applied to the SEL input, these outputs provide a code which is compatable with the GI AY5-9100 device.
19	INH	**Inhibit Input.** A logic HIGH on this input pin will inhibit the circuit from detecting the input frequencies corresponding to the 6 tone-pairs normally not used. This further improves "talk-off" for these applications.
20	FL	**Low Frequency Group (active HIGH) Input.** Accepts and detects the low band frequencies of 697Hz, 770Hz, 852Hz and 941Hz.
21	EST	**Early Steering (active HIGH) Output.** This output will go to a logic HIGH state as soon as a recognizable tone-pair is detected. A noise spike, a frequency drift or even a monentary drop in the incoming tones will cause this pin to return to a logic LOW state.
22	ST	**Steering Input.** A logic HIGH level applied to this input will cause the circuit to accept and latch the code for the tone-pair detected. It also causes the GT output (pin 21) to go to a logic HIGH. A logic LOW level on this pin will release the circuit to accept a new tone-pair. GT output will return to a logic LOW state.
23	GT	**Guard Time Output.** This output goes to a logic HIGH when the circuit detects and accepts a valid tone-pair. It will return to a logic LOW whenever the ST input (pin22) detects logic LOW level.
24	VDD	Positive Voltage Input Terminal

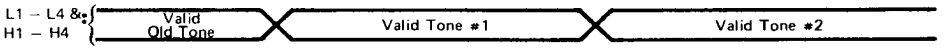
ELECTRICAL CHARACTERISTICS (TA = 25° C)

PIN	SYMBOL	CHARACTERISTIC	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT	CONDITIONS VDD	CONDITIONS VSS	CONDITIONS VEE
24	I_{DD}	Quiescent Current with Osc. operating at 3.58 MHz.		300 1500 2500		µAdc	5V 12V 15V	OV (1) (1)	OV OV OV
–	VIH	Input High Voltage, all inputs.		2.75 9.00		Vdc	VDD = 5V VDD = 15V		
–	VIL	Input LOW Voltage, all inputs.		2.25 6.00		Vdc	VDD = 5V VDD = 15V		
–	VOH	Output HIGH Voltage, all outputs.		4.5 11.5 14.0		Vdc	VDD = 5V, IOH=150µA VDD = 12V, IOH=350µA VDD = 15V, IOH=1.1 µA		
–	VOL	Output LOW Voltage, all outputs.		0.25 0.25 0.25		Vdc	VDD = 5V, IOL=0.4mA VDD = 12V, IOL=0.4mA VDD = 15V, IOL=2.4mA		
–	IOH	Output HIGH Current, all outputs.		–3.0 –3.0 –3.0		µAdc	VDD = 5V, VOH= 2.8V VDD = 12V, VOH= 8.1V VDD = 15V, VOH=13.1V		
–	IOL	Output LOW Current, all outputs.		1.0 3.0 8.0		µAdc	VDD = 5V, VOL=0.4V VDD = 12V, VOL=0.5V VDD = 15V, VOL=1.5V		
6/20	STV STV IPT IDT	Signal Time Valid Signal Time Not Valid Interdigit Pause Time Interdigit Drop-Out Time.	30 30 		 20 15	mS	See Waveforms below and figure 2 VDD = 5V.		
–	TP	Propagation Delay, TOE to L1–L4, H1–H4.			300	nS	VDD = 5V, See Fig. 2		

(1) See Figure 1.



MAXIMUM RATING
(Voltages referenced to VEE)



RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	VDD	–0.5 to + 16	Vdc
Logic Negative Supply	VSS	–0.5 to VDD	Vdc
Input Voltage, All Inputs	VIN	–0.25 to VDD + 0.25	Vdc
Operating Temperature Range	TA	–55 to + 125	°C
Storage Temperature Range	TSTG	–65 to + 150	°C

FIGURE 1. POWER SUPPLY OPTIONAL CONNECTIONS.

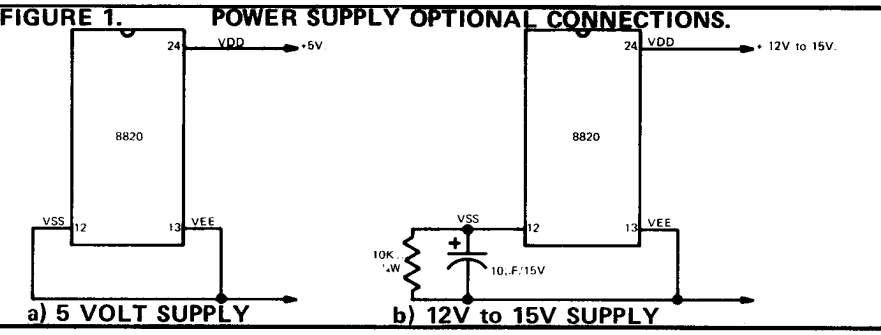
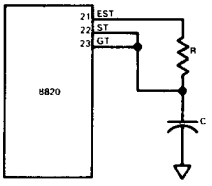
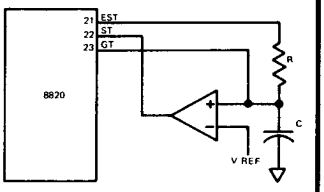


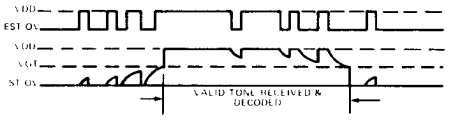
FIGURE 2. CONNECTIONS FOR EST, GT AND ST PINS.

a) VGT DETECT LEVEL ≅ 1/2V_{DD}



b) VGT DETECT LEVEL = V. REF.





OUTPUT TRUTH TABLE

OUTPUT FORMATS		SEL=H (2-of-8 Code)								SEL = L (Hexadecimal Code), H format compatible with GIAV-5-9100 Unit.							
		L1	L2	L3	L4	H1	H2	H3	H4	L1	L2	L3	L4	H1	H2	H3	H4
ORIGINAL DATA TRANSMITTED	1	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	2	H	L	L	L	L	H	L	L	L	H	L	L	L	H	L	L
	3	H	L	L	L	L	L	H	L	H	H	L	L	L	L	H	L
	4	L	H	L	L	H	L	L	L	L	L	H	L	L	L	L	H
	5	L	H	L	L	L	H	L	L	H	L	H	L	L	H	L	H
	6	L	H	L	L	L	L	H	L	L	H	H	L	L	L	H	H
	7	L	L	H	L	H	L	L	L	H	H	H	L	H	L	L	L
	8	L	L	H	L	L	H	L	L	L	L	L	H	H	H	L	L
	9	L	L	H	L	L	L	H	L	H	L	L	H	H	L	H	L
	0	L	L	L	H	L	H	L	L	L	H	L	H	L	H	H	L
	*	L	L	L	H	H	L	L	L	H	H	L	H	H	L	H	H
	#	L	L	L	H	L	L	H	L	L	L	H	H	H	L	L	H
	A	H	L	L	L	L	L	L	H	H	L	H	H	H	H	H	L
	B	L	H	L	L	L	L	L	H	L	H	H	H	H	H	L	H
	C	L	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H
	D	L	L	L	H	L	L	L	H	L	L	L	L	H	H	H	H

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