1977 DATA CATALOG

MICRO ELECTRONICS

GENERAL INSTRUMENT CORPORATION • MICROELECTRONICS

CALCULATORS — Section 2

FUNCTION	DESCRIPTION	9V LED	9V FLUOR.	9V LED (DIRECT)	15V FLUOR.	15V LED	PAGE NO.
8 DIGIT BASIC	4 functions and percent key.	C-683	CF-683	C-683D*	CF-583	C-583	2-5/8*
	4 functions, percent key, one-key or multi-key memory.	C-685	CF-685	C-685D*	CF-585	C-585	2-6/8*
8 DIGIT ALGEBRA	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, choice of 20 to 29 keys		CF-687*	C-687D*	CF-599	C-589	2-7/8*
	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, brackets, inch-centimeter conversion, choice of 24 to 30 keys.		CF-689	C-689D	CF-589HV	—	2-8
9 DIGIT BASIC	4 functions and percent key				CF-593	C-593	2-10
	4 functions, percent key, one-key memory.				CF-594	C-594	2-11
	4 functions, percent key, multi-key memory.				CF-595	C-595	2-12
9 DIGIT SCIENTIFIC	Basic 4 functions, scientific notation, sin, cos, tan, arc sin, arc cos, arc tan, memory, square root, pi, natural logs, 1/x, e^x, memory exchange, degrees and radians, exponent range to 99, choice of 19 to 35 keys				CF-596	C-596	2-13
	All the above plus: 0 to 10^{99} degree trig range, $\log_{10}$, y^x, extended digit accuracy of trancendentals, choice of 21 to 38 keys.				CF-598	C-598	2-14
	All the above plus: two levels of parenthesis, x^2, %, +/-, choice of 24 to 41 keys				CF-599	C-599	2-15

FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
8 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, and other features. Interfaces with the Olivetti Pu1100 dot matrix printer Option for use with thermal printing version of Pu1100.	C-716	40 DIP	Accumulator and 4 key memory	2-17
12 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, memory-in-use indicator, rounding options, non-add (#)/date key, and other features. Interfaces with the Shinshu Seiki Model 310 impact printer	C-717	40 DIP	Accumulator and Grend Total Memories.	2-18
		C-717X			
		C-718		Accumulator, item counter, and four-key independent memory.	2-19
PRINTER-DISPLAY INTERFACE	Adds display capability to the C-717X and C-718 printing calculator circuits	C-719	28 DIP	For both LED and flourescent displays	2-20
	Adds display capability to the C-716 printing calculator circuit.	C-720			2-21

CLOCKS — Section 3

FUNCTION	DESCRIPTION	PART NUMBER	DISPLAY TYPE	FLASHING SECONDS	ZERO BLANKING	50/60 Hz OPERATION	PACKAGE	FEATURES	PAGE NO.
4 DIGIT	12/24 hour clock	AY-5-1200A	7-SEGMENT FLUORESCENT		✓	✓	24 DIP	Direct fluorescent display drive.	3-2
		AY-5-1202A	7-SEGMENT FLOURESCENT	✓	✓	✓	24 DIP	Direct flourescent display drive.	3-2
		AY-5-1203A	BCD OUTPUTS	✓		✓	24 DIP	See AY-5-8320 TV circuit.	3-2
		AY-5-1204A	7-SEGMENT FLUORESCENT	✓		✓	24 DIP	Direct fluorescent display drive.	3-2
		AY-5-1224A	BCD OR 7-SEGMENT LED		✓	✓	16 DIP	Zero blanking in 12 hour mode only.	3-5
4 DIGIT WITH ALARM	12 hour clock, 24 hour alarm	CK3000	7-SEGMENT PLASMA	✓	✓	✓	40 DIP	Snooze alarm, individual digit drive.	3-7
		CK3100	7-SEGMENT LED	✓	✓	✓	40 DIP	Snooze alarm, individual digit drive.	3-7
	12/24 hour clock, 24 hour alarm	CK3200	7-SEGMENT PLASMA	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits	3-12
		CK3400	7-SEGMENT LED	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits	3-12
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm	CK3300	7-SEGMENT LED	✓	✓	✓	28 DIP	Snooze alarm, duplexed digits, sleep-timer, timeswitch, battery standby capability	3-20
4 DIGIT AUTOMOBILE CLOCK	12 hour clock	CK3500	7-SEGMENT LED		✓	CRYSTAL INPUT	40 DIP	Operates directly from a 3.58MHz TV crystal. Direct drive of LED display	3-34

CALCULATOR MODULES — Sec. 2

FUNCTION	DESCRIPTION (SEE ABOVE)	PART NUMBER	FEATURES	PAGE NO.
8 DIGIT CALCULATOR	Same as C-683D	M-683	Self-contained module which requires only the addition of a keyboard and battery to produce a working calculator.	2-8
	Same as C-685D	M-685		2-8
	Same as C-687D	M-687		2-8
	Same as C-689D	M-689		2-8

CLOCK MODULES — Sec. 3

FUNCTION	DESCRIPTION (SEE ABOVE)	PART NUMBER	FEATURES	PAGE NO.
4 DIGIT CLOCK	Same as CK3400	M-3400	Self-contained module which requires only the addition of switches and a power source to produce a working clock	3-18
4 DIGIT CLOCK RADIO	Same as CK3300	M-3300		3-32
4 DIGIT AUTO CLOCK	Same as CK3500	M-3500		3-36

RADIO — Section 4A

FUNCTION	DESCRIPTION	PART NUMBER	AM/MW/SW IF OFFSET	FM/VHF IF OFFSET	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
FREQUENCY COUNTER/ DISPLAY	Counts & displays MW, SW, and VHF frequencies	AY-5-8100	450KHz	10.7MHz	GND -17	28 DIP	4½ digit display. MW 2999KHz, SW 29.995MHz, VHF 299.99MHz, 0 to 99 FM channel indication (European standard).	4A-1
		AY-5-8102	455KHz					4A-2
FREQUENCY COUNTER/DISPLAY WITH 4 DIGIT CLOCK	Counts & displays AM/FM frequencies with a 12 hour clock	AY-3-8110	262.5KHz	PROGRAM-MABLE	+10 to +16, GND	28 DIP	Easy time set controls, low power consumption, on-chip intensity control. Clock functions down to +5V	4A-5
		AY-3-8112	455KHz					4A-6

TELEVISION — Section 4A

FUNCTION	DESCRIPTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
OMEGA®: 82 CHANNEL DIGITAL TUNING SYSTEM	Control circuit: accepts keyboard/remote inputs to control and program system	T-1001	+12, GND	40 DIP	Scan mode or search mode may also be selected	4A-10
	Display circuit: displays selected channel number	T-1101	+12, GND	40 DIP	Decodes and drives BCD or LED displays	4A-10
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	VREF +12, GND	14 DIP	14 bit accuracy for precise varactor tuning	4A-14
	Memory circuit, see ER 1400 EAROM description on Pg. 9	ER 1400	-12, -24	8 TO	100 × 14 bit memory	4A-17
	Optional channel selector interface circuit: permits preset favorite channel selection.	T-1201	+12, GND	40 DIP	Up to 20 channels pre-set and/or customer selection	4A-12
ECONOMEGA® I: 16 CHANNEL DIGITAL TUNING SYSTEM	Control circuit accepts direct/remote inputs to control/program system	AY-3-8203	+12, GND	40 DIP	16 programs, 14 bit accuracy with coarse and fine tune	4A-20
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	VREF +12, GND	14 DIP	14 bit accuracy for precise varactor tuning	4A-14
	Memory circuit, see ER 1400 EAROM description on Pg. 9	ER 1400	-12, -24	8 TO	100 × 14 bit memory	4A-17
ECONOMEGA® II: 20 CHANNEL DIGITAL TUNING SYSTEM	Control/memory circuit: accepts direct/remote inputs to control/program system.	AY-5-8290	+17 GND, -20	40 DIP	Contains both control logic and EAROM memory in a single chip, 20 programs	4A-24
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	VREF +12, GND	14 DIP	14 bit accuracy for precise varactor tuning	4A-14
ON-SCREEN CHANNEL/TIME DISPLAY SERIES	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display. Selection of display position on screen, automatic display recall BCD time inputs (see AY-5-1203A clock circuit)	AY-5-8300	+17 GND	14 DIP	Channels 0-15	4A-26
		AY-5-8301			Channels 1-16	4A-28
		AY-5-8310		24 DIP	Channels 0-15 or 00-99 or time	4A-26
		AY-5-8311	+12, GND			4A-28
		AY-5-8320	-17, GND		Channels 1-16 and/or time Upper right screen display	4A-28
		AY-5-8321	+12, GND			4A-29
		AY-5-8322	-13, GND		Channels 1-16 and/or time Lower center screen display	4A-28
		AY-5-8324	+13, GND			4A-28
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor tuned TV sets	AY-3-8330	+12, GND	16 DIP	4 bands, mask programmable band or channel number display, mask programmable display positions	4A-36

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REMOTE CONTROL — Section 4A

FUNCTION	DESCRIPTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
R/C SYSTEM I	30 Channel Transmitter	SAA 1024	9V BATTERY	16 DIP	30 ultrasonic control channels, 34-44KHz. Utilizes a 4.4MHz TV crystal for accuracy	4A-38
	30 Channel Receivers	SAA 1025-01	+16, GND	16 DIP	Power on/off output, 16 TV channel selection (& 5 spares), 3 analog outputs (8 functions)	4A-40
		SAA 1025-02				4A-40
R/C SYSTEM II	23 Channel Transmitters	AY-5-8410	+15, GND	18 DIP	23 channels, either local control at receiver or remote control,	4A-44
		AY-5-8411	9V BATTERY			4A-44
	31/63 Channel Receiver	AY-5-8420	+15, GND	14 DIP	5 or 6 bit modes, error-detection	4A-46
R/C SYSTEM III	30 Channel Transmitter	AY-5-8450	9V BATTERY	16 DIP	30 ultrasonic control frequencies, Interfaces directly with a 5×8 matrix keyboard	4A-48
	16 Channel Receivers	AY-5-8460	+12, GND, -6	18 DIP	Interfaces directly with OMEGA 10 digit keyboard inputs plus on/off, recall, 2 analog controls (4 functions)	4A-50
		AY-5-8461				4A-50

GIMINI TV GAMES — Section 4B

The General Instrument game repertoire offers game manufacturers a choice of approaches to the marketplace. GIMINI dedicated game chips and the GIMINI cassette programmable game set.

The dedicated game chips for 1977 include a choice of Ball and Paddle games with true game rules, realistic courts, and individual player identification. The Battle game offers all the thrills and excitement of its popular arcade big brother.

The programmable game set based on a variant of GI's CP1600, an advanced 16-bit single chip microprocessor, provides maximum flexibility in implementing a programmable system. The game "program" ROM, which can be incorporated in a cassette, connects directly to the system address and data busses. With this ROM/cassette approach, a library of game ROMs can be developed encompassing a multitude of game families.

Additionally, since the heart of the programmable system is based on the powerful 16-bit CP1600 microprocessor, expanded capabilities beyond a "game" function are possible — including home interactive teaching systems, data storage and retrieval systems ..in effect, a true "home computer."

DEDICATED TV GAMES — Section 4B

FUNCTION	DESCRIPTION	GAMES	PART NUMBER	LINE STANDARD	PACKAGE	FEATURES	PAGE NO.
BALL & PADDLE I	Six selectable games for one or two players, with vertical paddle motion.	Tennis Soccer Squash Practice Rifle Game I Rifle Game II	AY-3-8500	525	28 DIP	Automatic on-screen scoring. Sound generation (hit, boundary, score) Selectable paddle size, ball speed, rebound angles	4B-2
			AY-3-8500-1	525			4B-2
BALL & PADDLE IA	Six selectable games for one or two players, with horizontal and vertical paddle motion.	Tennis Soccer Squash Practice Rifle Game I Rifle Game II	AY-3-8550	525	28 DIP	All features of the AY-3-8500/8500-1 with the addition of full two-axis player motion, color-coding of score and player, and "hit" and "miss" scoring in Practice game	4B-14
			AY-3-8550-1	525			4B-14
COLOR CONVERTER I	Converts the black & white video outputs of either the AY-3-8500-1 or AY-3-8550-1 to a single color composite video signal	--	AY-3-8515-1	525	16 DIP	Colors of the background and paddle outputs are selectively changed directly by the "game select" inputs Also provides, as an output, a 2.045MHz clock for the game circuit	4B-23
BALL & PADDLE II	Eight selectable games for one or two players, with horizontal and vertical player motion	Tennis Hockey Soccer Squash Practice Gnoball Basketball Basketball Practice	AY-3-8600	525	28 DIP	Automatic on-screen scoring. Sound generation (hit, boundary, score) Selectable paddle size, (individually selectable for each player) ball speed, rebound angles. Full two-axis player motion. Color-coding of score and player. Realistic ball service and scoring. Flashing score as "end of game" indication	4B-24
			AY-3-8600-1	525			4B-24
COLOR CONVERTER II	Converts to the black & white video outputs of the AY-3-8600-1 to a single color composite video signal	--	AY-3-8615-1	525	28 DIP	Colors of the background and paddle outputs are selectively changed directly by the "game select" inputs Also provides, as an output, a buffered 3.579MHz clock for the game circuit	4B-33
BATTLE I	A two player "tank battle game where each player has a completely steerable tank with forward and reverse speed control and a firing button	Tank Battle	AY-3-8700	525	28 DIP	The on-screen "battlefield" includes anti-tank barricades and exploding mines to retard each tank's progress Unlimited ammunition to a scoring limit of 31 "hits."	4B-34
			AY-3-8700-1	525			4B-34

CASSETTE PROGRAMMABLE TV GAMES — Section 4B

FUNCTION	DESCRIPTION	GAMES	PART NUMBER	PACKAGE	FEATURES	PAGE NO.
GIMINI* PROGRAMMABLE GAME SET	The GIMINI chip set provides the basis for a user-programmed game series for up to eight players and featuring: up to eight user-controlled moving objects, 64 selectable moving objects, up to 240 programmable background locations, movable background field, and display in up to six colors plus black and white.	User game design for such as: Ball & Paddle, Aggression, Gambling, Racing, etc	CP1610	40 DIP	A variant of the GI CP1600 microprocessor, the CP1610 is 16-bit unit utilizing 8 general purpose registers for fast and efficient processing of all game data.	4B-38
			RO-3-2048G	40 DIP	The "program" ROM organized as 2048 × 10, contains all game "rules", symbol locations, color, velocity and direction data	4B-38
			AY-3-8900	40 DIP	The "STIC", Standard Interface Chip, provides the video signals including sync and blanking and the manipulation and interaction of all graphics data in a non-interlaced pattern for the TV.	4B-38
			AY-3-8900-1			4B-38
			RO-3-9316A	24 DIP	The "graphics" ROM organized as 2048 × 8, contains a series of 8 × 8 dot matrices for a large variety of game symbols, background/field data, and 64 alpha-numeric characters.	4B-38
			RAM	--	The "working" memory during game operation. A total of five 256 × 4 RAMs are required for a combined 256 × 12 and 256 × 8 memory complement	4B-38

*GIMINI is a trademark of General Instrument Corp

MOSFET TRANSISTORS — Section 4C

TYPE	PART NUMBER	V(BR)DSS VOLTS MIN.	V(BR)GSS VOLTS MIN.	IDSS nA TYP.	IGSSF nA TYP.	VGS(th) VOLTS MIN/MAX.	rDS(on) OHMS TYP.	Yfs MHO TYP.	Ciss pF TYP.	Crss pF TYP.	CASE	PAGE NO.
P-CHANNEL ENHANCEMENT MODE	MEM805	-40	-40	-1.0	-0.1pA	+2/-5.5	150	2,500	4.5	1.0	TO-72	4C-2
	MEM807	-40	-40	-0.5	-0.1	+2/-5.5	150	2,800	4.5	1.0	TO-72	4C-4
	MEM817	-45	±200	-0.1	-0.05pA	-2.5/-6.5	150	2,000	3.5	1.2	TO-72	4C-6
	3N183	-25	-25	-2.0	-0.3	-2/-6	50	9,000	15.0	10.0	TO-72	4C-7

TYPE	PART NUMBER	V(BR)DSS VOLTS MIN.	IGSSF nA TYP.	VGS(th) VOLTS MIN/MAX.	rDS(on) OHMS TYP.	Yfs MHO TYP.	Ciss pF TYP.	Crss pF TYP.	Yfs RATIO TYP.	|VG1S-VG2S| mV TYP.	CASE	PAGE NO.
DUAL P-CHANNEL ENHANCEMENT MODE	MEM550C	-25	-0.2	-3/-6	250	600	2.0	0.8	0.8	100	TO-77	4C-10
	MEM551C	-25	-1pA	-3/-6	250	750	1.5	1.5	0.95	75	TO-77	4C-10
	MEM954	-30	-0.03	-2/-5	100	1000	2.0	1.5	0.95	50	TO-77	4C-12
	MEM955	-35	-0.02pA	-2/-5	100	1000	2.0	1.5	0.95	50	TO-77	4C-12

TYPE	PART NUMBER	BVDSS MIN. VOLTS	V(BR)GSS VOLTS MIN.	IDSS nA TYP.	IGSSF nA TYP.	ID(on) mA TYP.	VGS(on) VOLTS MIN/MAX.	rDS(on) OHMS TYP.	Yfs MHO TYP.	Ciss pF TYP.	Crss pF TYP.	CASE	PAGE NO.
N-CHANNEL ENHANCEMENT MODE	MEM582	+20	+30	1	1pA	15	0.5/4	150	2,500	3	0.3	TO-72	4C-14
	MEM711	+25	+30	1	0.1	40	0.5/1.5	50	3,000	4.5	0.5	TO-72	4C-16
	3N177	+20	+30	5	50pA	15	1/3.5	300	1,500	5	0.5	TO-72	4C-18

TYPE	PART NUMBER	V(BR)DS VOLTS MIN.	V(BR)GSS VOLTS MIN.	V(BR)GSS VOLTS MIN	IDSS mA TYP.	IGSS nA TYP.	VGS(off) VOLTS MAX.	rDS(on) OHMS TYP	Yfs MHO TYP.	Ciss pF TYP.	Crss pF TYP.	GPS dB TYP.	NF dB TYP.	CASE	PAGE NO.
N-CHANNEL DEPLETION MODE	MEM557	+20	-10	--	5	.01	-4	200	10,000	3	0.32	18	2.5	TO-72	4C-22
	MEM616	+25	-6	±6	10	20	-4	--	18,000	5.4	.02	18	3.0	TO-72	4C-24
	MEM836	+20	-6	±6	15	50	-4	--	16,000	6	.02	22	3.5	Plastic	4C-28
	MEM855	+20	-6	--	4	10	-4	30	10,000	4	0.32	22	2.5	TO-72	4C-32
	MEM670	+20	-100	--	3	.05pA	-4	--	2,000	2	0.3	--	--	TO-72	4C-34
	MEM680	+25	-6	--	4/30	50	-4	--	16,000	5.4	0.2	21	2.5	TO-72	4C-36

MUSIC — Section 5

FUNCTION	DESCRIPTION	PART NUMBER	MAXIMUM FREQUENCY	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
MASTER FREQUENCY GENERATOR/ TOP OCTAVE GENERATOR	Generates a complete octave of musical frequencies	AY-1-0212	1.5 MHz	+12, GND	16 DIP	250KHz minimum frequency	5-3
		AY-1-0212A	2.5 MHz				5-3
		AY-3-0214	4.5MHz	+10 to +16, GND	16 DIP	12 outputs, 50% duty cycle	5-6
		AY-3-0215				13 outputs, 50% duty cycle	5-6
		AY-3-0216				13 outputs, 30% duty cycle	5-6
LATCHING NETWORK	Establishes priority level of 13 latch inputs/outputs	AY-1-1313	20KHz	GND, -12, -27	40 DIP	Stackable for expanded latching/ priority function	5-8
RHYTHM GENERATOR	Generates 5 rhythms, drives 8 instruments	AY-5-1315	10KHz	GND, -15	18 DIP	Resets for coupling chords to rhythm; 32 beat pattern. Mask programmable.	5-10
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass	AY-5-1317A	50KHz	GND, -15	40 DIP	Mixed outputs, sustain, top key priority	5-12
PIANO KEYBOARD	Electronically simulates piano operation and sound	AY-1-1320	--	GND, -10, -27	40 DIP	12 keys per unit, loudness proportional to key press velocity	5-16
FREQUENCY DIVIDERS	4 stage	AY-1-8051	1MHz	GND, -13, -27	10 TO	Arranged 2 + 1 + 1	5-20
	5 stage	AY-1-8721/5	1MHz	GND, -13, -27	10 TO	Arranged 3 + 2	5-20
	6 stage	AY-1-8721/6	1MHz	GND, -13, -27	12 TO	Arranged 3 + 2 + 1	5-20
		AY-1-1006	50KHz	GND, -12, -27	14 DIP	Arranged 3 + 2 + 1	5-22
		AY-1-2006	50KHz	GND, -12, -27	14 DIP	Arranged 2 + 2 + 1 + 1	5-22
	7 stage	AY-1-5050	1MHz	GND, -13, -27	14 DIP	Arranged 3 + 2 + 1 + 1	5-20
		AY-1-1007B	50KHz	GND, -12, -27	14 DIP	Arranged 3 + 2 + 1 + 1, power-on reset	5-24
	2^{n} FL Counter/Divider	AY-9-1000	Operation is a function of current through a resistor from V_{CC} to Injection input		8 TO, 16 DIP	Crystal/RC oscillator input, divide by 2^{10}, 2^{11}, 2^{12}, 2^{13}, or 2^{14}.	5-26

APPLIANCES / SECURITY — Section 6

FUNCTION	DESCRIPTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
CLOCK TIMER	24 hour programmable repeatable on/off time switch with 4 digit clock	AY-5-1230	GND, -12 to -18	28 DIP	50Hz input (50 or 60Hz on AY-5-1231), BCD or 7-segment direct fluorescent display drive outputs, zero blanking, 24 hour display (12 or 24 hour on AY-5-1231)	6-2
		AY-5-1231		40 DIP		6-2
		AY-5-1232		28 DIP		6-2
		AY-5-1233		28 DIP		6-2
COOKER TIMER	Appliance timer with clock Full control of "start" time, "stop" time, or "duration"	AY-5-1250	+9, GND	28 DIP	Two timed outputs (3 on the AY-5-1251) "minute minder" feature, 12/24 hour system temperature setting on AY-5-1251	6-6
		AY-5-1251				6-6
COINBOX CIRCUIT	A coin memory/credit accumulator for use in coin-operated equipment	AY-1-8622	GND, -12, -27	40 DIP	Seven different coin inputs, credit and "bonus" features.	6-10
IONIZATION SMOKE DETECTOR	Complete ionization smoke detector circuitry in a single CMOS LSI	MEM4962	+9, GND	14 DIP	On-chip input MOSFET and output driver Low battery warning.	6-15

TELECOMMUNICATIONS — Section 7A

FUNCTION	DESCRIPTION	PART NUMBER	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
PUSH BUTTON TELEPHONE DIALLER CIRCUIT	Converts push button input to rotary dial pulses	AY-5-9100	SEE DATA SHEET	16 DIP	Programmable timing, one-call memory. Optional redial and access pause capability (except on AY-5-9119)	7A-2
		AY-5-9106				7A-2
		AY-5-9110				7A-2
		AY-5-9118		14 DIP		7A-2
		AY-5-9120		18 DIP		7A-2
REPERTORY DIALLER	Stores ten telephone numbers	AY-5-9200	SEE DATA SHEET	16 DIP	Complements AY-5-9100 to enable storage of up to ten 22-digit telephone numbers. Stackable	7A-9
COINBOX CIRCUIT	Controls the operation of a standard pay telephone.	AY-5-9300	SEE DATA SHEET	24 DIP	Up to 3 coin denominations recognized, 16 selectable coin ratios	7A-15
DUAL TONE MULTI-FREQUENCY GENERATOR	Generates DTMF/tone telephone frequencies.	AY-3-9400	+5, GND	14 DIP	With a low cost ceramic resonator, generates 12 tone pairs	7A-16
		AY-3-9401	+5, GND	16 DIP	Same as AY-3-9400 but generates 16 tone pairs for data transmission.	7A-16
		AY-3-9410				7A-16
CMOS CLOCK GENERATOR	Generates 2-phase clocks from a single power supply	AY-5-9500	SEE DATA SHEET	14 DIP	Generates 2-phase clocks for AY-5-9100 & AY-5-9200	7A-19
MULTI-FREQUENCY RECEIVER	Detects and converts DTMF/tone telephone frequencies	AY-5-9800 SERIES	GND, -8.5, -17	28/40 DIP	Choice of output codes: 4 bit, 1 of 16, 2 of 8, binary. custom programmable	7A-22

HYBRID ACTIVE FILTERS — Section 7B

FUNCTION	PART NUMBER	DESCRIPTION	PAGE NO.
UNIVERSAL ACTIVE FILTER	ACF 7092C ACF 7092C	The ACF 7092C and the ACF 7092C filters are low cost devices which can be used to generate any filter response. Low pass, Band pass, Band Rejection, High pass, and All pass filter responses are available by means of external connections. The design provides for independent control of Frequency, Q, and Amplifier Gain, and is usable throughout the frequency range of 10Hz to 10KHz.	7B-2
3825Hz LPF	ACF 7110C	The ACF 7110C filter provides for low pass filtering of speech frequencies while attenuating the 3825Hz signaling frequency to a minimum attenuation of 42dB. The reference 1.0KHz gain of this filter is 0dB with a maximum in-band ripple specification plus or minus 0.1dB.	7B-6
PCM TRANSMIT LPF	ACF 7170C	The ACF 7170C filter has been designed for PCM transmit applications. This 0dB gain filter provides for a minimum 39dB attenuation at 4.6KHz and an in-band ripple specification of plus or minus 0.125dB	7B-6
PCM TRUNK TRANSMIT LPF	ACF 7173C	The ACF 7173C filter has been designed for PCM "Trunk" transmit applications. This variable gain, 0dB to 29dB, low noise filter is capable of exceeding the A.T. & T. D3 Channel Bank Compatibility specification. This filter provides a minimum attenuation of 32dB at 4.6KHz, a maximum in-band ripple of plus or minus 0.1dB, and 14.5dB minimum attenuation at 60Hz	7B-10
PCM TRUNK RECEIVE LPF & PAM GATE	ACF 7174C	The ACF 7174C filter has been designed for PCM "Trunk" receive applications. This variable gain, -18dB to +3.5dB, low noise filter is capable of exceeding the A.T.&T. D3 Channel Bank Compatibility specification. This filter has a self contained Pulse Amplitude Modulation (PAM) Gate and Sample and Hold Capacitor for demodulating and holding the input signal. The filter has been compensated for a Sin X over X correction and provides a minimum attenuation of 28dB at 4.6KHz and a maximum in band ripple of plus or minus 0.1dB.	7B-11
PCM LINE TRANSMIT LPF	ACF 7175C	The ACF 7175C filter has been designed for PCM "Line" transmit applications. This fixed gain, 6.26dB, low noise filter is capable of exceeding the A.T.&T. D3 Channel Bank Compatibility specification. This filter provides a minimum attenuation of 30dB at 4.6K-Hz and a maximum in band ripple of plus or minus 0.3dB and also provides for DC blocking	7B-13
PCM LINE RECEIVE LPF & PAM GATE	ACF 7176C	The ACF 7176C filter has been designed for PCM "Line" receive applications. This fixed gain, 8.2dB, low noise filter is capable of exceeding the A.T.&T. D3 Channel Bank Compatibility specification. This filter has a self contained Pulse Amplitude Modulation (PAM) Gate and Sample and Hold Capacitor for demodulating and holding the input signal. The filter has been compensated for a Sin X over X correction and provides a minimum attenuation of 26dB at 4.6KHz, and a maximum in band ripple of plus or minus 0.3dB	7B-14
DPF & FULL WAVE DETECTOR	ACF 7300C ACF 7301C ACF 7302C	The ACF 7300C/7301C/7302C each consists of a full wave detector and a four (4) pole fixed band width band pass filter factory tunable over a center frequency (Fo) range: ACF 7300C - 540Hz to 1980Hz. ACF 7301C - 700Hz to 1700Hz: ACF 7302C - 2280Hz to 3825Hz	7B-16 7B-18 7B-20
2600Hz BPF	ACF 7310C	The ACF 7310C is a sharply tuned filter designed to detect and pass the 2600Hz signaling frequency. This filter provides for a minimum attenuation of 30dB plus and minus 200Hz, 50dB plus and minus 500Hz, and 70dB plus and minus 1000Hz from the center frequency of 2600Hz.	7B-22
3825Hz BPF	ACF 7311C	The ACF 7311C is a sharply tuned filter designed to detect and pass the 3825Hz signaling frequency. This filter provides for a minimum attenuation of 40dB, plus and minus 200Hz from the center frequency of 3825Hz	7B-24
300-3400Hz BPF	ACF 7320C	The ACF 7320C is a 0dB, 300Hz to 3400Hz band pass filter with an in band ripple specification of plus or minus 0.15dB maximum. The filter provides for a minimum attenuation of 15dB at 170Hz and 3750Hz.	7B-25
DTMF TONE DETECTION BPF	ACF 7323C ACF 7363C ACF 7383C	The ACF 7323C/ACF 7363C/ACF 7383C Banc Pass Active Filters are factory pre-tuned filters designed specifically for tone receiver applications. These two pole constant Q filters are available in the standard AT&T tone frequencies and in the standard multifrequency steps	7B-26
DIAL TONE BAND SUPPRESSION FILTER	ACF 7401C	The ACF 7401C is a dual tuned band suppression filter which has been designed to reject frequencies of 350Hz and 440Hz, which are present on a telephone line. The unit is totally self contained and requires no external components for proper operation. The filter provides for 0dB insertion loss in the pass band of 697Hz through 1633Hz, the normal DTMF tone frequencies. The filter also provides for 50Hz attenuation for low noise operation	7B-28
2600Hz BAND SUPPRESSION FILTER	ACF 7410C	The ACF 7410C is a sharply tuned filter designed to reject the 2600Hz signaling frequency. This filter provides for a minimum attenuation of 60dB plus and minus 15Hz from the center frequency of 2600Hz	7B-29
60Hz NOISE SUPPRESSION FILTER	ACF 7480C	The ACF 7480C is a sharply tuned filter for 60 Hertz suppression. It provides a minimum attenuation of 40dB plus or minus 0.25Hz from the center frequency. The filter is self contained and requires no external components for proper operation.	7B-30
DTMF BAND SEPARATION FILTER	ACF 7711C	The ACF 7711C is a dual filter which has been designed to provide channel isolation between the low frequency group of the tone (DTMF) frequencies of 941Hz, and the high frequency group of 1209Hz through 1633Hz. This filter provides for a minimum attenuation of 30dB for the adjacent frequencies of 941Hz and 1209Hz, 0dB in the pass bands, and 25dB out-of-band attenuation.	7B-31

DATA COMMUNICATIONS — Section 8A

FUNCTION	DESCRIPTION	PART NUMBER	REPLACES (PIN-FOR-PIN)	BAUD RANGE	MAX. FREQ.	TEMP. RANGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
UAR/T®	Complete 5-8 bit serial/ parallel, parallel/serial interface.	AY-3-1015	AMI S1757 SIG 2536 SMC COM2505 TI TMS6011 WD TR1402A WD TR1602A	0 to 30KB	480KHz	0 to 70	+5, GND	40 DIP	1, 1.5, or 2 stop bits	8A-2
		†AY-5-1013		0 to 22.5KB	360KHz	-55 to +125	+5, GND, -12	40 DIP	1 or 2 stop bits	8A-2
		AY-5-1013A		0 to 40KB	640KHz	0 to 70				8A-2
		AY-3-1014A		0 to 30KB	480KHz	0 to 70	+5 to +14, GND	40 DIP	1, 1.5, or 2 stop bits	8A-2
P/SAR	A programmable receiver that interfaces variable length serial data to a parallel data channel.	AY-8-1472B	WD1472B	0 to 100KB	100KHz	0 to 70	+5, GND, -12	40 DIP	Data conversion to formats compatible with all standard Synchronous, Asynchronous, & Isochronous data communications media	8A-16
P/SAT	A programmable transmitter that interfaces variable length parallel data to a serial data channel.	AY-8-1482B	WD1482B	0 to 100KB	100KHz	0 to 70	+5, GND, -12	40 DIP		8A-17

†Also available with MIL STD 883 screening (add suffix TX to part number).
®UAR/T is a trademark of General Instrument Corporation.

MULTIPLEXERS — Section 8B

FUNCTION	DESCRIPTION	PART NUMBER	PEAK-PEAK SIGNAL INPUT RANGE	ON RESISTANCE	TEMP. RANGE	SUFFIX/ PACKAGE	PAGE NO.
RANDOM/ SEQUENTIAL ACCESS MULTIPLEXER	Multiplexes 16 analog channels, with on-chip logic control.	AY-5-1016	20 Volts	800 ohms	0 to 70	40 DIP	8B-2
		†AY-5-4016			-55 to +125		8B-2
MOSFET ANALOG GATES	4 CHANNEL	MEM 851	30 Volts	100 ohms	-55 to +85 (Plastic Dip) -55 to +125 (Ceramic DIP, Flat Pack)	P/14 Plastic DIP D/14 Ceramic DIP F/14 Flat Pack	8B-6
	6 CHANNEL	MEM 855	25 Volts	350 ohms			8B-10
		MEM 856	40 Volts	1000 ohms			8B-12
	8 CHANNEL	MEM 857	25 Volts	150 ohms		P/24 Plastic DIP D/24 Ceramic DIP F/24 Flat Pack	8B-14
	10 CHANNEL	MEM 853	25 Volts	150 ohms			8B-16

†Also available with MIL STD 883 screening (add suffix TX to part number).

INDUSTRIAL — Section 9

FUNCTION	DESCRIPTION	PART NUMBER	MAX. COUNT FREQUENCY	OUTPUT CURRENT	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
4 DIGIT COUNTER	Counts, stores & decodes four decades to BCD outputs.	AY-5-4057	500KHz	—	+5, GND, -12	18 DIP	BCD outputs	9-3
4 DIGIT COUNTER/ DISPLAY DRIVER	Counts (up or down), stores & decodes four decades to 7-segment outputs	AY-5-4007	600KHz	25 mA/V	+5, GND, -12	24 DIP	BCD outputs true/ complement control	9-5
		AY-5-4007A				40 DIP	Includes features of AY-5-4007 & 4007D	9-5
		AY-5-4007D				24 DIP	Serial count output, three carry outputs	9-5
3½ DIGIT DVM	DVM logic incorporating dual ramp integration	AY-5-3507	40KHz	6 mA	GND, -15	18 DIP	Range to 1999, 7-seg. outputs	9-12
		AY-5-3510		—		16 DIP	Range to 1999, BCD outputs	9-12
3¾ DIGIT DVM	DVM logic incorporating dual ramp integration	AY-5-3500	200KHz	6 mA	GND, -7.5, -15	28 DIP	3 ranges: 999, 1999, 2999. Dual polarity, BCD & 7-seg. outputs	9-17
4½ DIGIT DVM	DVM logic incorporating dual ramp integration	AY-3-3550	400KHz	2.5 mA	+5, GND	40 DIP	Auto-range, auto-zero, auto-polarity, 7-segment/ BCD outputs, counter mode	9-22
10 BIT D/A CONVERTOR	Ladderless D/A converter	AY-5-5063	SEE DATA SHEET	—	+5, GND, -12	24 DIP	Employs stochastic techniques	9-27
A/D CONVERTOR CONTROL	With AY-5-5353, performs A/D with transmitter facility	AY-5-5054	SEE DATA SHEET	—	+5, GND, -12	24 DIP	For use in remote sensing applications	9-32
SEQUENTIAL BOOLEAN ANALYZER	A simple, single bit processor which can directly evaluate a set of Boolean equations	SBA	600KHz CLOCK	20 mA TOTAL	+12, +5, GND	40 DIP	A microprogrammable circuit which forms the basic controlling element for many systems requiring timing and control functions.	9-36

SERIES 1600 MICROPROCESSOR — Section 10A

FUNCTION	FEATURES	DESCRIPTION	APPLICATIONS	PART NUMBER	PACKAGE	PAGE NO.
16 BIT SINGLE CHIP MICRO-PROCESSOR	■ 8 program accessible 16-bit general purpose registers ■ 87 basic instructions ■ 4 addressing modes ■ Unlimited interrupt nesting and priority resolution ■ 16-bit 2's complement arithmetic & logic ■ Direct memory access (DMA) for high speed data transfer ■ 64K memory using single address	The CP 1600 utilizes third generation mini-computer architecture with eight general purpose registers. The 16-bit word enables fast & efficient processing of alpha-numeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices	The CP 1600 Microprocessor is designed for high speed data processing & real time applications. Typical applications include programmable calculator systems, peripheral controllers, process controllers, intelligent terminals & instruments, data acquisition and digital communications processors, numerical control systems, programmable TV game systems	CP 1600	40 DIP	10A-2
INPUT/ OUTPUT BUFFER	■ Single 16-Bit or Dual 8-Bit Ports for Bidirectional Input/Output ■ Parity Check Logic on Both Ports ■ Three Levels of Priority ■ Automatic Handshake Logic and Signals ■ Control Register	The IOB 1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing feaiures for the CP 1600 microprocessor. Data is transferred to and from the peripheral on 16 bidirectional lines, each of which can be considered to be an input or output	The IOB 1680 enables efficient interfacing between a peripheral and the CP 1600 by the use of six 8-bit registers and a 16-bit programmable timer.	IOB 1680	40 DIP	10A-8
DUAL DIGITAL TO ANALOG CONVERTER	■ 10 bit bidirectional data bus ■ Synchronous/Asynchronous loading ■ Manual input mode	The DAC 1600 contains four registers which can be loaded or read through a 10-bit I/O data port	The DAC 1600 Digital to Analog Converter has been designed to interface to a process control loop	DAC 1600	40 DIP	10A-14
16 CHANNEL ANALOG MULTIPLEXER	■ Connects 1 of 16 analog inputs ■ Address latch on-chip ■ 0 to 6 volt input range ■ Analog output controlled by chip select signal	The MUX 1600 is a binary addressed 16 channel analog multiplexer. The MUX 1600 includes on-chip address latches and separate address strobe and chip select signals	The binary address selection of the 16 input channels provides for simplified direct control of analog signals by the CP1600 microprocessor chip	MUX 1600	36 DIP	10A-18
GIMINI MICRO-COMPUTER SYSTEM	■ Built around the CP 1600 Microprocessor ■ Complete microcomputer system ■ Separate Data, Address and Control Buses ■ Up to 65K memory space ■ Unlimited DMA channels ■ Nested interrupt system with full priority resolution	The GIMINI utilizes a totally modular design for maximum configurability. The system provides direct addressing to 65K words, unlimited DMA channels, and a multi-line multi-level nested interrupt system with full priority resolution and self-identifying addresses. All control & timing signals as well as data & address busses are fully buffered	To simplify microprocessor hardware and software development, speed the product design cycle & support product prototyping, a microcomputer development system and its associated components are a must. The Series 1600 family fills these requirements with the GIMINI Microcomputer	GIMINI	--	10A-20
GIMINI SINGLE CARD MICRO-COMPUTER	■ 16K words of RAM ■ 4K words of PROM ■ Up to 32 Input and 32 output lines ■ Two UART-RS232 Serial I/O channels ■ Real time clock	The SC1600 GIMINI Single Card Microcomputer provides full 16-bit processing power on a single card. The SC1600 uses the CP1600 microprocessor with all circuitry for a complete operating system	In industrial usage, the SC1600 can serve as the kernel of a modular expandable processing system with other cards added as required. In consumer applications, the SC1600 can serve as the basis for many user-programmable systems such as TV games, home TV terminals, etc.	SC1600	--	10A-23

SERIES 8000 MICROPROCESSOR — Section 10B

FUNCTION	FEATURES	DESCRIPTION	APPLICATIONS	PART NUMBER	PACKAGE	PAGE NO.
8 BIT MICRO-PROCESSOR	■ 2 Chip Minimum System (plus clock) ■ 46 Accessible 8 Bit Registers ■ 48 Basic Instructions ■ Binary and Decimal Arithmetic ■ Direct and Indirect Input/ Output Capability ■ Automatic subroutine nesting on memory devices	The LP 8000 Logic Processor Unit is a complete 8-bit single chip MOS-LSI Microprocessor. It has a modern computer architecture with forty eight general purpose internal registers. The 8-bit Data highway is supplemented by a 6-bit Address bus to give a 14-bit address capability which permits access to 16,384 words	The Series 8000 Logic Processor System is designed to perform any digital function using far fewer packages than a TTL or CMOS implementation. Typically a 100 package system can be reduced to a three chip solution or LP 8000 Processor, LP 8000 Program Memory and LP 1030 Clock Generator. Also available LP 1010 I/O Buffer, LP 1005 Memory Interface	LP 8000	40 DIP	10B-2
				LP 6000	40 DIP	10B-2
				LP 1030	8 DIP	10B-2
				LP 1010	40 DIP	10B-2
				LP 1005	40 DIP	10B-2

PIC SERIES MICROCOMPUTER — Section 10C

FUNCTION	FEATURES	DESCRIPTION	APPLICATIONS	PART NUMBER	PACKAGE	PAGE NO.
8 BIT SINGLE CHIP MICRO-COMPUTER	■ User Programmable ■ 32 8-Bit Registers ■ 512x12-Bit ROM for Program ■ Arithmetic Logic Unit ■ 4 Sets of 8 User Defined TTL-compatible Input/Output Lines ■ Real Time Clock Counter ■ Self contained Oscillator ■ Access to RAM Registers inherent in instruction	The PIC 1650 MOS/LSI circuit array is a byte oriented programmable controller. The array is a complete chip controller with an internal customer-defined ROM program specifying the overall functional characteristics and operational waveforms on each of the general purpose input/ output lines	The array can be programmed to scan keyboards, drive multiplexed displays, control vending machines, traffic lights, printers and automatic gasoline pumps. Since it contains ROM, RAM I/O as well as the central processing unit on one device, the PIC 1650 is truly a complete 8-bit microcomputer on one chip	PIC 1650	40 DIP	10C-2
8 BIT SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	■ PIC 1650 microcomputer without ROM ■ ROM address and data lines brought out to pins ■ Can be stopped or single stepped via a HALT pin	The PIC 1664 circuit is exactly the same as the PIC 1650 except that the ROM portion of the PIC 1650 has been removed. Any external RAM or PROM can be used to aid in the development of a final PIC 1650 configuration	The PIC 1664 has been designed as a useful tool for engineering development and prototyping and for initial field trial and demonstrations of systems which will utilize the PIC 1650	PIC 1664	64 DIP	10C-10

STATIC RANDOM ACCESS MEMORIES — Section 11

BITS	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME/ CYCLE TIME	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
1024	256x4	RA-3-4256	--	500ns/500ns	+5, GND	24 DIP	Power down mode	11-2
		RA-3-4258A	--	650ns/650ns	+5, GND	24 DIP	Power down mode	11-2
		RA-3-4258B	--	650ns/650ns	+5, GND	22 DIP		11-2
4096	4096x1	RA-3-4200	SEMI 4200	215ns/400ns	+12, -5, GND	22 DIP	TTL output	11-8
		RA-3-4402	SEMI 4402	200ns/350ns	+12, GND, -5	22 DIP	Differential output.	11-10

ELECTRICALLY ALTERABLE READ ONLY MEMORIES — Section 12

BITS	MEMORY ORGANIZATION	PART NUMBER	READ ACCESS	ERASE TIME/MODE	WRITE TIME/MODE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
512	32 x 16	ER2050	10 µs	100ms/16 bit word	10ms/16 bit word	+5, -26	28 DIP	10 year data storage @ +70°C	12-2
		ER2051	3 µs	50ms/16 bit word	50ms/16 bit word				12-2
1024	256 x 4	ER1105	2 µs	100ms/32x4 block	5ms/4 bit word	+12, -12	24 DIP		12-4
1400	100 x 14	ER1400	2.8 µs	16ms/14 bit word	16ms/14 bit word	-35	8 TO/DIP		12-9
4096	1024 x 4	ER2401	2.4µs	100ms/1024x4 block	10ms/4 bit word	5, -14, -24	24 DIP		12-12
		ER2401A	2 µs						12-12
		ER3400	650ns	10ms/4 bit word or 1024x4 block	1ms/4 bit word	+5, -12 -30	22 DIP		12-18
		ER3401	950 ns						12-18
8192	2048 x 4	ER2800	2.6µs	100ms/2048x4 block	10ms/4 bit word	5, -14, -24	24 DIP		12-22
		ER2805	2µs						12-22

READ ONLY MEMORIES — Section 13

BITS	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME	CLOCKS/ VOLTAGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
1024	256 x 4	RO-7-1024/4	--	1µs (typ.)	STATIC	+5, GND, -12	16 DIP	RO-8 versions available for -55°C to +125°C.	13-2
	128 x 8	RO-7-1024/8	--	1us (typ.)	STATIC	+5, GND, -12	24 DIP		13-2
2048	256 x 8	RO-5-1302	INTEL 1302	1.5 µs (typ.)	STATIC	+5, GND, -12	24 DIP	Masked version of 1702	13-4
		RO-7-2048/8	--	1.5 µs (typ.)	STATIC	+5, GND, -12	24 DIP	RO-6 versions available for -55°C to +125°C	13-6
	512 x 4	RO-7-2048/4	--	1.5 µs (typ.)	STATIC	+5, GND, -12	24 DIP		13-6
2560	512 x 5	RO-3-2560	--	450 ns	STATIC	+5, GND	18 DIP		13-8
4096	512 x 8	RO-3-4096	--	500 ns	STATIC	+5, GND	22 DIP		13-10
5120	512 x 10	RO-3-5120	EA 4000	500 ns	STATIC	+5, GND	24 DIP		13-12
8192	2048 x 4	RO-5-8192	AMI S8865	1.2 µs (typ.)	2/TTL	+5, -12	24 DIP		13-14
16384	2048 x 8	RO-3-8316A	INTEL 8316A AMI S6831A	850 ns	STATIC	+5, GND	24 DIP		13-17
		RO-3-8316B		450 ns					13-17
		RO-3-8316C		400 ns					13-22
		RO-3-9316A	INTEL 8316E AMI S6831B MOT 68317	850 ns	STATIC	+5, GND	24 DIP	Replaces two 2708 or 8705 UV PROMs	13-17
		RO-3-9316B		450 ns					13-17
		RO-3-9316C		400 ns					13-22
	4096 x 4	RO-3-16384	AMI S9995	1 µs	STATIC	+5, GND	24 DIP	Address/Chip Select latch	13-23
20480	2048 x 10	RO-3-20480	--	850 ns	STATIC	+5, GND	24 DIP		13-26
32768	4096 x 8	RO-3-9332A	--	850 ns	STATIC	+5, GND	24 DIP		13-2;

Note: All Read Only Memories are mask-programmable

KEYBOARD ENCODERS / CHARACTER GENERATORS — Section 14

BITS	MEMORY ORGANIZATION	PART NUMBER	REPLACES (PIN-FOR-PIN)	ACCESS TIME	CLOCKS/ VOLTAGE	POWER SUPPLIES	PACKAGE	FEATURES	PAGE NO.
2376	88 x 3 x 9 KEYBD. ENCOD	AY-5-2376	SMC KR2376	10-100kHz Scan Rate	1/TTL or INT. OSC	+5, GND, -12	40 DIP	2 key rollover, 66 keys, 3 modes.	14-2
3600	90 x 4 x 10 KEYBD. ENCOD	AY-5-3600	SMC KR3600	10-100KHz Scan Rate	1/TTL or INT. OSC	+5, GND, -12	40 DIP	2-N key rollover, 90 keys 4 modes	14-7
		AY-5-3600PRO	--						14-13
2240	64 x 5 x 7 CHAR. GENER	RO-5-2240S	MK 2302 FSC 3257	1 µs (typ.)	1/TTL for Scanning	+5, GND, -12	24 DIP	5x7 char. column output, on-chip scanning	14-16
2513	64 x 8 x 5 CHAR. GENER	RO-3-2513	SIG 2513	450 ns	STATIC	+5, GND	24 DIP	5x7 characters, row output	14-20
5184	64 x 9 x 9 CHAR. GENER.	RO-5-5184	--	5 µs (typ.)	1/TTL for Scanning	+5, GND, -12	24 DIP	9x9 characters, on-chip left/right scanning	14-25

Note: All Keyboard Encoders and Character Generators are mask-programmable. Standard patterns are available.

AMI DEVICE NO.	GI REPLACEMENT
S1757	AY-5-1013/1013A
S1757	AY-3-1014A/1015
S2470	AY-1-1006
S8865	RO-5-8192
S8996	RO-3-16384

ELECTRONIC ARRAYS DEVICE NO.	GI REPLACEMENT
EA4000	RO-3-5120

EMM/SEMI DEVICE NO.	GI REPLACEMENT
4200	RA-3-4200
4402	RA-3-4402

FAIRCHILD DEVICE NO.	GI REPLACEMENT
3257	RO-5-2240S

INTEL DEVICE NO.	GI REPLACEMENT
1302	RO-5-1302
2316A	RO-3-8316A/8316B
8316A	RO-3-8316A/8316B

MOSTEK DEVICE NO.	GI REPLACEMENT
MK2302	RO-5-2240S
MK50240	AY-3-0215
MK50241	AY-3-0216
MK50242	AY-3-0214
MK50242	AY-1-0212

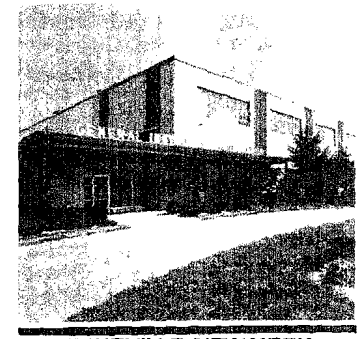
NATIONAL DEVICE NO.	GI REPLACEMENT
MM5303	AY-5-1013/1013A
MM5303	AY-3-1014A/1015
MM5823	AY-1-2006
MM5824	AY-1-1006

SIGNETICS DEVICE NO.	GI REPLACEMENT
2513	RO-3-2513
2536	AY-5-1013/1013A
2536	AY-3-1014A/1015

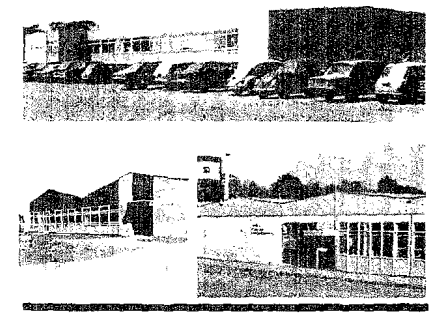
SMC DEVICE NO.	GI REPLACEMENT
COM2505	AY-5-1013/1013A
COM2505	AY-3-1014A/1015
KR2376	AY-5-2376
KR3600	AY-5-3600

WESTERN DIGITAL DEVICE NO.	GI REPLACEMENT
TR1602	AY-5-1013/1013A
TR1602	AY-3-1014A/1015

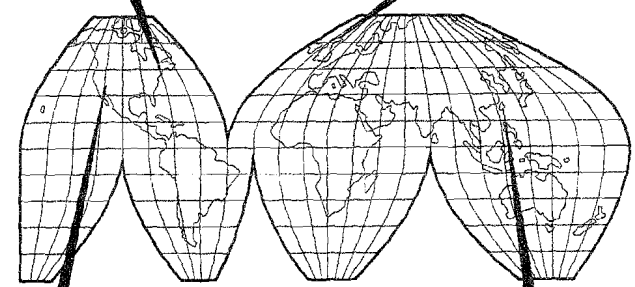
TEXAS INSTRUMENTS DEVICE NO.	GI REPLACEMENT
TMS0803	C-593
TMS0851	CF-593
TMS4000	RO-5-8192
TMS5001	AY-5-3600
TMS6011	AY-5-1013/1013A
TMS6011	AY-3-1014A/1015



HICKSVILLE, NEW YORK



GLENROTHES, SCOTLAND



CHANDLER, ARIZONA

KAOHSIUNG, TAIWAN

MICRO ELECTRONICS

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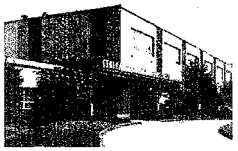
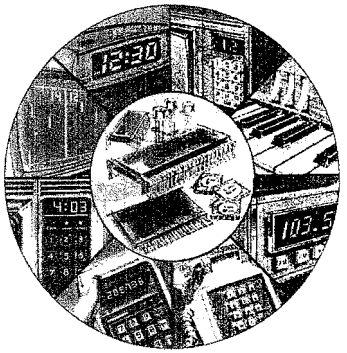
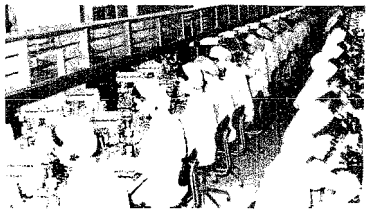


Hicksville, New York—Microelectronics World Headquarters

Glenrothes, Scotland—Mask Aligners.





Kaohsiung, Taiwan—Assembly operation.

General Instrument Microelectronics is one of the world's leading manufacturers of LSI (Large Scale Integration) microcircuits. A pioneer in MOS in 1966, General Instrument is now a worldwide source of microcircuits utilizing Hybrid, Bipolar and MOS technologies in service to the consumer, industrial and public service marketplaces.

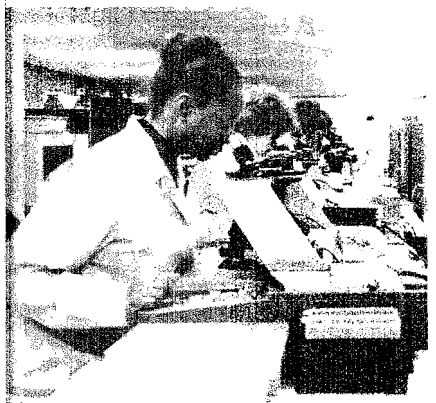
General Instrument Microelectronics has facilities in every major market providing customers with a full spectrum of services including new product development. . applications engineering. . .high volume circuit manufacturing. . .and immediate delivery of over 250 standard products "off the shelf."

Strategically Located Plants

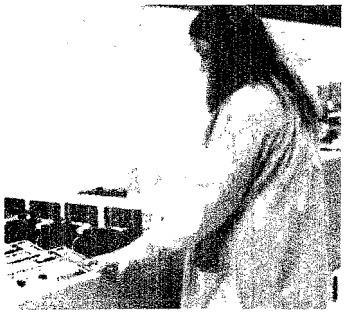
The Microelectronics Group operates four main production facilities in the United States, Europe and Far East. Plants at Glenrothes, Scotland; Chandler, Arizona; and Hicksville, New York, have complete capability for product design. mask making. diffusion, assembly, test and quality assurance. The factory in Kaohsiung, Taiwan, is dedicated to high volume assembly, test, quality assurance and applications of Microelectronics products.

In addition to providing reliable sources of supply on three continents, General Instrument operates each plant as a backup facility to the others, to insure uninterrupted delivery. Common processes and equipment are employed and major product styles are always produced in at least two separate locations. To maintain uniform standards from plant to plant, the quality assurance and process control groups at each facility are directed by quality control policy established at Group and Corporate levels.

Because General Instrument has a comprehensive exposure to all of the world LSI markets, it has been able to structure its facilities and engineering programs to conform to evolving customer needs. Production capabilities are concentrated in product areas of greatest volume. Each



ville, New York—Test area



Chandler, Arizona—Wafer Coating

plant has several separate manufacturing modules dedicated to the process most relevant to the primary marketplace. Cost effectiveness for the customer is enhanced because import duties are frequently saved on locally manufactured products.

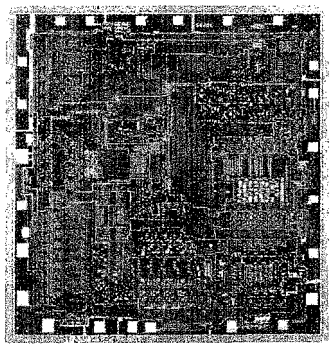
Broad Product Lines

General Instrument Microelectronics offers the widest range of standard LSI microcircuits in the industry. The company's off-the-shelf portfolio consists of over 250 different LSI products in fifteen families dedicated to the consumer, telecommunications and data marketplaces.

For the consumer market, General Instrument has pioneered LSI circuits for calculators, clocks, clock radios, TV tuners, remote control, appliance timers, radio and high fidelity systems, musical apparatus and TV games. For example, in 1976 General Instrument introduced the AY-3-8500 video game chip, the first standard single chip LSI microcircuit to provide six different games with on-screen scoring and realistic sound; over 5 million such parts were shipped that year.

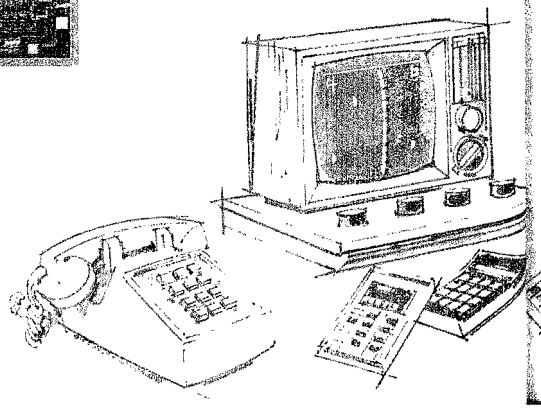
More recently, General Instrument has introduced its GIMINI LSI System for cassette operated "home information terminals," a product expected to be the next major development in consumer electronics.

Beginning in 1970, General Instrument has been a major manufacturer of microcircuits for hand held and printing calculators. Product selection ranges from low cost "four function" chips to complex circuits for consumer and business printing calculators.



Microphoto of AY-3-8500 TV Game chip.

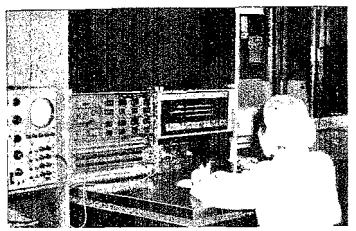
Glenrothes, Scotland—Assembly operation.



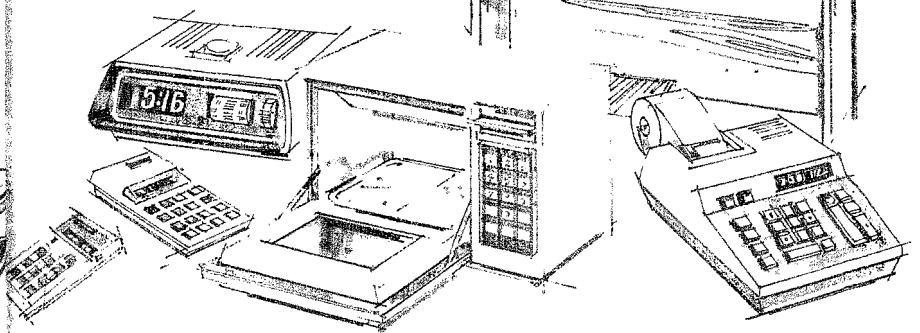
Another major development by General Instrument in the consumer marketplace is the introduction of the OMEGA series of digital tuning systems. The OMEGA concept brings the tuning precision and convenience of digital channel selection to the TV set, without the need for standby battery power to retain channel memory when the set is off. This pioneering advance was made possible by the utilization of a unique electrically alterable ROM (EAROM). The EAROM combines the reprogrammability of a RAM with the non-volatility of a hard-wired ROM. Recently, the OMEGA concept has been made available for popular priced TV — ECONOMEGA — and introduced in a special form for high fidelity systems — STEREOMEGA.

Supported by General Instrument Corporation's long experience in telecommunications, the Microelectronics Group has developed a series of standard circuits for use in the conversion of telephone apparatus from electromechanical to all-electronic operations. These circuits are being sold to major producers of telephone apparatus around the world, and have been qualified by major government telecommunications authorities. New circuits now being introduced in the telecommunications area are aiding in the development of solid state PABX's and digital central offices — the wave of the future in the telecommunications industry.

General Instrument has pioneered in the development of 16-Bit LSI microprocessor technology. The CP1600 introduced in 1975, has now evolved into a complete family of products for use in consumer, telecommunications and industrial control applications. Extensive software and applications support this reliable and cost effective microprocessor family.



Kaohsiung, Taiwan—Test facility



In addition to its work on standard microprocessors, General Instrument has also specialized in the concept of the dedicated microprocessor — that is a microprocessor architecture specifically tailored to a particular application. By combining the programmability of the microprocessor with optimum input-output architecture for a particular application, General Instrument provides the cost-effective solution for product development in each of the markets it serves.

Unlike many other LSI manufacturers, General Instrument Microelectronics does not produce end products. Our slogan, "We Help You Compete" means just that. We do not compete with our customers. Hence, customers can share their ideas for product innovation through LSI with us in confidence, knowing that we will not manufacture the end product ourselves.

We also help our customers compete by our concentration on cost-effective LSI manufacture. For example, the General Instrument Mini-Pak, introduced in 1976 for Consumer products, provides a significant saving in labor and material versus the popular dual-in-line plastic package.

Customer Service

General Instrument Microelectronics believes in CUSTOMER SERVICE. Independent customer service departmen are maintained at each major location to provide immediate response to questions concerning order service and delivery. O customer service personnel are trained to consider our customer's needs as their most urgent requirement. Call on them and let us prove that we are dedicated to responsive service.

Advanced Design Centers

To provide our customers with the latest i LSI technology, General Instrument Micro electronics maintains R&D centers at Glenrothes, Scotland; Hicksville, New York; and Chandler, Arizona. In addition, the Microelectronics activity is supported by general research in various fields carried out with such prestigious organizations as the Massachusetts Institute of Technology and the University of Utah.

In addition to its extensive catalog of standard products, General Instrument Microelectronics is happy to provide custom design service to satisfy special requirements. In some cases, the application is best served by a software or firmware modification of one of our standard microprocessors. In other cases, a dedicated microprocessor is more cost effective. These services may be arranged through any of the Microelectronics sales offices.

Applications Assistance Around the Globe

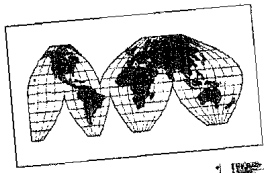
To provide the special applications assistance that customers may require, General Instrument Microelectronics maintains fully staffed Applications Centers at strategic locations around the world. . .

U.S.A. — Hicksville, New York and Chandler, Arizona

EUROPE — Glenrothes, Scotland; London, England; and Munich, Germany

ASIA — Kaohsiung, Taiwan; Tokyo, Japan; and Hong Kong

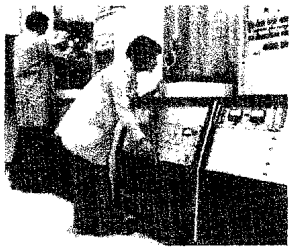
Arrangements can be made for immediate assistance from these centers by contacting any of the sales offices listed in our catalog.



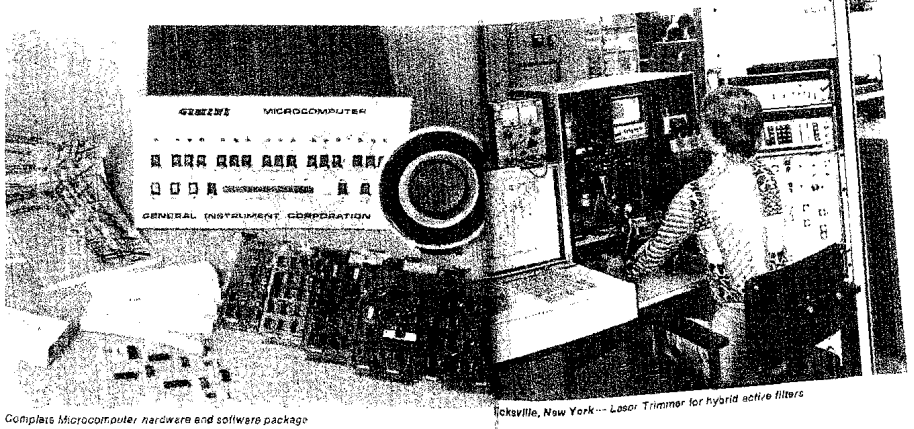
Corporate Support

General Instrument Microelectronics is backed by the full resources of the General Instrument Corporation, which has for over 50 years been among the leaders in the application of modern technology to entertainment, industrial, military, data and communications electronics. The skills, production know-how, and technological capability of the entire General Instrument organization are utilized by the Microelectronics Group to further improve its products and customer services.

Among the many other electronic components manufactured by General Instrument are discrete semiconductors, relays, miniature lamps, and TV components. General Instrument is a leading manufacturer of cable TV products, off-track and on-track wagering systems, point-of-sale equipment and apparatus for defense applications.

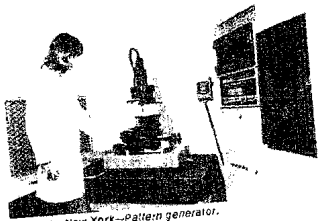


Chandler, Arizona—Electron Beam Evaporation.



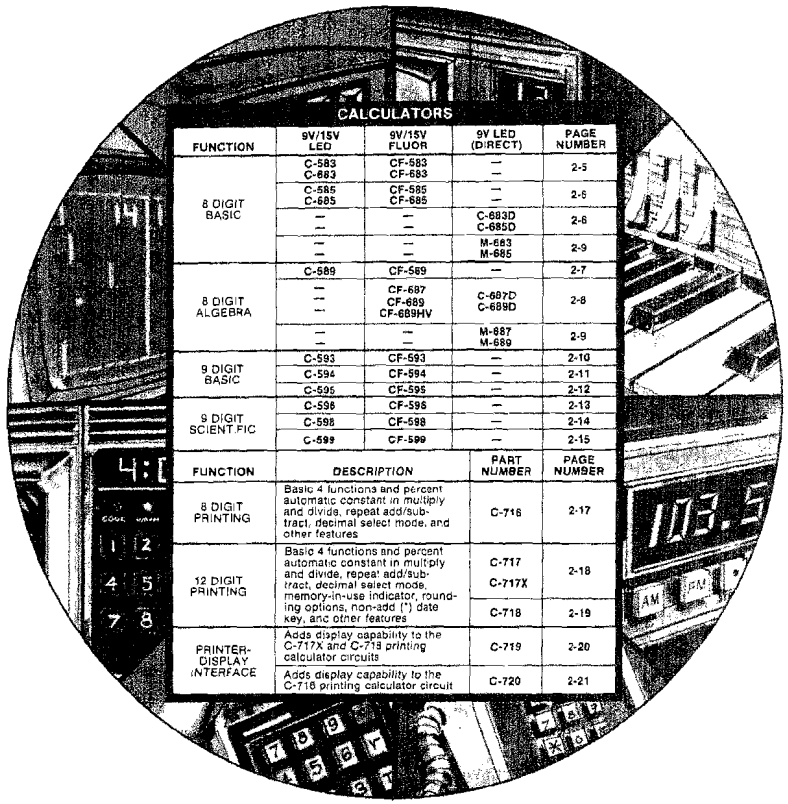
Complete Microcomputer hardware and software package

Hicksville, New York — Laser Trimmer for hybrid active filters



Hicksville, New York—Pattern generator.

Glenrothes, Scotland—Test area



CALCULATORS

FUNCTION	9V/15V LED	9V/15V FLUOR	9V LED (DIRECT)	PAGE NUMBER
8 DIGIT BASIC	C-583 C-683	CF-583 CF-683	— —	2-5
	C-585 C-685	CF-585 CF-685	— —	2-6
	— —	— —	C-683D C-685D	2-8
	— —	— —	M-683 M-685	2-9
8 DIGIT ALGEBRA	C-589	CF-589	—	2-7
	— — —	CF-687 CF-689 CF-689HV	C-687D C-689D	2-8
	— —	— —	M-687 M-689	2-9
9 DIGIT BASIC	C-593	CF-593	—	2-10
	C-594	CF-594	—	2-11
	C-595	CF-595	—	2-12
9 DIGIT SCIENTIFIC	C-598	CF-598	—	2-13
	C-598	CF-598	—	2-14
	C-599	CF-599	—	2-15

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 DIGIT PRINTING	Basic 4 functions and percent automatic constant in multiply and divide, repeat add/subtract, decimal select mode, and other features	C-716	2-17
12 DIGIT PRINTING	Basic 4 functions and percent automatic constant in multiply and divide, repeat add/subtract, decimal select mode, memory-in-use indicator, rounding options, non-add (*) date key, and other features	C-717 C-717X	2-18
		C-718	2-19
PRINTER-DISPLAY INTERFACE	Adds display capability to the C-717X and C-718 printing calculator circuits	C-719	2-20
	Adds display capability to the C-716 printing calculator circuit	C-720	2-21

CALCULATORS

MICRO ELECTRONICS

2

Display Calculator Circuits

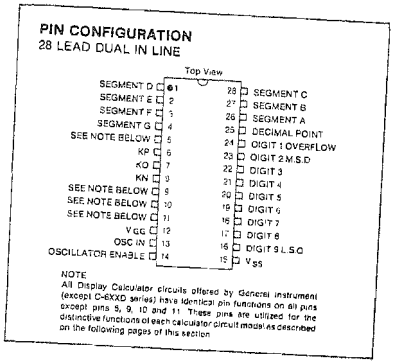
FEATURES

- Printed circuit board compatibility of circuits.
- Direct segment drive for LED displays (C-XXX)
- Direct fluorescent display drive (CF-XXX)
- Direct segment and digit drive for LED displays (C-XXXD)
- Algebraic operation
- Automatic constant
- Floating point operation
- Constant or chain operation (no switch required)
- Leading zero suppression
- Automatic power-on clear
- Internal clock (on-chip oscillator)
- Internal keyboard debounce logic

DESCRIPTION

General Instrument's broad line of display calculator circuits, the C/CF-500 Series and the C/CF-600 Series, consists of pin-for-pin compatible circuits (except C-6XXD series) designed to fit in the same basic PC board. This provides a high degree of flexibility in calculator models manufactured while minimizing the tooling required.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



NOTE
All Display Calculator circuits offered by General Instrument (except C-6XXD series) have identical pin functions on all pins except pins 5, 9, 10 and 11. These pins are utilized for the distinctive functions of each calculator circuit model as described on the following pages of this section.

FUNCTION	DESCRIPTION	9V LED	9V FLUOR.	9V LED (DIRECT)	15V FLUOR.	15V LED
8 DIGIT BASIC	4 functions and percent key.	C-583	CF-583	C-583D	CF-583	C-583
	4 functions, percent key, one-key or multi-key memory.	C-585	CF-585	C-585D	CF-585	C-585
8 DIGIT ALGEBRA	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, choice of 20 to 29 keys.		CF-587	C-587D	CF-589	C-589
	4 functions, percent key, x^2, $\sqrt{x}$, 1/x, +/-, one-key or multi-key memory, brackets, inch-centimeter conversion, choice of 24 to 30 keys.		CF-689	C-689D	CF-689HV	—
9 DIGIT BASIC	4 functions and percent key				CF-593	C-593
	4 functions, percent key, one-key memory.				CF-594	C-594
	4 functions, percent key, multi-key memory				CF-595	C-595
9 DIGIT SCIENTIFIC	Basic 4 functions, scientific notation, sin, cos, tan, arc sin, arc cos, arc tan, memory, square root, pi, natural logs, 1/x, e^x, memory exchange, degrees and radians, exponent range ± 99, choice of 19 to 35 keys				CF-596	C-596
	All the above plus: 0 to 10^{99} degree trig range, $\log_{10}$, y^x, extended digit accuracy of transcendentals, choice of 21 to 38 keys.				CF-598	C-598
	All the above plus: two levels of parenthesis, x^2, %, +/-, choice of 24 to 41 keys.				CF-599	C-599

I THE FOLLOWING APPLY AS NOTED:

A. AUTOMATIC CONSTANT (All circuits)
The answer from any operation is entered automatically as a Constant by the = key without a constant switch. The Constant may then be used with all five functions and the answer from any Constant calculation can be used for further calculations without re-entry. This provides an extremely powerful facility for solving many complex equations without the need for writing down or remembering intermediate results. It is particularly useful for raising to a power, compound interest calculations, nth roots, depreciation calculations, etc. In constant multiplication, the constant is the first entered number (constant multiplicand). In division, addition and subtraction, the constant is the second entered number. The completion of the first operation with the depression of the = key initiates the storage of the constant number. For subsequent operations it is only necessary to enter a number and depress the = key.

B. DECIMAL ALIGNMENT (C/CF-593, C/CF-594, C/CF-595)
The results of addition or subtraction will remain aligned to the preceding number having the most decimal places. This feature allows computation in the dollar and cents mode without suppression of the zeros to the right of the decimal point. If a right shift is needed to keep the eight most significant digits, the least significant digits are lost. The results of multiplication and division will be completely right adjusted such that only the most significant digits are displayed except during overflow.

C. CAPACITY (All except Scientific Circuits)
For the C/CF-580 Series and the C/CF-680 Series, in the case of overflow, the eight most significant digits are displayed (seven digits and minus sign for negative answers) all decimal points are lit and the keyboard is locked out. Only the operation of the clear key will allow continued operation. On depression of the clear key, the decimal point is shifted eight places to the left of its actual position.
For the C/CF-593, 594 and 595, in the case of overflow, the overflow symbol is displayed, and the decimal point shifted eight places to the left of its actual position. Under these conditions, the keyboard is locked out such that only the operation of the clear key will allow continued operation.
In all cases, for an attempted entry requiring more than eight display digits, the most significant digits are protected upon the attempted entry of another digit. The keyboard is not locked out and operations are still able to be performed.
When division by zero is attempted, an overflow condition results and a zero is displayed.

D. PERCENT KEY (all except C/CF-596 and 598)
Multiplies the two preceding entries and divides by 100, and when followed by = gives add-on and discount: A+B% yields (AB/100); A+B%=yields A+(AB/100). A−B% yields (AB/100); A−B%=yields A−(AB/100)

E. CHANGE NOTATION KEY (Scientific Circuits)
Depression of the CHG NOT key will convert the displayed number to scientific notation, if it is in the "normal" mode, or it will display the 8 most significant digits of a scientific mantissa with the decimal point correctly located (even if it falls beyond the display area) and trailing zeroes shall be blanked. In addition, for numbers less than one, the digits are left shifted until all leading zeroes have been eliminated.

F. EXPONENT KEY (Scientific Circuits)
EEX: This key operates as follows: The EEX key sets the two right most digits to zero, the third digit from the right is blanked and the calculator is conditioned to accept sign and numeral keys to define the exponent value of the number entry. If the mantissa had numbers in any of the last three digit positions, these are retained but not displayed.

G. FUNCTION KEY OPERATIONS (Used only with dual-function keys)
Depression of the F key sets the calculator in the "Function" mode and the F indicator is lit. The dual function keys will then function as indicated by their upper case designation. Single function keys directly perform the indicated function.
Depression of the second key of the sequence resets the "Function" mode and the F indicator is turned off when the answer is displayed. The "Function" mode can also be reset by a second depression of the F key.

II THE FOLLOWING APPLY AS NOTED TO CIRCUITS WITH MEMORY:

A. MEMORY DESCRIPTION: One-Key memory as provided in C/CF-585, 589, 594, 685, C-685D, C-689D and CF-689.
M: The Memory key is used in conjunction with other function keys to define a two key sequence which sets a mode of operation associated with the memory register and terminates any immediately preceding entry.
Operation of the M key followed by + adds the contents of the display register to the memory register without altering the contents of the display register.
Operation of the M key followed by − subtracts the contents of the display register without altering the contents of the display register.
Operation of the M key followed by = transfers the contents of the memory register into the display register without altering the contents of the memory register.
Operation of the M key followed by C/CE clears the contents of the memory register.
Operation of the M key followed by the X key performs a memory-display exchange function. The contents of the memory register are brought out to the display register and the contents of the display register are written into the memory register, replacing the previous contents of the memory register.
Operation of the M key followed by any key other than +, −, X, =, or C/CE shall reset the M condition and act upon the subsequent entry as if the M had not been entered.
In addition, two optional keys are provided with the C/CF-594 for operation as follows.
MR, MEMORY READ: Functions identically to the M = sequence above.
MC, MEMORY CLEAR: Functions identically to the M C/CE sequence above.

B. MEMORY DESCRIPTION: Multi-key memory as provided in all algebra, scientific circuits, and C-685D.
MR, MEMORY READ: Functions identically to the M = sequence above.
MC, MEMORY CLEAR: Functions identically to the M C/E sequence above.
M+, MEMORY PLUS: Functions identically to the M+ sequence above.
M−, MEMORY MINUS: Functions identically to the M− sequence above.
MEX, MEMORY EXCHANGE: Functions identically to the MX sequence above.
In addition, the C/CF-589 are provided with a STORE key which transfers the contents of the display to memory without changing the display.

C. MEMORY DESCRIPTION: Multi-key memory as provided in C/CF-585, 595 and 685.
MC, MEMORY CLEAR: clears the memory while leaving the display intact.
MR, MEMORY READ: transfers the data in memory to the display without changing the memory.
M∓, MEMORY EQUALS/PLUS: completes the preceding operation, displays the result, and adds the result to the memory.
M=, MEMORY EQUALS/MINUS: completes the preceding operation, displays the result and subtracts the result from the memory.
In addition, the C/CF-585 and C/CF-685 are provided with a MEX (Memory Exchange) Key which functions as previously described.
The C/CF-595 is provided with the following additional memory keys:
MR/MC, MEMORY READ/MEMORY CLEAR: this single key operation transfers the memory data to the display on the first depression. When depressed two successive times, the memory data is transferred to the display and the memory cleared.
Σ+ SUM KEY: when connected to V_{SS}, this accumulate switch, independent of the keyboard, adds the contents of the display to memory with each depression of the equals key.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*	Fluorescent Display CF-5XX Series	LED Display C-5XX Series	Fluorescent Display CF-6XX Series	LED Display C-6XX/ C-6XXD Series
V_{GG} supply voltage range[1]	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	−15V to +0.3V
Clock input voltage range[1]	−20V to +0.3V	−20V to +0.3V	−15V to +0.3V	−15V to +0.3V
Data input voltage range[1]	−32V to +0.3V	−20V to +0.3V	−30V to +0.3V	−15V to +0.3V
Applied output voltage range[1]	−32V to +0.3V	−20V to +0.3V	−30V to +0.3V	−15V to +0.3V
Maximum power dissipation at +25°C[2]	500 mW			
Storage temperature range	−20°C to +70°C			
Operating free-air temperature range	0°C to +40°C			
Relative humidity range (no condensation)	0 to 95%			

All inputs and outputs are internally protected against static charge damage during handling consistent with standard industry practices.

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

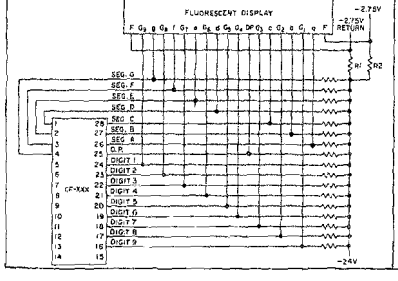
[1] Measured with respect to V_{SS}.
[2] Derate at 10mW/°C.

Operating Conditions	CF-5XX Series Range	C-5XX Series Range	C/CF-6XX Series Min.	Typ.*	Max.	C-6XXD Series Min.	Typ.*	Max.
V_{SS}, substrate supply	0V	0V		0V			0V	
V_{GG}, gate supply: C/CF-5XXA	−15.0V±5%	−15.0V±5%		—			—	
C/CF-5XXB	−16.0V±5%	−16.0V±5%		—			—	
C/CF-5XXC	−17.0V±5%	−17.0V±5%		—			—	
C-6XXA	—	—	−10.3V	−7.5V	−6.5V	−10.3V	−7.5V	−6.5V
C-6XXB	—	—	−9.5V	−7.5V	−6.5V	−9.5V	−7.5V	−6.5V

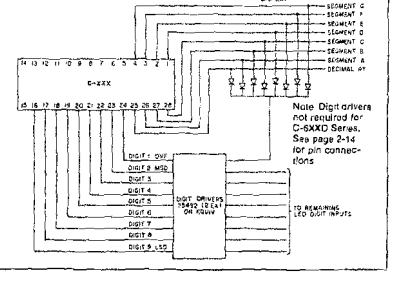
Characteristics- at typical operating conditions over a 0°C to +40°C range.	CF-5XX/6XX Series Min.	Typ.*	Max.	C-5XX Series Min.	Typ.*	Max.	C-6XX Series Min.	Typ	Max.	C-6XXD Series Min.	Typ.*	Max.
Keyboard input characteristics-												
Input signal levels: Logic 0	−1.5V	—	0V	−1.5V	—	0V	−0.5V	—	0V	−0.5V	—	0V
Logic 1	V_{GG}	—	−6.0V	V_{GG}	—	−6.0V	V_{GG}	—	−4.0V	V_{GG}	—	−4.0V
Keyboard resistance	—	—	1K	—	—	1K	—	—	1K	—	—	1K
Output buffer characteristics-[3]												
Segment output on-resistance: at −0.5V V_{OUT}	—	—	—	—	—	—	—	200Ω	300Ω	—	1K	1.3K[4]
at −1.5V V_{OUT}	—	200Ω	600Ω	—	200Ω	300Ω	—	—	—	—	—	—
Digit output on-resistance at −1.5V V_{OUT}	—	200Ω	300Ω	—	200Ω	300Ω	—	200Ω	300Ω	—	30Ω	50Ω[5]
Digit and segment off-leakage: at V_{OUT}=−9V	—	—	—	—	—	18μA	—	—	18μA	—	—	100μA[6]
at V_{OUT}=−27V (CF-590, CF-680 Series) or V_{OUT}=−30V (CF-580 Series)	—	—	18μA	—	—	—	—	—	—	—	—	—
Anode and grid supply voltage through 200K resistor: CF-580 Series	−30V	−24V	—	—	—	—	—	—	—	—	—	—
CF-590, CF-680 Series	−27V	−24V	—	—	—	—	—	—	—	—	—	—
Power (all outputs off)-												
at V_{GG}=−16.0V, C/CF-580 Series	—	75mW	100mW	—	75mW	100mW	—	—	—	—	—	—
at V_{GG}=−16.0V, C/CF-590 Series	—	100mW	125mW	—	100mW	125mW	—	—	—	—	—	—
at V_{GG}=−7.5V, C-680 Series	—	—	—	—	—	—	—	15mW	30mW	—	15mW	30mW

[3] All output buffers are open-drain to V_{SS}.
* Typical values are at +25°C and nominal voltages.
[4] At 4mA
[5] At 36mA
[6] At −9V

FLUORESCENT DISPLAY INTERCONNECT



LED DISPLAY INTERCONNECT



C-583 C-683
CF-583 CF-683

8 Digit / 5 Function Basic Calculator Circuits

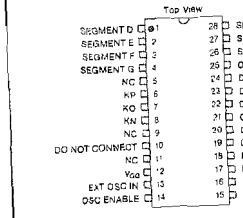
2

FEATURES

- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- C-583 and C-683: direct LED segment drive. CF-583 and CF-683: direct fluorescent display drive.
- All other features listed on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



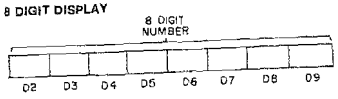
NOTE
The oscillator is enabled by connecting a resistor from V_{GG} to pin 14 (150K ±10% for C/CF-583, 470K ±10% for C/CF-683).

DESCRIPTION

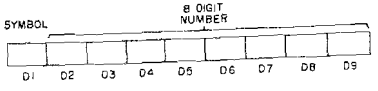
The C/CF-583 and C/CF-683 circuits are basic five-function circuits which may be used with either eight or nine digit LED or fluorescent displays. They compute and display the results of calculations with numbers up to eight digits (seven for negative). On overflow, the keyboard is locked and all decimal points are lighted. In addition, an overflow symbol will appear in the ninth digit position for those calculators having nine digit displays.

DISPLAY

8 DIGIT DISPLAY

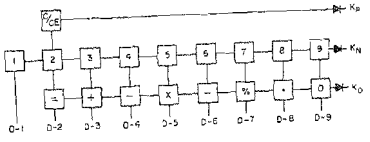


OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT

KEY MATRIX



Note: Diodes used only for CF-583 and CF-683.

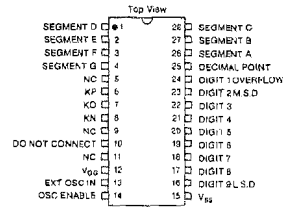
8 Digit / 5 Function Basic Calculator Circuits With One-Key or Multi-Key Memory

FEATURES

- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-585 and C-665: direct LED segment drive. CF-585 and CF-685: direct fluorescent display drive.
- All other features listed on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



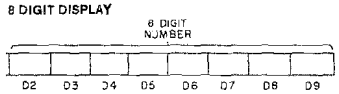
NOTE:
The oscillator is enabled by connecting a resistor from V_{GG} to pin 14 (150K ±10% for C/CF-585, 470K ±10% for C/CF-685)

DESCRIPTION

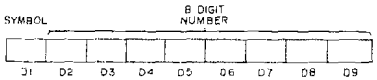
The C/CF-585 and C/CF-685 circuits are basic five-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-583 and C/CF-683 circuits with the addition of the memory function.

DISPLAY

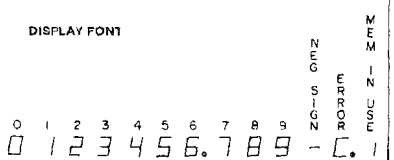
8 DIGIT DISPLAY



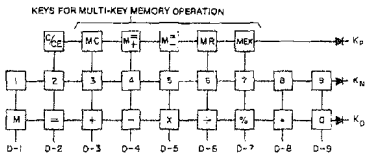
OPTIONAL 9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-585 and CF-685.

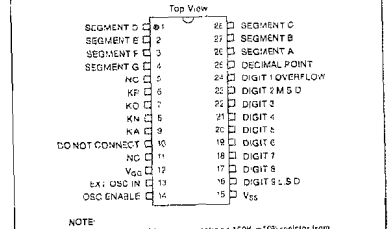
8 Digit / 9 Function Algebra Calculator Circuits With One-Key or Multi-Key Memory

FEATURES

- 8 digit, 7 segment display outputs.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Convenience functions (x^2, $\sqrt{x}$, 1/x, +/-)
- Floating negative sign.
- Right-justified entry and result.
- One-key or multi-key memory function (refer to the description at the beginning of this section.)
- C-589: direct LED segment drive. CF-589: direct fluorescent display drive.
- All other features listed on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



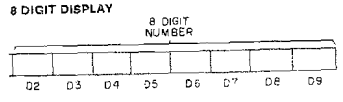
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14

DESCRIPTION

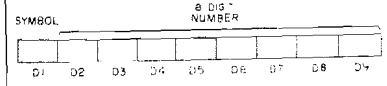
The C/CF-589 circuits are basic eight-function memory circuits which offer the user the highest degree of functional flexibility in implementing a memory calculator. The circuits include all the features of the C/CF-585 circuits with the addition of the functions x^2, $\sqrt{x}$, 1/x and +/−. The C/CF-589 circuits may be operated with either single or dual function keys with a keyboard configuration of from 20 to 29 keys.

DISPLAY

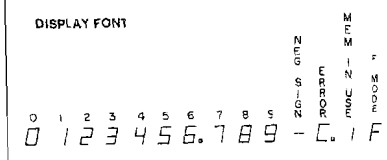
8 DIGIT DISPLAY



OPTIONAL 9 DIGIT DISPLAY

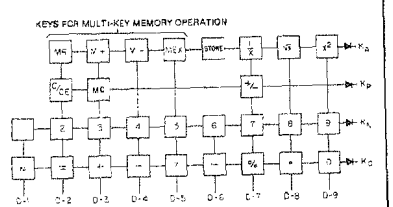


DISPLAY FONT

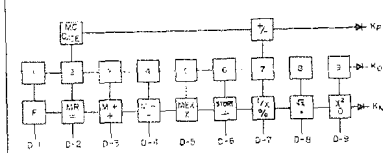


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-589

8 Digit Direct Drive Algebra Calculator Circuits

FEATURES

- Direct LED segment and digit drive (except CF-687/689/689HV)
- 8 digit, 7 segment display outputs
- Floating negative sign.
- Right-justified entry and result.
- All other features listed on the first page of this section.

C-683D: 5 Function
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).

C-685D: 5 Function with Memory
- Basic four arithmetic functions (+, −, x, ÷)
- Percent (add-on and discount)
- One-key or multi-key memory function (refer to the description at the beginning of this section).

C-687D: 11 Function with Memory
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount)
- One-key or multi-key memory function (refer to the description at the beginning of this section).
- Convenience functions (x^2, $\sqrt{x}$, 1/x, +/−, x-y exchange)
- π key to display the value of π
- User option for single or dual function key operation.

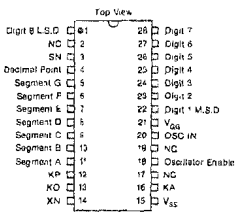
C-689D: 13 Function with Memory
- All features of the C-687D plus linear metric conversion (inch-cm, cm-inch) and one level of parenthesis.

CF-687: 11 Function with Memory
- Same as C-687D except direct flourescent display drive.

CF-689/CF-689HV 13 Function with Memory
- Same as C-689D except direct fluorescent display drive. Supply voltage: 9V for CF-689 15V for CF-689HV.

PIN CONFIGURATION

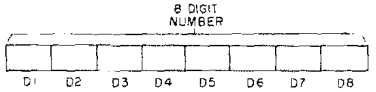
28 LEAD DUAL IN LINE
(Also available in a 28 Lead Mini-Pak)



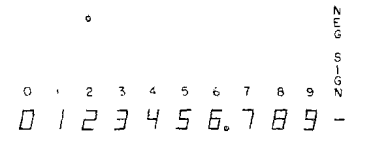
NOTE
The oscillator is enabled by connecting a 150K ±10% resistor from V_{DD} to pin 18

DISPLAY

8 DIGIT DISPLAY

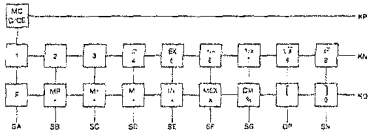


DISPLAY FONT

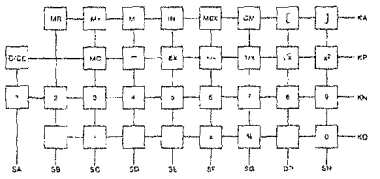


KEY MATRIX (C-689D shown)

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



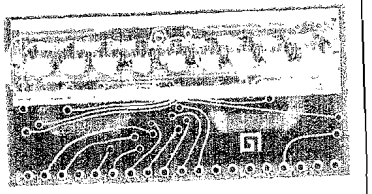
PRELIMINARY INFORMATION

8 Digit Calculator Modules

MODULE FEATURES

- 8 Digit LED display & lens with calculator circuit on one board
- Algebraic operation
- Automatic constant
- Floating point operation
- Constant or chain operation (no switch required)
- Leading zero suppression
- Automatic power on clear
- Internal clock (on-chip oscillator)
- Internal keyboard debounce logic
- Self contained module (only needs keyboard and battery for complete calculator)

M-683/685/687/689 MODULE



Note: Mini-Pak mounted on back side

CALCULATOR FEATURES

- M-683 — 4 function with percent key
- M-685 — 4 function, percent key, one or multi-key memory
- M-687 — 4 function, percent key, slide rule functions, one or multi-key memory
- M-689 — Same as 687 with brackets, inch centimeter conversion.

DESCRIPTION

The M-683, 685, 687, 689 series of modules contains an eight digit LED display and a C-680D series calculator circuit featuring all the necessary logic, contact noise elimination circuits and timing for a complete, simple to use, low-cost, multi-featured calculator. For full information on the many features of the calculator circuits used on these modules, refer to the detailed descriptions on the preceding pages.

The M-680 series modules are fabricated on a double-sided printed circuit board.

9 Digit / 5 Function Basic Calculator Circuits

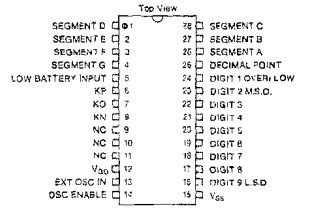
FEATURES

- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- C-593: direct LED segment drive.
  CF-593: direct fluorescent display drive
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-593 circuits are basic five-function circuits for use with nine digit LED or fluorescent displays. These circuits enter and compute both positive and negative numbers to an eight digit resolution. On overflow, the overflow symbol is displayed in the ninth digit position, the decimal point is automatically shifted eight positions to the left of its computed position and the keyboard is locked.

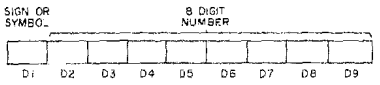
PIN CONFIGURATION
28 LEAD DUAL IN LINE



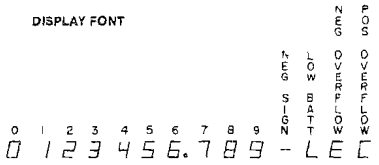
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14

DISPLAY

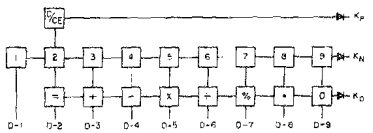
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-593.

9 Digit / 5 Function Basic Calculator Circuits With One-Key Memory

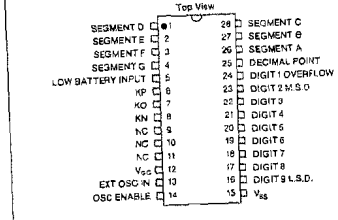
FEATURES

- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- One-key memory operation, with option for two additional memory function keys (refer to the description at the beginning of this section).
- C-594: direct LED segment drive.
  CF-594: direct fluorescent display drive.
- All other features listed on the first page of this section.

DESCRIPTION

The C/CF-594 circuits enable a manufacturer to add a memory calculator to his line with the simple inclusion of one additional memory key in the matrix of the C/CF-593 keyboard. All other operations are identical to the C/CF-593.

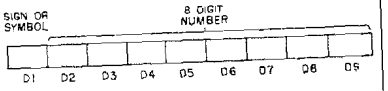
PIN CONFIGURATION
28 LEAD DUAL IN LINE



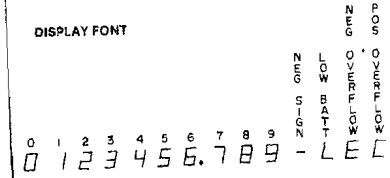
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DISPLAY

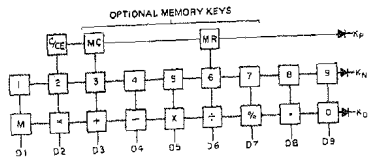
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-594.

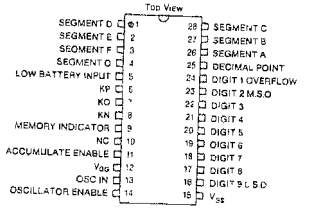
9 Digit / 5 Function Basic Calculator Circuits With Multi-Key Memory

FEATURES

- 8 digit, 7 segment display outputs with ninth digit for sign or symbol.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Floating negative sign.
- Right-justified entry and result.
- Results of addition or subtraction remain aligned to preceding number having most decimal places.
- Multi-key memory operation and automatic accumulating memory (refer to the description at the beginning of this section.)
- C-595: direct LED segment drive.
  CF-595: direct fluorescent display drive.
- All other features listed on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



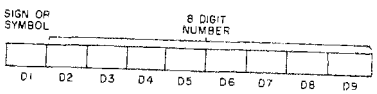
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DESCRIPTION

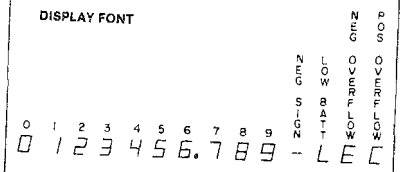
The C/CF-595 circuits add a variety of memory options to the basic C/CF-593 functions. While the basic pin configuration is identical to the C/CF-593, two additional connections are provided for a selectable "memory accumulate" switch and a "memory in use" indicator output.

DISPLAY

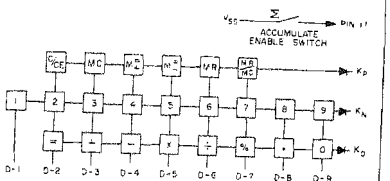
9 DIGIT DISPLAY



DISPLAY FONT



KEY MATRIX



Note: Diodes used only for CF-595.

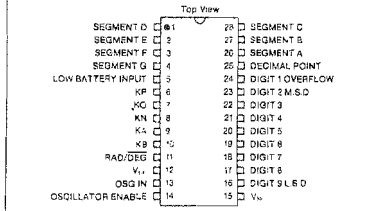
9 Digit / 15 Function Scientific Calculator Circuits

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
  8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln$x$ and e^x).
- Convenience functions ($\sqrt{x}$, 1/x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation
- C-596: direct LED segment drive.
  CF-596: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



NOTE.
The oscillator is enabled by connecting a 470K ±10% resistor from V_{GG} to pin 14.

DESCRIPTION

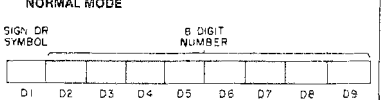
The C/CF-596 circuits are fifteen function circuits which offer trigonometric and inverse trigonometric functions, natural logs, e^x, $\sqrt{x}$, 1/x and π as well as the basic four functions and memory.

The circuit operates in the normal 8 digit mode until the display capacity is exceeded at which time it converts to the scientific mode of operation.

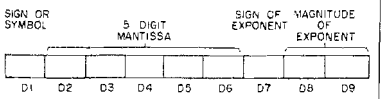
The C/CF-596 features single or dual function key operation for a keyboard configuration of from 19 to 35 keys.

DISPLAY

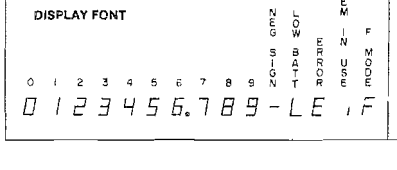
NORMAL MODE



SCIENTIFIC NOTATION

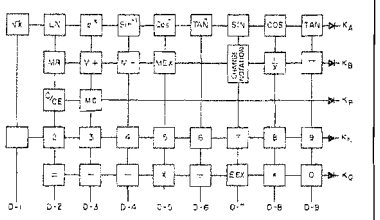


DISPLAY FONT

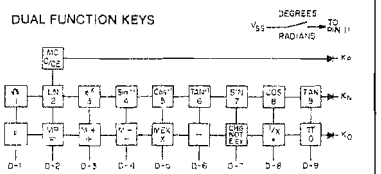


KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-596.

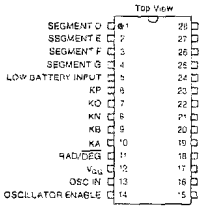
9 Digit / 18 Function Scientific Calculator Circuits

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, 1/x, y^x).
- A separate memory register (refer to the description at the beginning of this section).
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-598: direct LED segment drive.
  CF-598: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



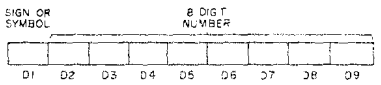
NOTE:
The oscillator is enabled by connecting a 470K ±10% resistor from V_{GG} to pin 14.

DESCRIPTION

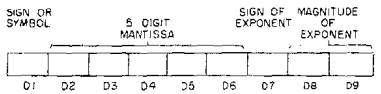
The C/CF-598 circuits are eighteen function circuits whose operations are identical to the C/CF-596 with the addition of three functions: $\log_{10}$, 10^x and Y^x. Single or dual function key operation is optional with keyboard configurations of from 21 to 38 keys.

DISPLAY

NORMAL MODE



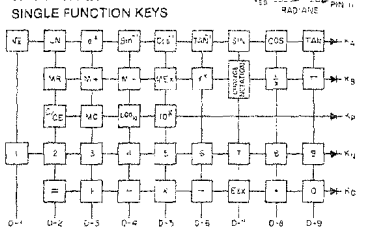
SCIENTIFIC NOTATION



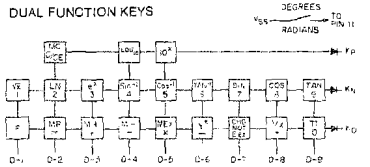
DISPLAY FONT

KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-598.

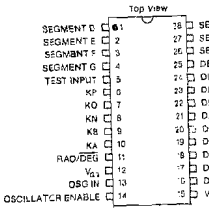
9 Digit / 21 Function Scientific Calculator Circuits

FEATURES

- Number entry in floating point or scientific notation.
- 9 digit output with 5 digits of the mantissa displayed, 2 digits for the exponent, and 2 digits for the sign of the mantissa and exponent.
- 8 digit display and sign for numbers not requiring scientific notation, or for the display of the 8 significant digits of a number that is in scientific notation.
- Basic four arithmetic functions (+, −, x, ÷).
- Percent (add-on and discount).
- Transcendental functions (sin, cos, tan, $\sin^{-1}$, $\cos^{-1}$, $\tan^{-1}$, ln x, e^x, $\log_{10}$ and 10^x).
- Convenience functions ($\sqrt{x}$, $1/x$, y^x, x^2, +/−).
- A seperate memory function (refer to the description at the beginning of this section).
- Two levels of parentheses.
- Trigonometric functions are performed in degrees or radians (switch selectable).
- π key to display the value of π.
- Left-justified entry and result.
- User option for single or dual function key operation.
- C-599: direct LED segment drive.
  CF-599: direct fluorescent display drive.
- All other features described on the first page of this section.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



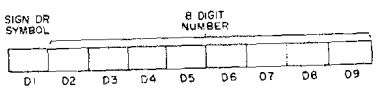
NOTE:
The oscillator is enabled by connecting a 150K ±10% resistor from V_{GG} to pin 14.

DESCRIPTION

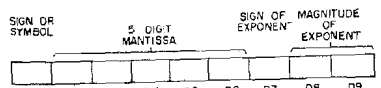
The C/CF-599 circuits are twenty-one function circuits whose operations are identical to the C/CF-598 with the addition of two levels of parentheses and three functions: x^2 % and +/−. Single or dual function key operation is optional with keyboard configurations of from 24 to 41 keys.

DISPLAY

NORMAL MODE



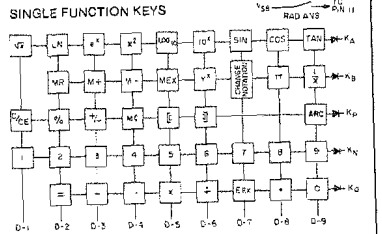
SCIENTIFIC NOTATION



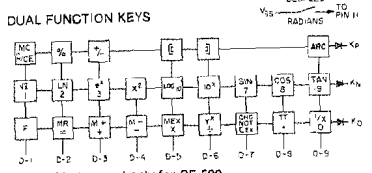
DISPLAY FONT

KEY MATRIX

SINGLE FUNCTION KEYS



DUAL FUNCTION KEYS



Note: Diodes used only for CF-599.

Printer Calculator Circuits

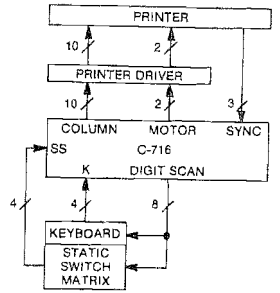
FEATURES

- 5 functions (+,−, ×, ÷,%).
- Chain calculations.
- Repeat add/subtract
- Automatic underflow and reverse underflow.
- Non-add (#)/date key.
- Memory non-zero indicators.
- Overflow indication.
- Automatic constant in multiply or divide.
- Right-justified entries and results.
- Leading zero suppression.
- 2 key rollover operation.
- Internal oscillator and power-on clear.

DESCRIPTION

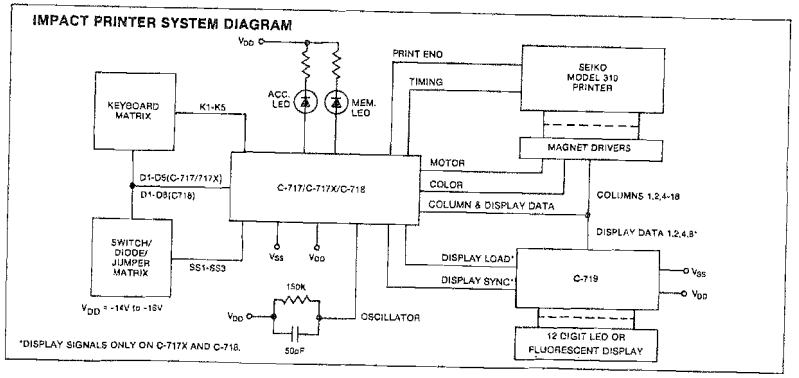
The C-700 Series is a growing family of circuits for the printing calculator manufacturer which provide the capability for a broad-based, multi-feature business calculator product offering. The C-700 Series currently includes four different calculator circuits (the C-716, C-717, C-717X and C-718) and two printer-display interface circuits (C-719 and C-720), each described on the following pages of this section.

DOT MATRIX PRINTER SYSTEM DIAGRAM



FUNCTION	DESCRIPTION	PART NUMBER	PACKAGE	FEATURES
8 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, and other features. Interfaces with the Olivetti Pu1100 dot matrix printer. Option for use with thermal printing version of Pu1100	C-716	40 DIP	Accumulator and 4 key memory
12 DIGIT PRINTING	Basic 4 functions and percent, automatic constant in multiply and divide, repeat add/subtract, decimal select mode, memory-in-use indicator, rounding options, non-add (#)/date key, and other features. Interfaces with the Shinshu Seiki Model 310 impact printer.	C-717 C-717X	40 DIP	Accumulator and Grand Total Memories.
		C-718		Accumulator, item counter, and four-key independent memory.
PRINTER-DISPLAY INTERFACE	Adds display capability to the C-717X and C-718 printing calculator circuits	C-719	28 DIP	For both LED and flourescent displays.
	Adds display capability to the C-716 printing calculator circuit.	C-720		

IMPACT PRINTER SYSTEM DIAGRAM



*DISPLAY SIGNALS ONLY ON C-717X AND C-718.

8 Digit / 5 Function Matrix Printer Calculator Circuit with Accumulator and Independent Memory

FEATURES

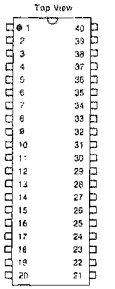
- 8 digit printout plus 2 full reight justified audit trail columns and floating sign.
- Automatic accumulating memory.
- Four-key independent memory.
- Arithmetic operation in add/subtract sequences, algebraic in multiply/divide (business logic).
- Decimal select modes: full floating; fixed point (0,1,2,3,4,5,6,7,8); add mode(automatic decimal 2 in + and −)
- Keyed decimal select.
- Automatically set to decimal 2 at power-on.
- Full floating accuracy on intermediate results in chain operation.
- Multistage keyboard buffer stores up to 6 keyed entries to allow uninterrupted operation during print.
- All other features listed on the General Information page.

DESCRIPTION

The C-716 is a single MOS/LSI circuit containing all the logic functions required to implement a five-function general purpose printing calculator with accumulator and a four-key independent memory. The C-716 has been designed to operate with the Olivetti Pu 1100 matrix printer with 50 dots in each horizontal row arranged in 10 groups of 5. Two of the ten groups are used to form the negative sign and the audit trail symbol. An option allows the C-716 to be used with the thermal printing version of the Pu 1100.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

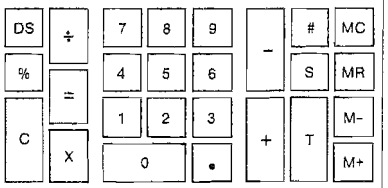


Not yet defined.

KEYBOARD SWITCH MATRIX

	D0	D1	D2	D3	D4	D5	D6	D7
K0	C/CE	0	1	2	3	4		
K1	×	÷	=	%	#	DS		
K2	+	−	S	T	M+	M−	MR	MC
K3			5	6	7	8	9	•

TYPICAL KEYBOARD ARRANGEMENT



DECIMAL SECTION

The C-716 features keyed decimal selection, a two key sequence of the DS key and a second key as in the following chart:

KEYS	•	0	1	2	3	4	5	6	7	8	9
DS	ADD MODE	0	1	2	3	4	5	6	7	8	FLOAT-ING

12 Digit / 5 Function Impact Printer Calculator Circuits with Acumulator and Grand Total Memory

FEATURES

- 12 digit printout plus 2 full right-hand justified audit trail columns.
- Automatic accumulating memory (stores group totals).
- Grand total memory.
- Selectable memory modes: normal (last entry printed); (running subtotal printed); GT (grand total memory access).
- Fully arithmetic operation.
- Decimal select modes: full floating; fixed point (0-6); add mode (with hardwired secondary add mode option for quantity × dollars).
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Multistage keyboard buffer stores up to 8 keyed entries to allow uninterrupted operation during print.
- C-717: printer only.
  C-717X: printer and display (with the C-719 interface chip).
- All other features listed on the General Information page.

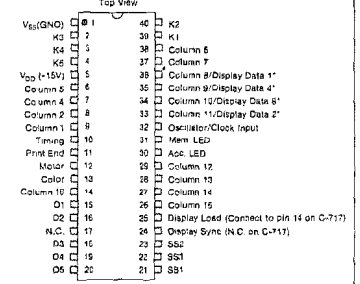
DESCRIPTION

The C-717 and C-717X are each single MOS/LSI circuits containing all the logic functions required to implement a five-function, two memory general purpose business calculator using a Seiko Model 310 impact printer. While both the C-717 and C-717X are pin-compatible with each other, the C-717X additionally provides signals for use with the C-719 printer-display interface chip. This allows the addition of a 12-digit fluorescent or LED display to the basic printer.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



*NOTE.
On the C-717X, pins 33-36 are multifunction pins with both display data and column 2-11 data. On the C-717, these pins are single-function, containing only column 8-11 data.

KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5
K1	0	5	00	.	=
K2	1	6	000	+	%
K3	2	7	=+	−	*
K4	3	8	=−	×	◊
K5	4	9	# DATE	÷	C/CE

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5
SS1	DECIMAL SELECT - SEE BELOW				
SS2			ADD MODE OPTION		PRINTER ON/OFF
SS3	◊ MODE	GT MODE	PAPER ADVANCE	TRUNCATE	ROUND OFF

DECIMAL SELECT CHART

The decimal select switch is a four-pole switch with encoded outputs during D1 thru D4 strobe periods. In the chart below, a '1' denotes a switch closure.

DECIMAL POSITION	D1	D2	D3	D4
+	1	1	0	1
F	1	0	0	1
0	1	0	0	0
1	0	1	0	0
2	1	1	0	0
3	0	0	1	0
4	1	0	1	0
5	0	1	1	0
6	1	1	1	0

12 Digit / 5 Function Impact Printer Calculator Circuit with Accumulator, Item Counter and Independent Memory

FEATURES

- 12 digit printout plus 2 full right-hand justified audit trail columns.
- Switch-selectable automatic accumulation.
- Three digit item counter.
- Four-key independent memory.
- Arithmetic operation in add/subtract sequences, algebraic in multiply/divide (business logic).
- Decimal select modes: full floating; fixed point (0-6, excluding 5); add mode (automatic decimal 2 in + and −, unit/price mode in ×).
- Non-coded decimal select switch input.
- Rounding options (truncate, 5/4 round off, 1/0 round up).
- Separate clear-all key
- Full floating accuracy on intermediate results in chain operation
- Multistage keyboard buffer stores up to 6 keyed entries to allow uninterrupted operation during print.
- Display capability (with the C-719 interface chip).
- All other features listed on the General Information page

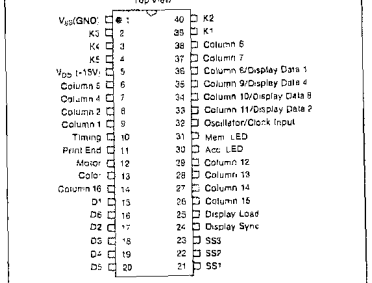
DESCRIPTION

The C-718 is a single MOS/LSI circuit containing all the logic functions required to implement a five-function general purpose consumer calculator with an accumulator, item counter and four-key independent memory. The C-718 has been designed to operate with a Seiko Model 310 16 column impact printer. When used with the C-719 printer-display interface, the C-718 also provides a 12-digit display capability, using either fluorescent or LED displays.

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



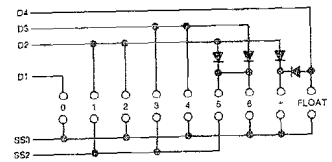
KEYBOARD SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
K1	0	5	00	N	=	C/CE
K2	1	6	.	+	%	M+
K3	2	7	=+	−	*	M−
K4	3	8	=−	×	◊	M*
K5	4	9	# DATE	÷	CA	M◊

STATIC SWITCH MATRIX

	D1	D2	D3	D4	D5	D6
SS1	Σ		PAPER ADVANCE	TRUNCATE	5/4 1/0	PRINTER ON OFF
SS2	DECIMAL SELECT - SEE BELOW					EXT. POINT
SS3						

DECIMAL SELECTION



C-719

Printer-Display Interface Circuit

FEATURES

- Adds display capability to C-717X and C-718 printer chips.
- Full 12 digit display capability.
- Drives LED or fluorescent displays.

DESCRIPTION

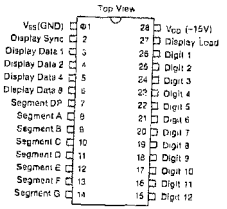
The C-719 is a single MOS/LSI circuit designed to add a 12 digit display capability to General Instrument's C-717X and C-718 printer calculator circuits. Data from the printer calculator chips is transferred to the C-719 interface chip serially and reformulated to drive seven segment multiplexed common cathode displays.

The segment and digit outputs of the C-719 are open-drain and have a breakdown voltage of −30 Volts to enable the driving of fluorescent displays with a minimum of interface components. LED displays may also be driven by the C-719 with direct drive of the segments and the addition of digit-drive buffers.

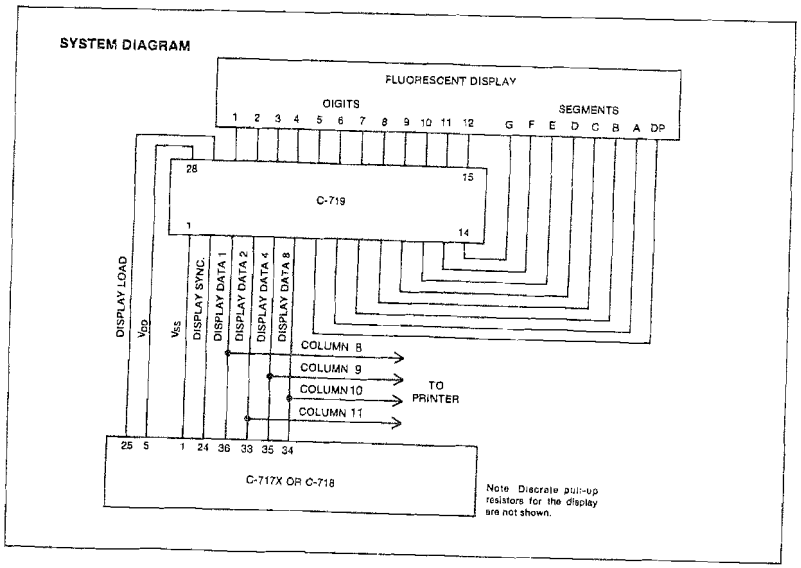
In the display, leading zeroes are suppressed and entries and results are right-justified.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



C-720

PRELIMINARY INFORMATION

Printer-Display Interface Circuit

FEATURES

- Adds display capability to the C-716 printer chip.
- Full 8-digit display capability
- Drives LED or fluorescent displays.

DESCRIPTION

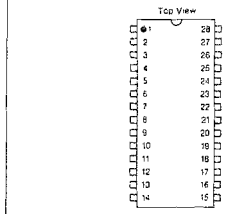
The C-720 is a single MOS/LSI circuit designed to add an 8 digit display capability to General Instrument's C-716 printer calculator circuit. Data from the printer calculator chip is transferred to the C-720 interface chip serially and reformulated to drive seven segment multiplexed common cathode displays.

The segment and digit outputs of the C-720 are open-drain and have a breakdown voltage of −30 Volts to enable the driving of fluorescent displays with a minimum of interface components. LED displays may also be driven by the C-720 with direct drive of the segments and the addition of digit-drive buffers.

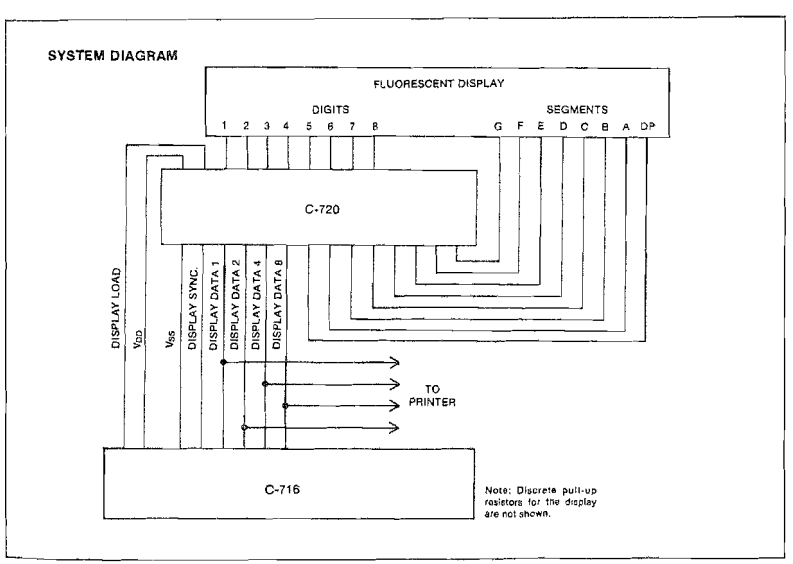
In the display, leading zeroes are suppressed and entries and results are right-justified.

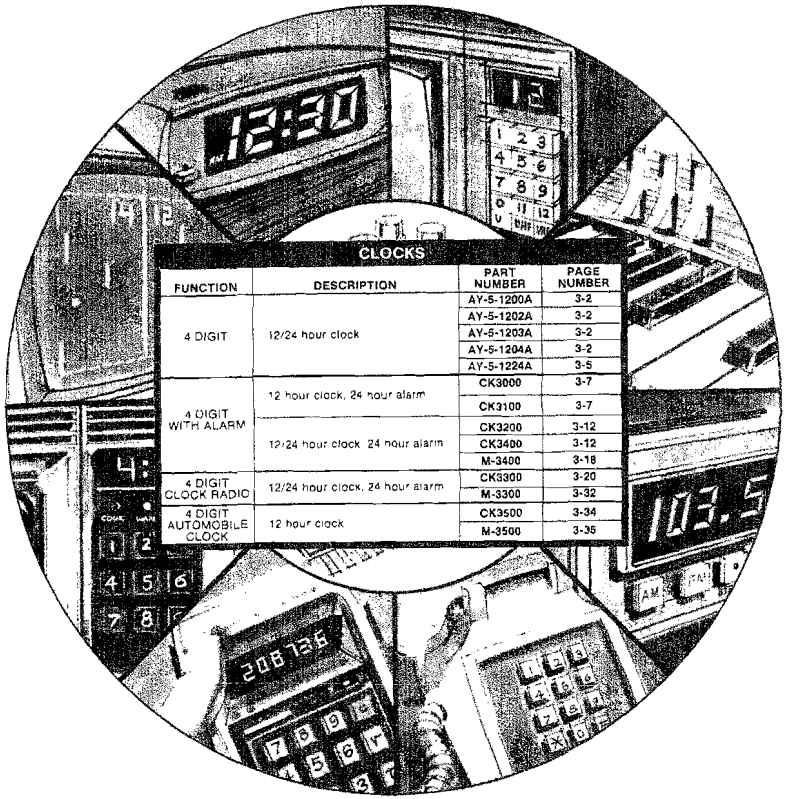
PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM





CLOCKS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
4 DIGIT	12/24 hour clock	AY-5-1200A	3-2
		AY-5-1202A	3-2
		AY-5-1203A	3-2
		AY-5-1204A	3-2
		AY-5-1224A	3-5
4 DIGIT WITH ALARM	12 hour clock, 24 hour alarm	CK3000	3-7
		CK3100	3-7
	12/24 hour clock 24 hour alarm	CK3200	3-12
		CK3400	3-12
		M-3400	3-18
4 DIGIT CLOCK RADIO	12/24 hour clock, 24 hour alarm	CK3300	3-20
		M-3300	3-32
4 DIGIT AUTOMOBILE CLOCK	12 hour clock	CK3500	3-34
		M-3500	3-36

CLOCKS

MICRO ELECTRONICS

4 Digit Clock Circuits

FEATURES

- Hours and minutes display.
- 12/24 hour operation.
- 50/60Hz operation.
- High voltage direct Fluorescent drive Outputs.
- Flashing seconds output (option)
- BCD output (option).
- Leading Zero Blanking (option).
- Power-On Reset to zero.
  (Counting does not start until time is set.)
- Options:

	7 Seg	BCD	Zero Blank	Flashing Sec
AY-5-1200A	Yes	No	Yes	No
AY-5-1202A	Yes	No	Yes	Yes
	No	Yes	No	Yes
AY-5-1204A	Yes	No	No	Yes

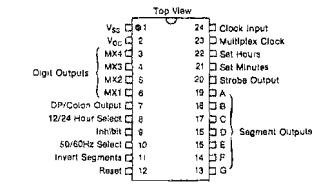
DESCRIPTION

The AY-5-1200A Series are P-Channel MOS integrated circuits, containing all the logic necessary to make a 4 digit, 12 or 24 hour clock, operating from 50 or 60Hz. High voltage output stages capable of driving fluorescent displays are provided

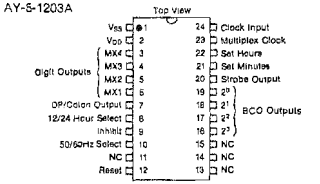
PIN CONFIGURATION

24 LEAD DUAL IN LINE

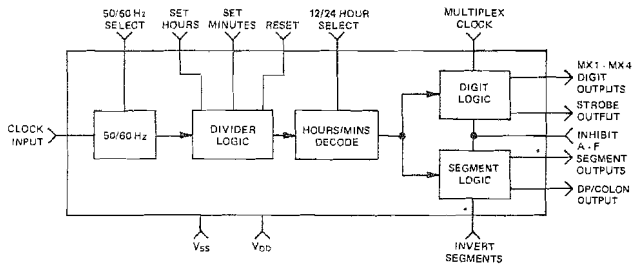
AY-5-1200A/AY-5-1202A/AY-5-1204A



AY-5-1203A



BLOCK DIAGRAM



* Not included in the AY-5-1203A. Four BCD outputs are provided in place of the seven segment outputs

PIN FUNCTIONS

Name	Function
Segment Outputs A—F	In 7 segment mode the digits are multiplexed on to these pins. These outputs are at logic '0' to display (positive) and will drive Fluorescent displays directly. In BCD mode outputs A to D are used, the code for 0 being 0000
DP/Colon Output	This is a high voltage output intended to drive a decimal point or colon. It is enabled during the MX3 time slot and can flash once per second if required
Multiplex Outputs MX1—MX4	These outputs select the display digits sequentially, they will drive Fluorescent displays directly. Five multiplex time slots are generated the fifth one being blank. Minutes are output in MX1 time, 10's of hours in MX4 time
Reset Input	When taken to logic '0' the clock is reset to zero.
Set Minutes Input	When taken to logic '0' the minutes counter is advanced at the rate of 2 min. per sec. and the hours counter at the rate of 2 hours per minute.
Set Hours Input	When taken to logic '0' the hours counter is advanced at the rate of 2 hours per second.
50/60Hz Select Input	When taken to logic '0', 60Hz operation will result
12/24 Hours Select Input	When taken to logic '0', 12 hour operation will result.
Invert Segments Input	When taken to logic '0' the segment outputs will be inverted.
Multiplex Oscillator	An external capacitor is used to select the multiplex frequency. If required the pin can be driven by an external oscillator.
50/60Hz Input	The master clock is input to the pin. Hysteresis is provided so that the input waveform is not critical.
V_{SS}	Positive Supply.
V_{DD}	Negative Supply
Inhibit Input	When taken to logic '0' all outputs are switched OFF.
Strobe Output	This is a short pulse occurring during the middle of each multiplex period.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Multiplex outputs).	+0.3 to -35V
Operating Temperature Range.	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation at +70°C Ambient—Total	500mW
Per Output	50mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -17V ± 10% (AY-5-1200A/1202A/1204A)
V_{DD} = -11.4V to -19V (AY-5-1203A)
Operating Temperature (T_A) = 0°C to +70°C

NOTE:
In the chart below, numbers in ( ) refer only to the AY-5-1203A.

Characteristic	Min.	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	
Clock input logic '0'	+0.5	—	-2(-1)	Volts	Note 1
Clock input logic '1'	-8	—	V_{DD}	Volts	
Multiplex clock frequency	DC	—	50	KHz	Note 2
Control inputs logic '0'	+0.3	—	-1.5(-1)	Volts	
Control inputs, current logic '0'	—	100	—	μA	Note 3
Control inputs logic '1'	-6	—	$-V_{DD}$	Volts	
Segment Outputs					
ON current	2(1.3)	—	—	mA	V_{OUT} = -2V
OFF leakage	—	—	5(10)	μA	V_{OUT} = -25V(-19V)
	—	—	10	μA	V_{OFF} = -35V
Multiplex Outputs					
ON current	5(3.3)	—	—	mA	V_{OUT} = -2V
OFF leakage	—	—	5(10)	μA	V_{OUT} = -25V(-19V)
	—	—	10	μA	V_{OFF} = -35V
Supply Current	—	8.5(6.5)	14	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. The clock input pin may be taken positive with respect to V_{SS} provided that the current is limited to 100μA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. These inputs have a 170Kohm pull up resistor to V_{DD}.

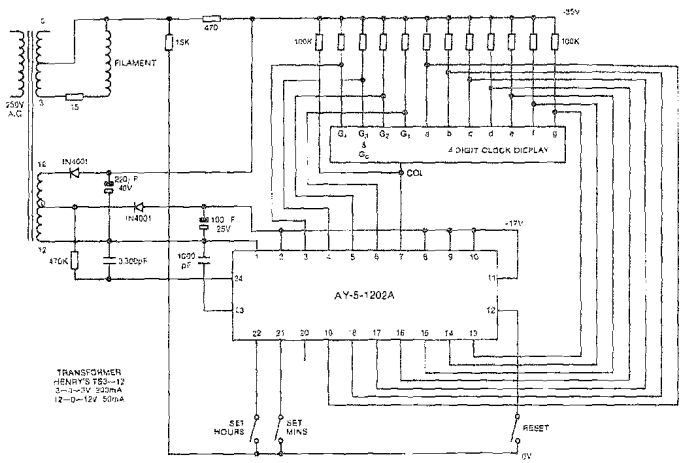


Fig.1. DIGITAL CLOCK CIRCUIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01

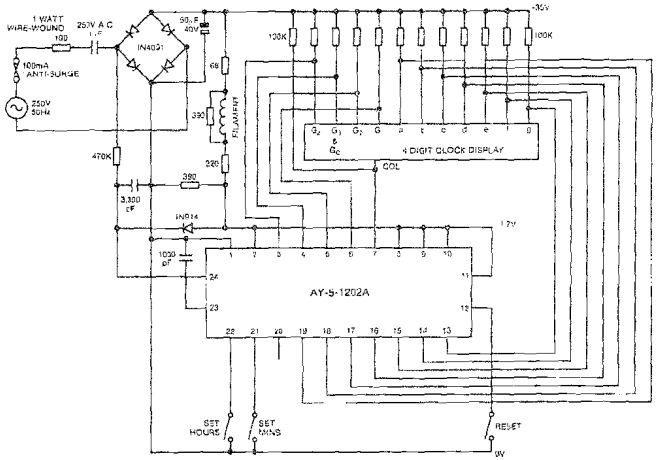


Fig.2. DIGITAL CLOCK CIRCIT USING AY-5-1202A WITH FUTABA FLUORESCENT DISPLAY 5-LT-01 AND CAPACITIVE POWER SUPPLY

4 Digit Clock Circuit

FEATURES

- 12/24 hour operation.
- Leading zero blanking in 12 hour mode.
- 50 or 60 Hz clock input.
- Hours and minutes display (4 digits).
- 7 segment outputs direct LED drive or TTL compatible BCD outputs.
- Complement control for segment outputs.
- Interdigit blanking for gas discharge displays.
- On chip multiplex oscillator.
- Single 15V supply.
- Power-On Reset to zero. (Counting does not start until time is set.)

DESCRIPTION

The AY-5-1224A is a P channel MOS integrated circuit containing all the logic necessary to make a 4 digit 12 or 24 hour clock operating from a 50 or 60Hz input. It has multiplexed BCD or 7-segment outputs and will drive LED, Fluorescent and Gas discharge displays with the minimum of interfacing.

PIN FUNCTIONS

Pins 1 and 11 are multifunction. During multiplex times 1 to 4 they function as data outputs, either 7 segment code or BCD according to the display mode selected. During multiplex time 5 (Strobe) they function as inputs.

Segment Outputs A-G (Pins 1 and 11 to 16)
In 7 segment mode the digits are multiplexed out on to these pins. Normally the outputs are at logic '0' (positive to display). Inter-digit blanking for ¼ the digit time is incorporated for gas discharge displays.

BCD Outputs 2^0—2^3 (Pins 1, 16, 15, 14)
In BCD mode the digits are multiplexed on to these pins in BCD code. Normally the outputs are at logic '0' (positive), i.e. code 0=0000.

Multiplex Outputs 1-4 (Pins 10, 9, 8, 7)
These pins are successively switched to logic '0' to select appropriate digit display. A fifth multiplex time (Strobe) is used to enable the control inputs. These outputs have interdigit blanking. The multiplex rate is 1/20th the multiplex clock frequency.

Strobe Output (Pin 6)
This pin is used to enable the control input keyboard, it goes to logic '0' to enable.

Set Hours Input (Pin 1)
When taken to logic '0' during strobe time this input causes the hours counter to advance at the rate of 1 hour per second.

Set Min Input (Pin 15)
When taken to logic '0' during strobe time this input causes the minutes counter to advance at the rate of 1 per second and the hours counter to advance at the rate of 1 hour per minute.

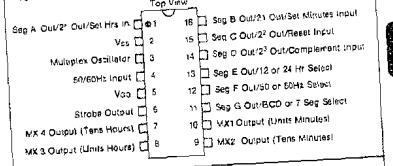
Reset Input (Pin 15)
When taken to logic '0' during strobe time this input causes the clock to reset to zero.

Complement Input (Pin 14)
When left open the segments and BCD outputs will have normal polarity. When connected to Strobe output via a diode the 7 segment and BCD outputs will be inverted.

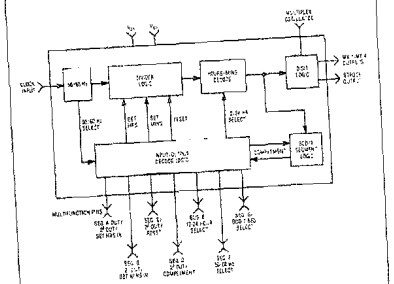
PIN CONFIGURATION

16 LEAD DUAL IN LINE

Top View



BLOCK DIAGRAM



12/24 Hour Select (Pin 13)
When left open the clock will run in the 12 hour mode. When connected to strobe via a diode 24 hour operation will result.

50/60Hz Select (Pin 12)
When left open a 50Hz clock will be accepted. When connected to strobe via a diode 60Hz operation will result.

BCD/7 Segment Select (Pin 11)
When left open 7 segment outputs will be provided, when connected to strobe via a diode BCD outputs will be provided.

50/60Hz Input (Pin 4)
The master clock (50 or 60Hz) is input to this pin. Hysteresis is provided on the input so that the input wave form is not critical.

Multiplex Oscillator (Pin 3)
An external capacitor is used to set the multiplex frequency. If required this input can be driven by an external oscillator.

V_{SS} (Pin 2)
Positive supply line nominally 0V.

V_{GG} (Pin 5)
Negative supply line nominally -15V.

Power-On Reset
At power-on the chip is reset to zero. Counters will not start until Set Hours or Set Minutes has been activated.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS}	+0.3 to −20V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation at 70°C Ambient—Total	500mW
Per Output	50mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

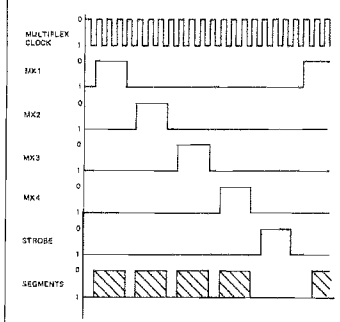
V_{SS} = 0V
V_{GG} = −12 to −18V
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input frequency	DC	50/60	—	Hz	—
Clock input logic '0'	+0.5	—	−2	Volts	Note 1
Clock input logic '1'	−8	—	V_{DD}	Volts	—
Multiplex Clock Frequency	DC	—	50	KHz	Note 2
Interdigit Blanking	—	150	—	µS	at 6.67 KHz Note 3
Control inputs logic '0'	+0.3	—	−1.5	Volts	—
Control inputs logic '1'	−6	—	V_{DD}	Volts	—
Outputs Logic '0'	—	—	500	Ohms	V_{OUT} = -2V, I_{OUT} = 4mA
Outputs Logic '1' (Leakage)	—	—	10	µA	V_{OUT} = −18V
Supply Current	—	—	10	mA	V_{GG} = -15V

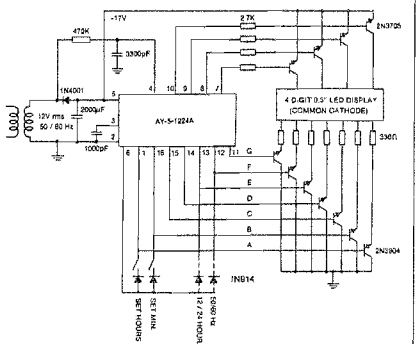
**Typical values are at +25°C and nominal voltages.

NOTES.
1. The clock input pin may be taken position with respect to V_{SS} provided that the current is limited to 100µA. The input will behave like a forward biased silicon diode in this condition.
2. The frequency is determined by an external capacitor.
3. At 6.67KHz multiplex frequency the digit ON time is 450µS and the OFF time is 150µS.

TIMING DIAGRAMS



AY-5-1224A WITH 0.3" LED DISPLAY



4 Digit Alarm Clock Circuits

FEATURES

- 12 Hour clock, 24 Hour alarm setting
- AM/PM indication
- 50 or 60 Hz operation
- Snooze (Sleep-over) alarm
- Direct display driving
  - CK3000 - Plasma
  - CK3100 - LED
- No display interface components
- Seconds flashing colons
- Alarm, set, and snooze indication
- Power interrupt indication
- Low current consumption
- Alarm output tone - direct drive with magnetic speakers
- Wake output for appliance switching(CK3100)

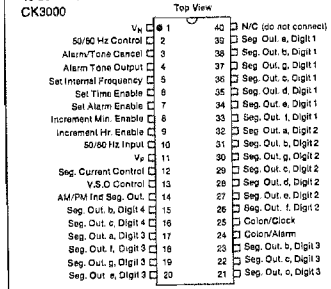
DESCRIPTION

The CK3000 and CK3100 are N-Channel MOS integrated circuits, containing all the logic necessary to produce low cost 4 digit alarm clocks operating from 50 or 60 Hz line frequencies. The output stages of these circuits have been designed specifically to directly driva the cathodes of Plasma displays (CK3000) or the cathodes of large digit common anode L.E.D.'s (CK3100) with no interface electronic components whatsoever.

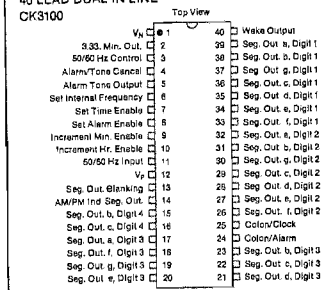
These integrated circuits also contain all the logic needed for contact noise elimination and line frequency noise rejection reducing further support components.

PIN CONFIGURATION

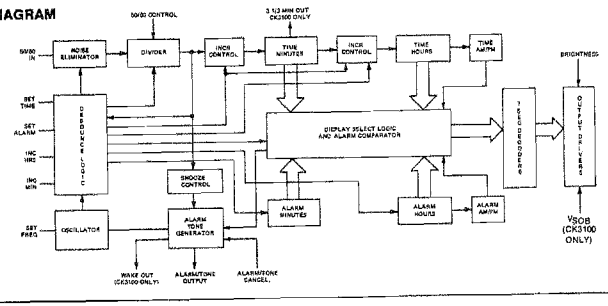
40 LEAD DUAL IN LINE
CK3000
Top View



40 LEAD DUAL IN LINE
CK3100
Top View



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The block diagram shows diagramatically the various logical function blocks that make up the CK3000 and CK3100 integrated circuits. The various units have the following functions.

Oscillator

The oscillator provides two basic functions in the integrated circuit.

1. Provides a suitable frequency in the audio range for modulating an external transducer at and during the alarm time (nominally 1 KHz).
2. Provides a strobe frequency for strobing the 50 or 60 Hz line frequency into a 'D' type flip flop to statistically eliminate line noise (nominally 250 Hz).

Debounce Logic

The logic here is used to eliminate contact noise closure on any input line and this is achieved using one second digital one shots in combination with 250 Hz strobe pulses. e.g. with the set-time or alarm enable inputs at logic zero the increment inputs are looking for one contact closure in each one second period. Any further closures are ignored. However if any increment pin is at logic zero and the set alarm set time switch is open and closed multiple counting will result. This logic also directs increment signals to the appropriate counters.

Divider

The divider counts down the line frequency counts to one per second depending on the 50/60 Hz control.

Snooze Control

This logic stores the information that an alarm compare has been reached, and initiates a 5 minute counter, which then runs continuously until such time that on an exact multiple of five minutes if the alarm/tone control switch is at zero, it will then stop and reset the alarm compare store. During the 5 minutes the alarm tone is made active for 1 minute in each five, producing a 1 Hz moduleted 1 KHz tone. If when the alarm tone is active the alarm tone cancel is taken to logical zero the tone will cease until the next five minute period.

50/60Hz Control

For 50 Hz operation - Connect to V_P or leave open circuit
For 60 Hz operation - Connect to V_N

Alarm/Tone Cancel - Tone Output

For normal operation the alarm cancel input is left open circuit. Under this condition any coincidence between the time and alarm store will cause the tone to output on alarm tone pin. This tone will remain present for one minute unless cancelled by momentarily connecting alarm cancel to a logical '0'. This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of tone cancel to a logic '0', thus providing a snooze facility.

To completely cancel the alarm sequence, the coincidence of the alarm cancel pin being at a logical 0 and the start of the next alarm tone period is required. Immediately after this occurrence the alarm cancel input may be open circuited and the alarm will be re-enabled for the following day.

Alternatively if either the set time or set alarm inputs are connected momentarily to a logical '0' after the first minute of alarm, the alarm logic will be re-triggered for the next day.

The alarm tone is a nominal 1 KHz square wave chopped by a 1 Hz square wave.

Frequency Set

An external resistor to V_P and external capacitor to V_N are used to control the frequency of the oscillator. These values should be selected to ensure appropriate 4 KHz oscillation.

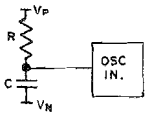


Fig.1

Typical Values for 4KHz:
R = 680K
C = 2200pF
for V_P = 15V

Figure 3 shows frequency vs. capacitance and resistence for nominal supply voltage.

Figure 4 gives a guide to component values for different V_P values.

With the oscillator set to 4KHz, the alarm tone output will be 1KHz, and the internal antibounce logic is strobed at 250 Hz.

Setting Up Procedure (Pins 6 thru 9)

In the normal clock running condition pins 6 thru 9 should be open circuit or at a logical '1'.

To enter set mode either set time or set alarm should be pulled to logical '0'. Under this condition the increment minutes and increment hours inputs are enabled and when either is pulled to a logical '0' then the corresponding hours and minutes will increment at a 1 Hz rate. All minutes to hours carries are suppressed while time is being set.

When set alarm is at a logical '0' the contents of the alarm store are displayed.

When set time/increment minutes occurs, the clock is stopped and remains stopped with the seconds reset until set time is open circuited or returned to a logical '1'. This enables the clock to be easily synchronized to an independent time source. No other setting conditions interrupt the seconds.

50/60Hz Input

This input accepts a line frequency signal at either 50 or 60 Hz and is subsequently used as the basic count time base.

Segments Output Control (Brightness) - CK3000

All output steges consist of a three device cascade configuration of which one device controls the output voltage current characteristics. (See Fig. 7.) From the characteristics it will be seen that a wide range of operating conditions are possible, allowing operation in either the resistive region (V proportional to I) or the constant current region. (I independent of V). Note that during device operation 24 of the 26 available segments can be on simultaneously, so in setting the device operating point it is important that each output stage does not exceed (on an average basis) one twenty fourth of the peak allowable package dissipation. i.e. approximately 20 mW per output.

It is also important that the display V-I load characteristic does not interrupt the avalanche region of the output device characteristic or off segment glow will be observed or in the limit device malfunction or damage can occur.

The output stages and control brightness were designed to be used with half line cycle anode voltage and a corresponding half cycle control of brightness to ensure the display is: (a) Off during segment data changes, and (b) To allow current to turn off and on in display gradually. Which will result in almost a total absence of R.F.I.

Segments Output Control (Blanking) - CK3100

Due to the high current handling capabilities of the output stages of this I.C., it is not possible to control the output V.I. characteristic by using a second series device. To regulate the display to the required brightness several options are possible externally and the following internally. The segment output control can turn off the display at any time by taking this input to a logical '0'. It is possible therefore to use half or full wave rectified signal on this display anode and prematurely shut the display down in each line cycle to control the conduction angle hance, average light output, using this control pin in phase relationship to the anode wave form.

Stand Off Voltage (VSO) — CK3000

The voltage on this pin influences the voltage current characteristics of the segment drives, its prime purpose is to enable the segment outputs to withstand more than 30 volts. Any voltage from 5 volts to V_P will ensure that 45 volts can be withstood through a plasma tube off-segment. For ease of operation it is suggested that V.S.O. is connected to V_P.

AM/PM Indicator

This output is an additional segment driver which can be used to give AM/PM indicator. (voltage current characteristic as other segments).

Cathode (Segment) Output Drivers (Pins 15 thru 39) — CK3000

All these pins drive the cathodes of the display without any additional interface components. These outputs are designed to withstand higher voltage signals than the other outputs. The output characteristics of the segment drivers can be controlled by pin 12 (See Figs.7 and 8).

Cathode (Segment) Drivers (Pins 15 thru 39) — CK3100

The output drivers of the CK3100 have sufficient current handling capabilities to drive even the most inefficient of today's available L.E.D.'s.

The output characteristics of the segments are shown in (Fig.5). Note: It is recommended that the package power dissipation be kept below 500mW, therefore, with a possible 24 simultaneous outputs being on together then each segment should be operated with an average power level of 21 mW or on average current of 15mA. The peak current for maximum number of segments condition (i.e. 24) should not exceed 40 mA per segment or the device will suffer permanent damage.

Colon Utilization (Pins 24 and 25)

Two colons show alarm/clock condition.

Clock	Alarm	Colon A	Colon B
Stopped/Setting	Don't care	Off	Off
Running	Set	1 Hz flash	1 Hz flash.
Running	Not set	1 Hz flash.	Off
Running	Snooze period	1 Hz flash*	1 Hz flash*

*colons flash alternately.

3.33 Minute Output — CK3100

This pin produces 3 pulses in each ten-minute period or 18 pulses per hour, and can be used for inputting to an external sleep counter, for clock radio type applications.

Wake Output — CK3100

This output turns "on" at the instance of alarm compare and stays on until the I.C. receives an alarm cancel signal. The wake output has been incorporated for appliance control, or clock radio applications. Output characteristics are shown in Figure 6.

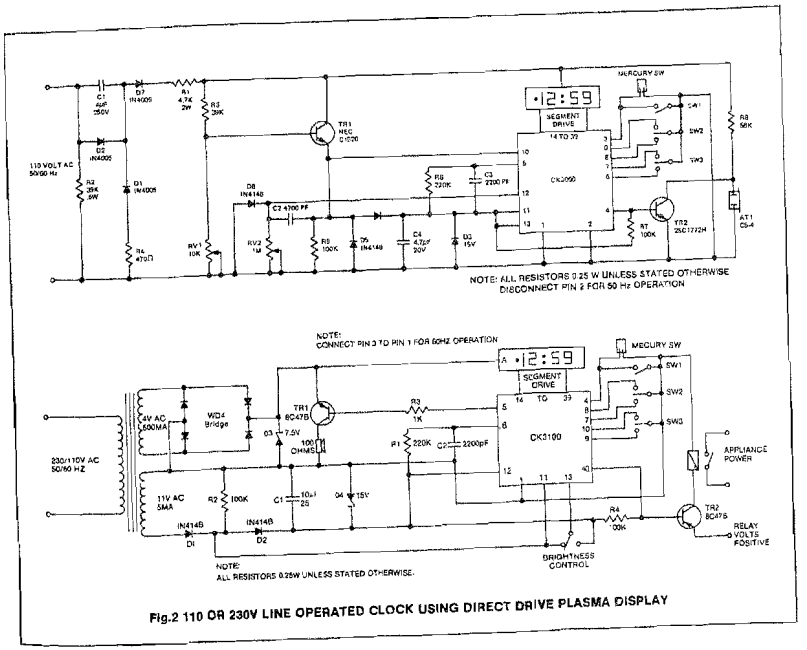


Fig.2 110 OR 230V LINE OPERATED CLOCK USING DIRECT DRIVE PLASMA DISPLAY

Maximum Ratings*

Voltage on any pin with respect to VN	0 to +25V
Voltage on Segment Output Pins	0 to +45V (CK3000-2)
Storage Temperature Range	−65°C to +150°C
Power Dissipation at 70°C	500mW
Operating Temperature	−25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$V_N = 0V$
$V_P = +7$ to $+18V$
$V_{SO} = +5$ to $+18V$ (CK3000)
Operating Temperature (T_A) = +25°C

CK3000

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input Frequency	DC	50/60	2500	Hz	Max. figure for test only.
Clock Input					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Oscillator Frequency (Fosc)	3.5	4	8	kHz	Set by external resistor and capacitor - See Fig.3
Control Inputs					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Outputs					
Alarm Tone					
'0' Level	20	-	-	mA	at $V_{OUT} = 3V$; $V_P = 15V$
'1' Level	-	-	10	µA	at $V_{OUT} = 15V$
Display Drive					
OFF Level	-	-	500	nA	$V_{OUT} = V_P = V_{SO} = 15V$; $V_{OUT} = 30V$
ON Level	2	-	-	mA	See Figs.7 & 8; $V_{OUT} = 5V$
Current	-	-	2.5	mA	Not including outputs

CK3100

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input Frequency	DC	50/60	2500	Hz	Max figure for test only
Clock Input					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Oscillator Frequency (Fosc)	2.5	4	6	KHz	Set by external capacitor and resistor - See Fig.3
Control Inputs					
Logic '0'	0	-	+1.0	V	
Logic '1'	0.7 V_P	-	V_P	V	
Outputs					
Alarm Tone					
'0' Level	20	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	0.7 V_P	-	-	V	Internal pull-up to V_P (approx. 5KΩ)
Wake Output					
'0' Level	20	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	-	-	10	µA	$V_{OUT} = V_P$
Display Drive					
'0' Level	20	-	-	mA	$V_{OUT} = 2.2V$; $V_P = 15V$
'1' Level	-	-	10	µA	$V_{OUT} = V_P$
3-1/3 Min. Output					
'0' Level	5	-	-	mA	$V_{OUT} = 3V$; $V_P = 15V$
'1' Level	0.7Vp	-	-	V	Internal pull-up (approx. 5KΩ)
Current	-	-	5	mA	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. Pins 2,6,7,8 and 9 have an internal pull-up resistor to V_P, value approximately 200KΩ. (CK3000)
2. Pins 3,4,6,7,8,9 and 10 have an internal pull-up resistor to V_P, value approximately 200KΩ. (CK3100)
3. Under no circumstances must any pin be biased temporary or permanently negative with respect to V_N or device operation will be affected.
4. No output pin during operation must exceed V_P transiently or operation will be affected.

TYPICAL CHARACTERISTIC CURVES

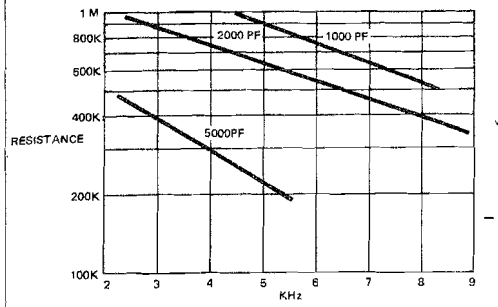


Fig.3 OSCILLATOR FREQUENCY VS. RESISTANCE/CAPACITANCE V_P = 15V

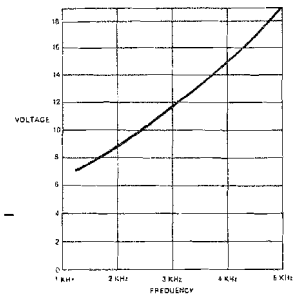


Fig.4 OSCILLATOR FREQUENCY VS. SUPPLY VOLTAGE (V_P) R-680K C = 2000 pf

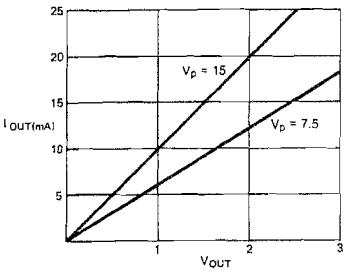


Fig.5 TYPICAL LED OUTPUT DRIVER

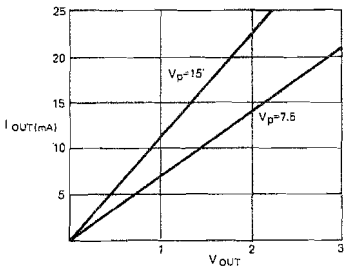


Fig.6 TYPICAL WAKE OUTPUT CURRENT CHARACTERISTIC FOR CK3000, CK3100 ALARM OUTPUT AND WAKE OUT FOR CK3100

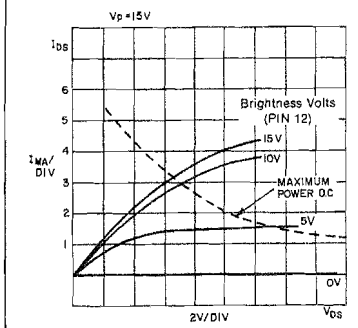


Fig.7

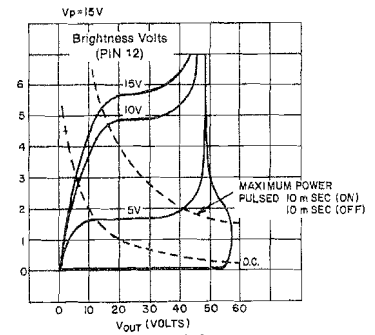


Fig.8

TYPICAL PLASMA OUTPUT DEVICE "ON" CHARACTERISTICS

4 Digit Alarm Clock Circuits

FEATURES

- 12 and/or 24 hour clock, 24 hour alarm setting
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- 50 or 60 Hz operation
- Snooze (sleep-over) alarm
- Direct display driving (two digit duplexing)
  CK3200 - Plasma
  CK3400 - LED
- No display interface components
- Seconds flashing colons
- Alarm, set, and snooze indication
- Line power interrupt indication
- Low current consumption

DESCRIPTION

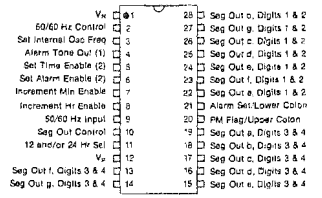
The CK3200 and CK3400 are N-Channel MOS integrated circuits, containing all the logic necessary to produce low cost 4 digit alarm clocks operating from 50 or 60 Hz line frequencies. The output stages of these circuits have been designed specifically to directly drive the cathodes of Plasma displays (CK3200) or the cathodes of large digit common anode L.E.D.'s (CK3400) with no interface electronic components whatsoever (Duplex mode).

These integrated circuits also contain all the logic needed for contact noise elimination and line frequency noise rejection reducing further support components. In order to overcome the extreme difficulties in eliminating radio frequency interference (common problem of multiplexed display clocks) and to keep the device in a low cost package a novel display driving technique is used - that of half line cycle anode duplexing. The duplex technique depends on the use of the two half sine-waves produced by two diodes placed across an a.c. supply where the common connection becomes the system reference.

PIN CONFIGURATION

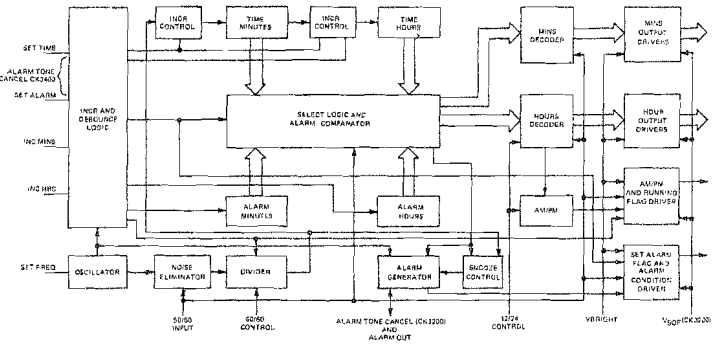
28 LEAD DUAL IN LINE

Top View



NOTES:
1. For CK3200, this pin is also alarm tone cancel.
2. For CK3400, either of these pins can be used as alarm cancel.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The block diagram shows diagramatically the various logical function blocks that make up the CK3200 and CK3400 integrated circuits. The various units have the following functions.

Oscillator
The oscillator provides two basic functions in this integrated circuit.

1. Provides a suitable frequency in the audio range for modulating an external transducer at and during the alarm time. (Nominally 1 KHz)
2. Provides a strobe frequency for strobing the 50 or 60 Hz line frequency into a 'D' type flip flop to statistically eliminate the noise. (Nominally 250 Hz)

Debounce Logic
The logic here is used to eliminate contact noise closure on any input line and this is achieved using one second digital one shots in combination with 250 Hz strobe pulses. e.g. With the set-time or alarm enable inputs at logic zero the increment inputs are looking for one contact closure in each one second period. Any further closures are ignored. However if any increment pin is at logic zero and the set time switch is open and closed multiple counting will result. This logic also directs increment signals to the appropriate counter.

Divider
The divider counts down the line frequency counts to one per second depending on the 50/60 Hz control.

Snooze Control
This logic stores the information that an alarm compare has been reached, and initiates a 5 minute counter, which then runs continuously until such time that on an exact multiple of five minutes if the alarm/tone cancel switch is at zero, it will then stop and reset the alarm compare store. During the 5 minutes the alarm tone is made active for one minute in each five producing a 1 Hz modulated 1 KHz tone. If when the alarm tone is active the alarm tone cancel is taken to logical zero the tone will cease until the next five minute period.

Duplex Display Driving
To use either CK3200 or CK3400 the display is connected in the following manner.

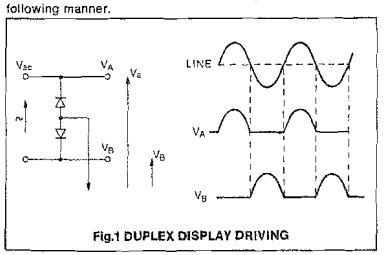


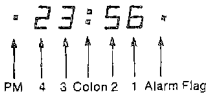
Fig.1 DUPLEX DISPLAY DRIVING

Segment	a	Digit 1 connected to segment	a Digit 2
	b		b
	c		c
	d		d
	e		e
	f		f
	g		g
Segment	a	Digit 3 connected to segment	a Digit 4
	b		b
	c		c
	d		d
	e		e
	f		f
	g		g

PM flag (indicator) segment connected to upper colon segment
Alarm setting flag segment connected to lower colon segment
Anode digit 1 connected to Anode digit 3
Anode PM indicator connected to Anode digit 4
Anode digit 2 connected to Anode digit 4
Upper colon anode connected to anode digit 3
Lower colon anode connected to anode digit 2
Alarm setting flag connected to anode digit 1

The anode can then be selected by the application of alternate half-cycle sine waves.

NOTE:
The phase of the incoming 50/60 Hz count to IC will then automatically deliver the correct segment data to display.

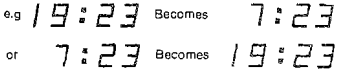


Anode phasing 50/60 Hz High = Digits 1 and 3 selected
Low = Digits 2 and 4 selected

DEVICE UTILIZATION

50/60 Hz Control
For 60 Hz operation Connect to V_{ss} or leave open circuit
For 50 Hz operation Connect to V_{dd}

12 And/Or 24 Hour Select
The IC has the ability to display the correct time in 12 or 24 hour mode under the control of the 12/24 select pin. Changing this pin from Logic '0' to '1' or '1' to '0' will immediately display the corrected time.
High i.e. '1' = 24 hour mode
Low '0' = 12 hour mode



No leading zero is shown in 24 hour mode.

For economy a single segment is employed which is illuminated in 12 hour time, during PM period.

Alarm Cancel & Alarm Tone Output - CK3200
In CK3200 (Plasma) the alarm tone output, alarm and tone cancel input uses the same pin for all three functions.

1. Alarm pin held to less than 1 volt (inputting a logic '0') alarm is not requested.
2. Alarm pin returned to positive supply through an appropriate resistance such that output is above 3 volts. (IC pulling approximately 1 mA) Alarm is requested.
3. At the alarm time this pin alternates between an open circuit condition and pulling 1 mA at the alarm tone rate.

(See Fig. 2 for typical external connections)

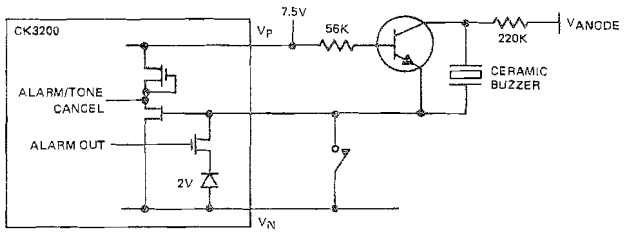


Fig.2 TYPICAL BUZZER CIRCUIT - CK3200

For normal operation the alarm cancel input is allowed to establish its own voltage (see Fig. 2). Under this condition any coincidence between the time and alarm store will cause the alarm tone to be output on this pin. This tone will remain present for one minute unless cancelled by momentarily connecting this pin to a logical '0' (less than one volt). This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of pin to logic '0' thus providing the snooze facility.

To completely cancel the alarm - snooze sequence, the coincidence of this alarm pin being at a logical '0' and the start of the next alarm tone period is required. Immediately after this occurence the alarm cancel input may be returned to the normal position and the alarm will be re-enabled for the following day.

Alternately if either the set time or set alarm inputs are connected momentarily to a logical '0' after the first minute of alarm, the alarm logic will be triggered for the next day.

Alarm Cancel & Alarm Tone Output - CK3400

In CK3400 the alarm output is on a dedicated pin (see Fig.3). Alarm cancel can be achieved by either taking set time or set alarm to a logic '0' during the post alarm time.

Tone cancel is achieved by a momentary connection to a logic '0' of both set time and set alarm simultaneously.

For normal operation the set time and set alarm input are left open circuit. Under this condition any coincidence between the time and alarm store will cause the alarm tone to output on the alarm tone pin. This tone will remain present for one minute unless cancelled by momentarily connecting both set time and set alarm simultaneously to a logical '0'. This tone will re-occur five minutes (and subsequent multiples of 5 minutes) after the original alarm time for a duration of one minute unless cancelled by momentary connection of set time alarm to a logic '0' thus providing a snooze facility.

To completely cancel the alarm sequence, either set time or set alarm pin is taken to a logical '0'. Immediately after this occurence the alarm will be re-enabled for the following day.

The alarm tone is a nominal 1 KHz square wave chopped by a 1 Hz square wave.

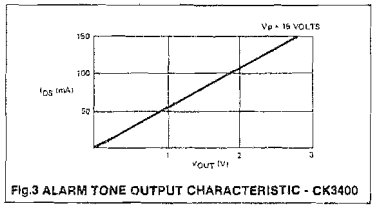


Fig.3 ALARM TONE OUTPUT CHARACTERISTIC - CK3400

Frequency Set

An external resistor to V_P and external capacitor to V_N are used to control the frequency of the oscillator. These values should be selected to ensure approximately 4KHz oscillation.

The following graphs give a guide to component values for different V_P values.

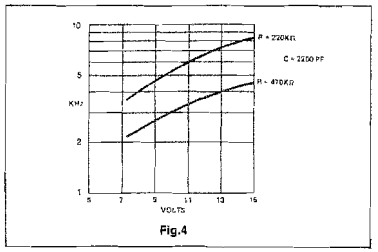


Fig.4

With the oscillator set to 4KHz, the alarm tone output will be 1KHz and the internal antibounce logic is strobed at 250 Hz.

Setting Up Procedure (Pins 6 Thru 9)

In the normal clock running condition, pins (6 thru 9) should be open circuit or at logical '1'.

To enter set mode either set time or set alarm should be pulled to logical '0'. Under this condition increment minutes and increment hours inputs are enabled and when either is pulled to a logical '0' then the corresponding hours or minutes will increment at a 1 Hz rate. All minutes to hours carries are suppressed while time is being sat.

When set alarm is at a logical '0' the contents of the alarm store are displayed.

When set time/increment minutes occurs, the clock is stopped and remains stopped with the seconds reset until set time is open circuited or returned to a logical 1. This enables the clock to be easily synchronized to an independent time source. No other setting conditions interrupt the seconds.

50/60 Hz Input

This input accepts a line frequency signal at either 50 or 60 Hz and is subsequantly used as the basic count time base.

Segments Output Control (Brightness) - CK3200

All output stages consist of a three device cascode configuration of which one device controls the output voltage current characteristics (see Fig.5). From the characteristics it will be seen that a wide range of operating conditions are possible, allowing operation in either the resistive region (V proportional to I) or the constant current region (I independent of V).

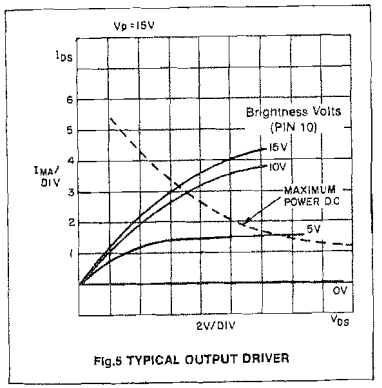


Fig.5 TYPICAL OUTPUT DRIVER

The output stages and control brightness were designed to be used with a half line cycle anode voltage and a corresponding half cycle control of brightness to ensure the display is

a. Off during segment data changes
b. To allow current to turn off and on in display gradually.

This will result in almost a total absence of R.F.I.

Segments Output Control (Blanking) - CK3400

Due to the high current handling capabilities of the output stages of this I.C., it is not possible to control the output V.I. characteristic by using a second series device. To regulate the display to the required brightness several options are possible externally and the following internally. The segments output control can turn off the display at any time by taking this input to a logical '0'. It is possible therefore to use half or full wave rectified signal on the display anode and prematurely shut the display down in each line cycle to control the conduction angle hence average light output, using this control pin in phase relationship to the anode wave form.

AM/PM Indicator

This output is an additional segment driver which can be used to give an AM/PM indicator. (Voltage current characteristic as other segments)

Cathode (Segment) Output Drivers - CK3200

All these pins drive the cathodes of the display without any additional interface components. These outputs are designed to withstand higher voltage signals than the other outputs. The output characteristic of the segment drivers can be controlled by pin 10. (See Fig.5)

Cathode Segment Drivers - CK3400

The output drivers of the CK3400 have sufficient current handling capabilities to drive even the most inefficient of today's available L.E.D.'s. The output characteristics of the segments are shown in Fig.5.

NOTE:

It is recommended that the package power dissipation is kept to below 500mW, therefore, with a possible 16 simultaneous outputs being on together, then each segment should be operated with an average power level of 31mW or on average current of 25mA. The peak current for the maximum number of segments condition (i.e. 16) should not exceed 60mA per segment or the device will suffer permanent damage.

It is also important that the display V-I load characteristic does not interrupt the avalanche region of the output device characteristic or off segment glow will be observed or in the limit device malfunction, or damage can occur.

Colon Utilization

Two colons (Pins 24 and 25) show alarm/clock condition.

Clock	Alarm	Colon A	Colon B
Stopped/Setting	Don't care	OFF	OFF
Running	Set	1 Hz Flash.	1 Hz Flash.
Running	Not set	1 Hz Flash.	1 Hz Flash.
Running	Snooze period	1 Hz Flash.	1 Hz Flash.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_N	−0.3 to +30 volts
Voltage on segment output pins	−0.3V to +45V
Storage temperature range	−65°C to +150°C
Power dissipation at 70°C	500 milliwatts
Operating temperature	−25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_N = OV
V_P = +10 to +18V
Operating Temperature (T_A) = +25°C

CK3200

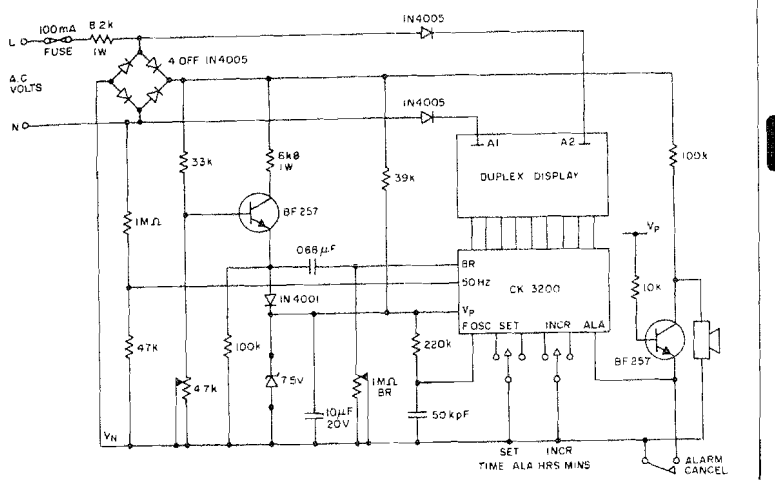
Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	DC	50/60	50,000	Hz	Max figure for test only
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_P$	—	V_P	V	
Oscillator Frequency (Fosc)	3	4	6	kHz	Set by external resistor and capacitor at V_P = 15V
Control Inputs					
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_P$	—	V_P	V	
Outputs					
Alarm Tone					
Cancelled	−0.3	—	0.3	V	Typ I sink = 3ma at > 2.5V
Tone	3	—	V_P	V	
Display Drive					
OFF Level	—	—	2	µA	V_P = 15 V, V_{OUT} = 45 Volts
ON Level	—	—	—	—	See Figs.4a-b-c
Current	0.4	—	3.0	mA	Not including outputs

CK3400

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	DC	50/60	50,000	Hz	Max figure for test only
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_P$	—	V_P	V	
Oscillator Frequency (Fosc)	3	4	6	kHz	Set by external resistor and capacitor at V_P15V
Control Inputs					
Logic '0'	0	—	0.8	V	
Logic '1'	$0.7V_P$	—	V_P	V	
Outputs					
Alarm Tone			40	µA	V_{OUT} = 0.3 Volts, Typ I sink = 3ma at > 2.5V
Display Drive					
OFF Level	—	—	10	µA	V_P = 15V, V_{OUT} = V_P
ON Level	—	—	20	mA	See Figs. 4a-b-c, V_{OUT} = 3 Volts
Current	0.4	—	3.0	mA	Not including outputs

**Typical values are at +25°C and nominal voltages.

Fig.6 TYPICAL APPLICATION



PRELIMINARY INFORMATION

Digital Clock Module

MODULE FEATURES

- CK3400 N-channel clock radio circuit
- LED display: 4 Digits plus colons
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation

CLOCK FEATURES

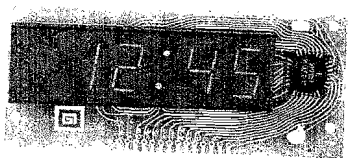
- Simple support electronics
- 5 minute repeating snooze
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)

DESCRIPTION

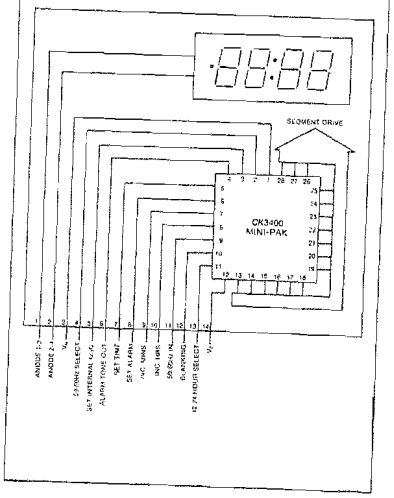
The M-3400 module contains a four digit LED display and a CK3400 LSI microcircuit featuring all the necessary logic, contact noise elimination circuits, control switching and timing circuits to implement simple-to-use, low-cost, multi-featured digital clocks. For full information on the many features of the CK3400 microcircuit, refer to the detailed descriptions and applications suggestions contained in the CK3400 product data sheet beginning on page 3-12.

The M-3400 module is fabricated on a single-sided printed circuit board measuring 1.500" × 3.930".

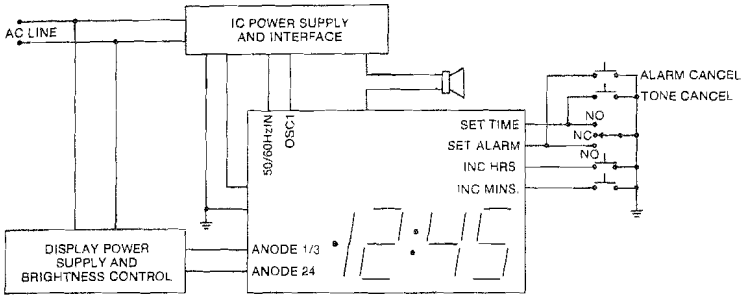
M-3400 MODULE



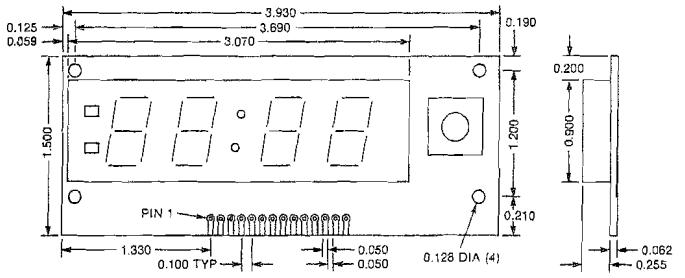
MODULE DIAGRAM



CLOCK SYSTEM DIAGRAM



MODULE OUTLINE



All dimensions in inches.
All dimensions nominal.

4 Digit Clock Radio Circuit

FEATURES

- 4 Digits plus colons
- LED direct duplex drive
- No display-IC interface components
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line Failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation (under 30 mW)

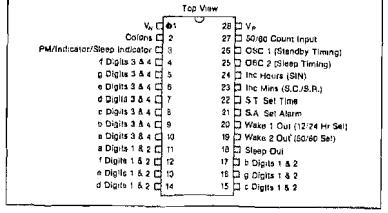
CLOCK RADIO FEATURES

- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 60 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)
- 5 minute pre-alarm applicance switching
- Automatic tape recorder control (record your favorite program automatically 0-120 minutes—starting from the exact second)

PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View



DESCRIPTION

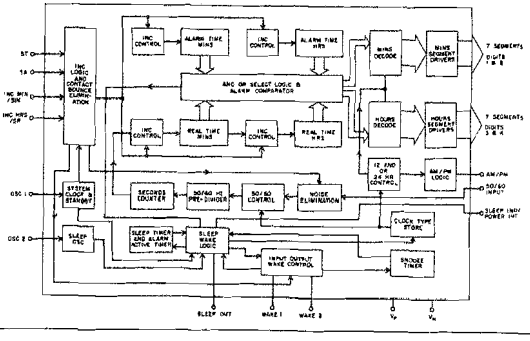
The CK3300 N-Channel MOS I.C. contains all the necessary logic, contact noise elimination circuits, control switching, segment drivers and timing circuits to implement simple-to-use, low cost, multi-featured clock radios.

Due to the extreme difficulties in eliminating R.F.I. in radios when used in conjunction with digital electronics a great deal of care has gone into the design of the L.S.I. to ensure that little or no R.F.I. problems are met by the clock radio designer. The largest R.F.I. problem in Display Driving has been solved using a novel technique—that of half-line cycle anode duplexing using the half-sine waves produced by two diodes, and ensuring that all segment data changes occur at the zero crossings of the line cycle. This technique allows brightness control to be achieved simply by resistively dividing down the line voltage with a potentiometer, or a simple two level scheme using a transformer tap.

Segment driving of the two groups is directly from the I.C. through 50 ohm switches which allow the high current peaks required of LEDs, up to one inch in size, while keeping the I.C. Power dissipation, for reliability, down to the 200 to 250 mW level.

The I.C. also contains many unique foatures which enable the equipment designer to put into the clock radio his company's own product image.

BLOCK DIAGRAM



PIN FUNCTIONS

V_N - (Pin 1)
Is the most negative power supply to the chip (0 volts).

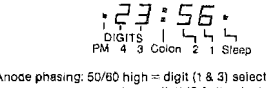
Segment Drivers (Pins 2-17)
These outputs are 50 Ω switches which drive the segments of common anode LED's directly. Their use and operation is as follows:

To use the CK3300 with LEDs, the LEDs must be of the COMMON ANODE TYPE, and connected in the following manner.

segment a digit 1 connected to segment a digit 2
segment b digit 1 connected to segment b digit 2
segment c digit 1 connected to segment c digit 2
segment d digit 1 connected to segment d digit 2
segment e digit 1 connected to segment e digit 2
segment f digit 1 connected to segment f digit 2
segment g digit 1 connected to segment g digit 2
segment a digit 3 connected to segment a digit 4
segment b digit 3 connected to segment b digit 4
segment c digit 3 connected to segment c digit 4
segment d digit 3 connected to segment d digit 4
segment e digit 3 connected to segment e digit 4
segment f digit 3 connected to segment f digit 4
segment g digit 3 connected to segment g digit 4

Colon 1 segment connected to colon 2 segment
PM indicator segment connected to sleep/power down indicator segment
Anode digit 1 to anode digit 3
Anode PM indicator to anode digit 4
Anode sleep indicator to anode digit 1
Anode colon upper to anode digit 3
Anode digit 2 to anode digit 4
Anode colon lower to anode digit 2

The anodes can then be selected by the application of alternate half-cycle sine waves derived from a transformer from the line The phase of the incoming 50/60Hz count to IC will then automatically deliver the correct segment data to the display.



Anode phasing: 50/60 high = digit (1 & 3) selected
low = digit (2 & 4) selected

Sleep Output (Pin 18)
This output turns on while the sleep counter is running and is indicated as active by an indicator in the display (Pin 3). This output turns on immediately following a sleep initiate and is cancelled either by sleep time being complete, a sleep cancel, an alarm comparison taking place, or an end of snooze period. This pin is also used as an input during circuit test to speed up testing.

Wake 2 Output/50-60 Hz Mode Select (Pin 19)
This output turns on at alarm compare time and stays on unless either an alarm cancel or a snooze repeat is activated.

If snooze repeat is activated this pin will go off until the next 5 minute period elapses when it will again turn on.

The snooze can be repeated indefinitely.

If the alarm is not cancelled this output will turn off 60 mins after the last snooze repeat re-triggering alarm for the next 24 hour period.

This pin is also the 50/60 Hz Select input during the time at which Set Time and Set Alarm are at a logic '1' (last data on this input when either Set Time or Set Alarm changes state is stored in an internal latch).

Wake 1 Output/12 Or 24 Hour Select (Pin 20)
This output turns on at alarm compare time and stays on uninterrupted until either:

a. An alarm cancel
b. 60 continuous minutes from alarm time
c. 60 continuous minutes from last snooze repeat

During the time that Set Time and Set Alarm are at a logic '1' together, this pin is the 12/24 hour select input.

The last data on this pin before a data change on Set Time or Set Alarm is stored internally in a latch, and defines 12 or 24 hour operation.

Set Alarm (Pin 21)
This pin, held at zero while Set Time is at a logic '1', enables the Increment Minutes and Increment Hours inputs to the alarm counter, such that each change of state (1→0) of the increment inputs will advance the appropriate counter by one unit.

Set Time (Pin 22)
Is identical in operation to the Set Alarm pin, but in this instance allows the counts to be entered into the time counter.

Taking both Set Time and Set Alarm to a logic '0' allows the Wake outputs to become active when the time reaches the alarm time. Returning either Set Time or Set Alarm to a logic '1' will cancel the alarm.

Increment Mins/Sleep Cancel/Snooze Repeat (Pin 23)
If Set Time or Set Alarm is at zero, this input provides one unit of increment for each logic transition from one to zero. (This input is de-bounced against switch noise). If both Set Time and Set Alarm are at a logic '1' or logic '0' and the sleep timer is running, a logic zero on this input will cancel sleep.

If both Set Time and Set Alarm are at e zero and the Wake outputs are active (i.e., post alarm time), then Wake 2 will be cancelled for a period of up to 5 mins when Pin 23 is taken to logic '0'. If this input is at zero when the alarm comparison takes place, then Wake 2 will stay off until 5 minutes have passed.

Increment Hours/Sleep Initiate (Pin 24)
If either Set Time or Set Alarm is at logic '0', this input provides one unit of increment to the required counter for each logic transition from 1 to 0. (This input is de-bounced against switch noise). If both Set Alarm and Set Time are at logic '1' or logic '0', this input will cause Sleep output to become active for the time resulting from current sleep oscillator frequency.

OSC 2 (Pin 25)
This pin produces a triangular wave oscillation depending on the value of resistance and capacitance. This oscillator is used to produce the sleep period by being gated internally with 160th of Osc 1 frequency (i.e. 50/60Hz).

Additionally connected to this pin is a low level detect circuit used with oscillator 1 for re-setting all internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used to detect that standby operation is required.

OSC 1 (Pin 26)
This pin produces a triangular wave oscillation depending on the external value of resistance and capacitance. The signal is used during normal operation to provide internally to the I.C. -

a. the internal timing for a series of one-shot gates
b. After division, the frequency to de-bounce other external pins via D-type latches. This frequency is further divided down to 50/60Hz and is used as the source frequency during standby operation.

Connected internally to this pin is a low level voltage detector which is used in conjunction with a low level voltage detector on Osc. 2 (pin 25) to reset all the internal logic to 12:00 in 12 hour mode and 0:00 in 24 hour mode. This low level detect is also used for test purposes.

50/60 Hz In (Pin 27)
This input is the normal source of timing. This input drives both the internal count and the alternate half line selection of the segment outputs.

For equal brightness in the display this input must have a 1:1 mark space ratio (±20%).

There is no necessity for eliminating line noise externally when providing this input signal as an internal arrangement eliminates undesired counts.

V_P (Pin 28)
Is the most positive power supply to the chip (typically 10 volts)

Pins 19, 20, 23 and 24 are dual function pins which operate as inputs or outputs dependent on the state of the Set Time and Set Alarm inputs:

S.T.	S.A.	INC MIN	INC HR	SC/ SR	SIN	Wake 1	Wake 2	50/ 60	12/ 24
1	1	-	-	*	*	-	-	*	*
1	0	*	*	-	-	-	-	-	-
0	1	*	*	-	-	-	-	-	-
0	0	-	-	*	*	*	*	-	-

*Operable - Not Operable

Set time (S.T.)	Pin 22
Set alarm (S.A.)	Pin 21
Increment minutes (inc min)	Pin 23
Increment hours (inc hrs)	Pin 24
Sleep cancel (S.C.)	Pin 23
Snooze repeat (S.R.)	Pin 23
Sleep initiate (SIN)	Pin 24
Wake 1	Pin 20
Wake 2	Pin 19
50/60Hz Select	Pin 19
12/24Hr. Select	Pin 20

Using Wake 1 Or 2—Input/Output Functions

When the Set Time (S.T.) and Set Alarm (S.A.) inputs are at logic one, the IC outputs Wake 1 and Wake 2 become inputs to two bistable gates which store the logic conditions on those pins: 50/60Hz Select on the Wake 2 pin and 12/24Hr. Select on the Wake 1 pin.

50/60Hz Select

Set Time or Set Alarm must be at zero before data on Wake 2 changes, or clock can change its 50/60 pre-divide mode. To avoid this, the following circuit is recommended:

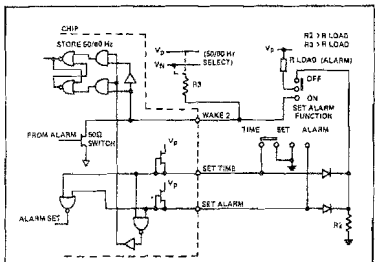


Fig.1 SUGGESTED USE OF WAKE OUTPUTS TO ENSURE PROPER OPERATION OF INPUT/OUTPUT FUNCTION

With the Set switch in the center position the set inputs are pulled up to a logic '1' by the IC, provided the Alarm switch is in the off position. The load (R load) will pull the junction of the two diodes and R2 to a logic '1'.

The output pin Wake 2 will either be pulled up or down depending on the connection of R3.

Changing of Set switch will pull down the appropriate input and not affect other external circuit conditions.

Change of position of alarm ON-OFF switch will allow R2 to pull down both Set inputs to zero before Wake 2 output is connected to load. This ensures that the internal IC latch is disconnected from wake line before data on wake line can influence stored data in latch.

12/24 Hr. Select

For the "Wake 1 output 12-24 hour select", changing the logic polarity will immediately change the displayed time from 12 hour mode to 24 hour mode or vice versa.

e.g. 21 : 56 becomes •9 : 56
or •9 : 56 becomes 21 : 56

No leading zero is shown in 24 hour mode:

12 : 32 in 12 hour time becomes 0 : 32 in 24 hour time

(Note: 12 to 24 hour displayed time change can only be achieved when the alarm is not requested and not in set mode)

For economy of LEDs a single dot is employed which is illuminated during the PM period in 12 hour time.

Time Setting

Four input pins (S.T., S.A., Inc Hr., Inc Mins.) are provided to enable the following four functions to be provided:

a. Setting the time
b. Setting the alarm
c. Stopping the clock
d. Starting the clock

For synchronizing purposes

S.T. = 0

Allows each depression of Inc Hrs to advance hrs by one count. Clock will stop on the first inc mins and will remain stopped until ST = 1, thus allowing synchronization. The device assumes that the hours may need to be changed without affecting mins, but assumes clock is incorrect if minutes are changed, thus stopping clock and re-setting internal seconds counter to zero.

S.A. = 0

Selects alarm time and, for each depression of Inc Hours, hours are advanced one and, for each depression of Inc Mins, minutes are advanced one.

NOTE:

No carries from minutes to hours occur during setting of time or alarm

Radio Control Inputs

The inputs S.T., S.A., Inc Min, Inc Hr. serve as radio control inputs under the following conditions.

S.T. And S.A.

At zero together - alarm is requested. S.T. and S.A. at logic one together - alarm not requested, but if taken to logic one during post alarm, alarm is cancelled.

S.T. and S.A. different will also cancel alarm if alarm is active.

S.T.	S.A.	Pre-Alarm	Post-alarm
1	1	Not required	Cancel
1	0	Not required	Cancel
0	1	Not required	Cancel
0	0	Requested	Alarm maintained for 80 mins

S.T., S.A. = 1

If S.T. and S.A. are at a logic 1 together during pre-alarm time, the following functions can be obtained using Inc Min - Inc Hrs inputs. Inc Hrs input going to logic zero for at least 20m secs will result in sleep output going to zero for the period of time set by sleep potentiometer.

At any time Inc Mins input (SC/SR) going to zero for at least 20m secs will cancel sleep timer if sleep output is active.

To reduce the number of knobs, switches, wiring etc., in the clock radio the following alternative feature is provided. If (S.C./S.R.) is wired to (SIN) a dual action is achieved, 1st depression of switch activates sleep, 2nd cancel sleep, 3rd re-activates etc. This allows features (a) if user decides he wishes radio off after he has been in bed for a few minutes, he pushes button, or (b) radio goes off automatically because sleep period has finished, but user is not asleep and would like radio to continue, so he presses button again.

S.T., S.A. = 0

In pre-alarm period the function performed when S.T., S.A. = 1 is identical. (When the alarm sounds at the requested alarm time the input (S.C./S.R.) (Inc Mins) becomes the 5 min snooze repeat input.)

At alarm, the effect of (S.C./S.R.) becoming zero for at least 20m secs is to turn Wake 2 output off until next 5 min interval, if again depressed, Wake 2 will turn off for a further 5 mins—this sequence will go indefinitely until S.T., or S.A. or both are returned to logic '1', cancelling alarm. If inputs to the device are left unchanged for 80 mins then alarm will re-set for 24 hours.

Again to improve the radio features and simplify radio operation the tied function of (S.C./S.R.) and (SIN) on one button performs the following three functions:

Initiate sleep (SIN)
Cancel sleep (S.C.)
Snooze repeat (S.R.)

Delaying Alarm by 5 Minutes

If, when Wake 1 output is capactively coupled to (S.C./S.R.) input then at alarm time Wake 1 will turn on and stay on but Wake 2 will immediately become cancelled, hence no alarm will be heard from radio until 5 minutes later; this allows an electrical appliance to be turned on 5 minutes prior to alarm sounding.

Use of Sleep Timer for Tape Recorder Control

If sleep input (SIN) in directly coupled to Wake 1 output, then a tape recorder or any electrical equipment can be turned on at alarm time using sleep output for a period of time set on sleep potentiometer.

Radio Control Outputs

There are three radio control outputs:

a. Wake 1
b. Wake 2
c. Sleep output

Function

1. Wake 1—goes at zero; i.e. is on at alarm time for a period of 80 mins or until an alarm cancel.

2. Wake 2 goes to zero at alarm time, and stays at zero until a snooze repeat is activated then it will stay off until next 5 minute point then return to zero, for a period of 80 mins unless snooze repeat is re-activated. Snooze repeat can be used indefinitely, until either a continuous 80 mins occurs or alarm is cancelled

Note: The 5 minute period is any 5 min interval from alarm time and not 5 min from each snooze repeat.

3. Sleep output goes low after a sleep initiate for the period of time set by sleep potentiometer. (Will be overridden by Wake if sooner.)

Colon Utilization

FUNCTION	COLON CONDITIONS BOTTOM	TOP
Set time	on	off
Set alarm	off	on
Stopped (Sync)	off	off
Run (alarm not requested)	1Hz	off
Run (alarm requested)	1Kz	1Hz
Snooze period	1Hz	1Hz

Sleep dot is on for sleep timer running, flashing for post line interrupt (removed from flashing by movement of S.T. or S.A. to '0')

Stand-By Operation

If a circuit is employed to change the IC power source to battery during line failure, e.g. two diodes, then if the external timing components of oscillator 1 are set to give 8KHz (nominally R = 120K Ω = 2200pF), then the IC will maintain operation to an accuracy of one part in 120, i.e., 30 secs/hr, during the failure. On return to main power the sleep indicator will flash at 1HZ to notify user that indicated time could be in error.

The standby condition is detected by the failure of oscillator 2 to oscillate, therefore oscillator 2 is connected to the line-derived power source, not the battery.

It is assumed OSC 2 input has gone to zero volts.

To remove flash condition take S.T. or S.A. momentarily to zero.

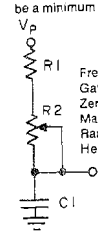
Analog Sleep Control

A second oscillator is provided on IC whose frequency can be controlled by an RC network. This oscillator is identical to oscillator one (Standby oscillator) and occupies the same silicon real estate location ensuring that process variations, temperature variations and voltage variations have as nearly as possible identical effects on frequency stability. Oscillator 1, which is set to 8KHz is divided down to 50HZ (20.0 m secs); and is used as a gating time for oscillator 2 (Sleep Timer Source). The number of gated counts is loaded in the sleep timer (capacity 160 counts) and subsequently counted up at one per minute until 160 is reached.

The range of sleep time is controlled by varying OSC 2 resistance. At 4:1 change in resistance will give variation of 160 to 40 gated pulses, this giving a sleep time of 0 to 120 minutes.

NOTE:

Minimum sleep time to ensure correct snooze operation should be a minimum of 5 minutes.



R1, C1 = 120K, 2200PF
R2 = 0 – 450K
Frequency range = 8kHZ – 2kHZ
Gate time = 20ms
Zero sleep counts = (20 x 10^{-3}) x (8 x 10^{3}) = 160
Maximum sleep counts = (20 x 10^{-3}) x (2 x 10^{3}) = 40
Range = 120 counts
Hence 1 count = 1 min

Fig.2

To initiate the sleep timer both S.T. and S.A. must logically be the same, and INC HR/SIN must be momentarily at zero. (See later section).

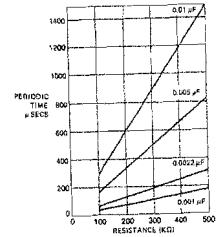


Fig.3 OSCILLATOR CHARACTERISTICS FOR V_P = 10V

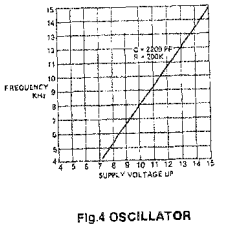


Fig.4 OSCILLATOR CHARACTERISTICS WITH VOLTAGE

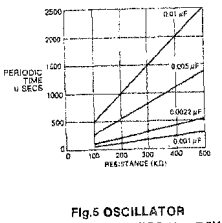


Fig.5 OSCILLATOR CHARACTERISTICS FOR V_P = 7.5V

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

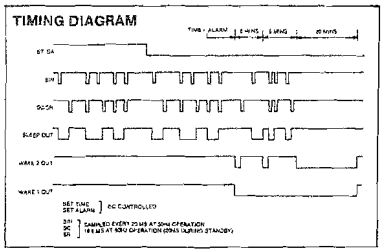
Voltage any pin with respect to V_n ..... +20V
Storage temperature ..... -65°C to +150°C
Operating temperature ..... -20°C to +70°C
Lead temperature (soldering 10 sec) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Characteristic	Min	Typ**	Max	Units	Conditions
Power Supply Voltage	6	10	18	Volts	V_n = 0V
Supply Current	—	2	—	mA	
50/60HZ Input					
Frequency (must be identical to anodes)	0	50/60	50,000	Hz	V_p = 10V
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Inputs (Excl Oscillators)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Segments Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	µA	
Wake 1, 2, Sleep Out (on)	—	30	—	mA	V_{OUT} = 1.5V
(off)	—	10	—	µA	
Wake 1, 2 (As Inputs)					
Logic '1' level	0.6Vp	—	Vp	Volts	
Logic '0' level	0.0	—	0.7	Volts	
Oscillators 1 and 2					
Hi level	—	5.5	—	Volts	Free run
Lo level	—	3.5	—	Volts	
Reset Level	—	—	0.7	Volts	

Unless specified otherwise, characteristics are defined with V_p = 10V at T_A = +25°C.
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Under no circumstances during IC operation must any pin either input or output be taken to a voltage more negative than V_n or IC malfunction will occur
2. No input or output must be taken to a positive voltage greater than 20 volts or permanent damage can result
3. No output must be allowed to dissipate a continuous power in excess of 100mW.
4. Total chip continuous power dissipation must not exceed 500mW
5. The total current being returned to V_n through all device pins must not exceed 1 amp.



Input and Output Characteristics

INPUTS
S.A.
S.T.
INC HR (SIN)
INC MIN (SC/SR)
} Active pull up's to V_p Operate level logic '0' } 250KΩ

50/60HZ count input, active pull down
For correct operation duty cycle of 50/60Hz must be 1:1 ± 20%

OUTPUTS
Normally open circuit
Operate "on" (low impedance typically 50Ω)

INPUTS
Wake 1 - as input '1' = 12hr '0' = 24hr
Wake 2 - as input '1' = 60Hz '0' = 50Hz

CLOCK INPUT NOISE ELIMINATION TIMING
50/60Hz - strobed every 4ms internally for less than 1 µs

Testing I.C. Facilities

1. Master reset: This can be activated by pulling OSC1 (Pin 26) and OSC 2 (Pin 25) to zero volts together
2. Internal debounce and predivider logic may be bypassed if OSC 1 is taken to zero volts while OSC 2 is left running
   a. Under this condition Inc Hrs and Inc Mins pins are not debounced to allow fast incrementing for test purposes.
   b. Also in this mode the 50/60Hz input pin is directed straight to the main counters under control of the sleep pin. If Sleep pin at '0'—50/60Hz input clocks 120 minute sleep counter, and with Sleep at '1' it clocks the main minutes count by passing the debounce and divide by 50/60 counter. Under this condition it also clocks the 5 minute snooze counter.

Operation Clock Radio Example

(showing some features and their use) - ref Figs.21 and 22

Start-Up
Radio is connected to line for 1st time, then battery is inserted
Assume following switch position RADIO OFF, SET TIME SWITCH = RUN

Actions
Display will illuminate and read 12:00 sleep indicator will flash at 1Hz. Set clock as indicated previously (Flashing will cease)
In 24hr mode 0:00 will illuminate with flashing sleep indicator

Snooze Bar Action
IN RADIO OFF POSITION

1st button depression	Low volume radio (set required volume)
2nd button depression	Radio off
3rd button depression	Radio on low volume
4th button depression	Radio off

etc. .

IN RADIO ON POSITION
Radio comes on high volume (set wake volume required)

1st button depression	Low volume radio (mute facility)
2nd button depression	High volume
3rd button depression	as 1
4th button depression	as 2

Radio Auto
In auto, alarm is requested at "set alarm" time. If sleep is desired press button. Subsequent button pushes will have same effect as in radio "off" position.

Select Wake to Alarm Tone or Radio
Assume radio selected
At alarm time radio will come on at wake volume setting

1st button depression	Radio will switch to low volume
2nd button depression	Radio will switch off
3rd button depression	Radio back a low volume

If after first depression radio is left untouched, radio will return to wake volume after five minutes
If after 2nd depression radio is left untouched, radio will stay off for five minutes then return to wake volume
This wake volume, if left, will be maintained for 80 mins unless radio is returned to radio ON or radio OFF switch position, changing switch momentarily from auto to ON or OFF and back to auto will reset alarm and re-request for same time next day. The above, repeating snooze, can be maintained idenfinitely if button is pushed before 80 mins elapses
Note. 80 mins is timed either from alarm time, if untouched, or 80 mins from last button depression

Select Wake to Alarm Tone
The alarm tone or buzzer is obtained by placing positive feedback around the audio amplifier or radio in such a manner that the desired sound can be achieved and the feedback can be stopped by open circuit one point in the network
At alarm time buzzer will sound:

On 1st button depression	Buzzer will cease and radio will switch to low volume
2nd button depression	Radio and buzzer will be off

If after first depression radio is left untouched, radio will return to buzzer after 5 mins
If after 2nd depression radio is left untouched, radio and buzzer will be off and at 5 mins BUZZER WILL AGAIN SOUND
As for radio position - radio will reset after 80 mins for 24 hrs. At any time in buzzer sequencing, buzzer radio select can be changed over to radio, then the radio will alternate high-low volume with button. Cancelling in buzzer mode is identical to radio mode

Typical Application
To combine the S.A and S.T. functions to provide simple and rapid clock setting. It is suggested that the following is incorporated in the clock radio.
Two toothed wheels are placed over two seperate sprung contacts and coupled to two concentric rotating knobs, (say 12 teeth each) along side is a three position switch labeled 'set time, run, set alarm'
To set clock, select time or alarm and rotate Hrs knob, or mins knob, each click will result in one unit change of time, rapid rotation will result in 12 increments per revolution of knob.
The above procedure results in an easy to use system with the advantage over mechanical clocks of independent hrs and mins setting
NOTE:
No carries from mins to hrs can occur during setting of time or alarm

Use of Auto Tape
Fig.21 shows - the facility for automatically switching on an appliance (e.g. tape recorder) at a specific time and keeping appliance active for a period of time up to 120 mins. In this mode the wake output is made to start the sleep - timer at the wake time.

Use of 5 Min Delayed Alarm with Appliance Switching
In this mode of operation the wake 1 output is made to cancel the first alarm through the SC (inc hr) input such that radio or alarm time will only occur at the end of the first snooze period
This result in appliance being activated at set alarm time and after 5 mins the alarm or radio will sound

Fig.6 — shows a typical clock-radio block diagram
Fig.7 — shows the chip/display circuit

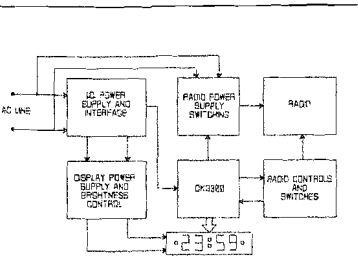


Fig.6

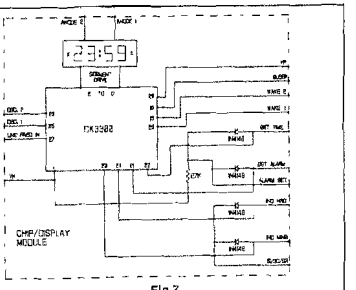


Fig.7

Interface with a Radio

There are many possible configurations of clock radios in use today and a wide range of different radio chassis are employed in these units. It is necessary therefore that the clock radio I.C. be sufficiently flexible to allow simple interfacing to be accomplished.

The following section gives different options, features and interfacing to demonstrate some of the approaches possible with the CK3300.

Power Supply Interface

To enable any existing line operated radio chassis to be used with the minimum of changes it is suggested that the following power supply is used with the adoption of a 2nd line transformer. This will (a) reduce the need for a change at the existing transformer. (It is unlikely that the existing transformer will be capable of providing the additional power required of the display).

a. Allow the electronic clock movement to be self contained therefore, keeping the interface wiring to a minimum.

b. Allow the same electronic movement to be used with several radio chassis.

Options

1. Without battery standby facility Fig.8
2. With battery standby facility Fig.9

Display Interface and Power Source

Four options are shown

1. No brightness control Fig.10
2. Day/night brightness (two level) Fig.11
3. Manual brightness control Fig.12
4. Automatic brightness control Fig.13

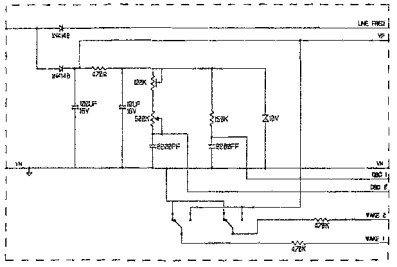


Fig.8 POWER SUPPLY INTERFACE WITHOUT STANDBY

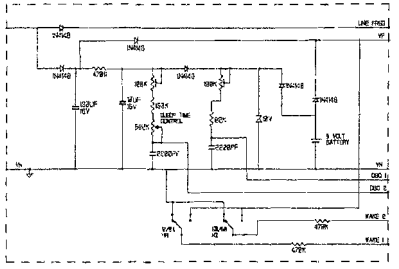


Fig.9 POWER SUPPLY INTERFACE WITH STANDBY OPTION

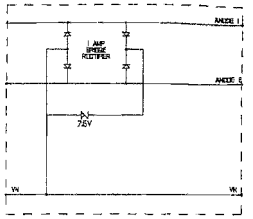


Fig.10 NO BRIGHTNESS CONTROL

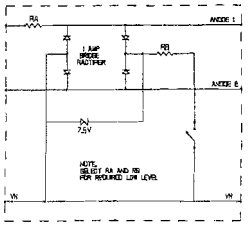


Fig.11 TWO LEVEL BRIGHTNESS CONTROL

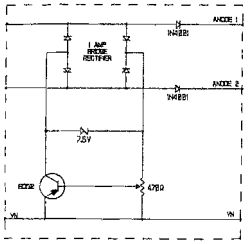


Fig.12 MANUAL BRIGHTNESS CONTROL

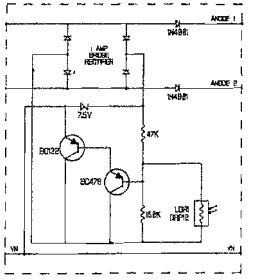


Fig.13 AUTOMATIC BRIGHTNESS CONTROL

Radio Switching

Option 1 Push button operation (Fig.14)
Option 2 Rotary switch operation (Fig.15)

Radio Powering

Option 1(Fig.16A, 16B) Direct audio amplifier control (no active components)
Option 2 (Fig.17) Power supply switching using Transistor
Option 3 (Fig.18) Power supply switching using a relay

Tone Generation

Option 1 (Fig.19) Saw tooth generation independent of radio
Option 2 (Fig.20) Sine wave generation independent of radio
Option 3 (Fig.15,16B) Sine wave using the existing radio audio amplifier

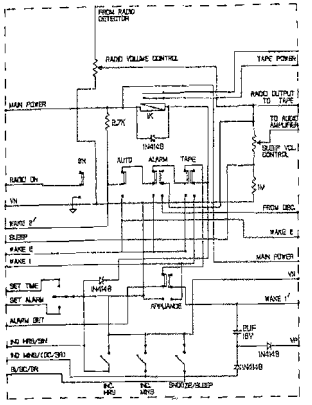


Fig.14 RADIO SWITCHING

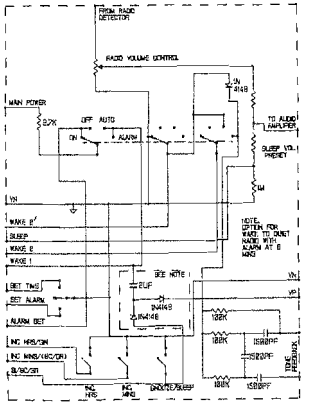


Fig.15 RADIO SWITCHING

Additional Facilities

1. Automatic tape recording (Fig.21)
2. Appliance switching with delayed alarm (Fig.21)
3. Wake to normal radio with 5 minute alarm over-ride (Fig.21)
4. Wake to quiet radio with 5 minute alarm over-ride (Figs. 21 and/or 22)
5. Radio muting during normal radio listening (Figs.21 and/or 22)

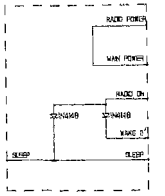


Fig.16a RADIO SWITCHING BY BIAS CHANGE

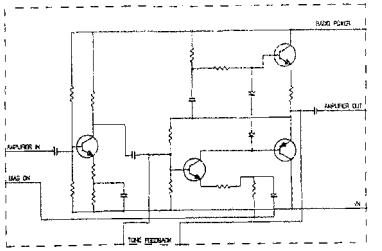


Fig.16b TYPICAL TRANSFORMERLESS AUDIO AMPLIFIER

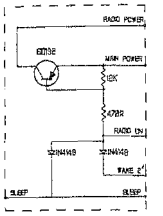


Fig.17 RADIO POWER SWITCHED BY TRANSISTOR

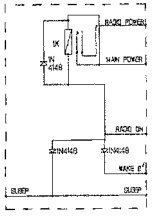


Fig.18 RADIO POWER SWITCHED BY RELAY

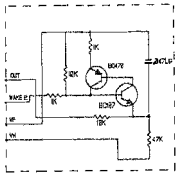


Fig.19 SAW TOOTH OSC

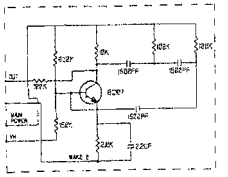


Fig. 20 SINE-WAVE OSC

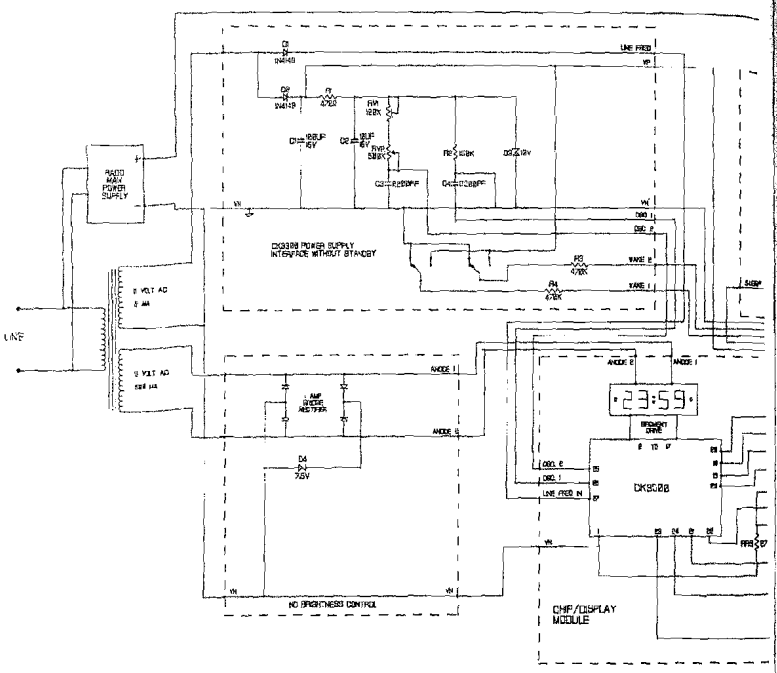


Fig.21(a) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

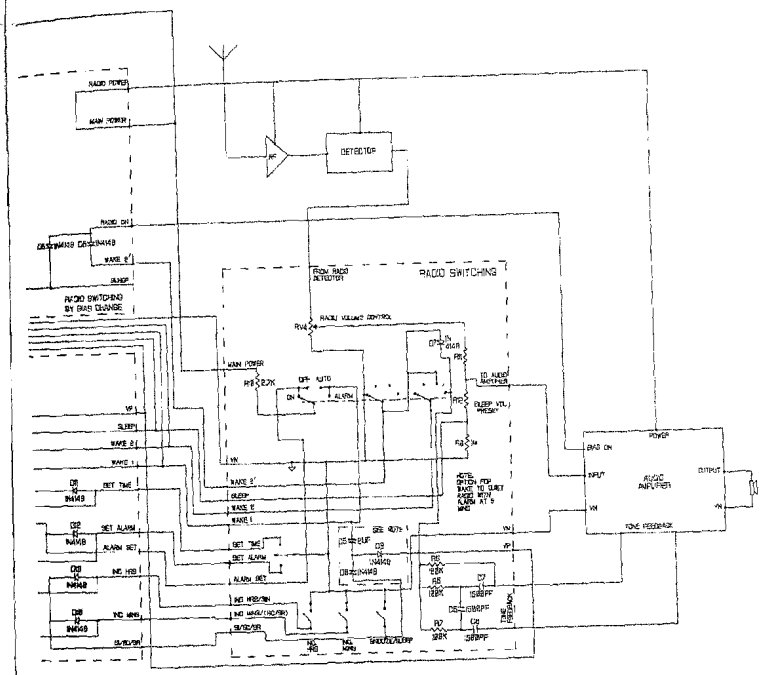


Fig.21(b) TYPICAL "BASIC" CLOCK RADIO CIRCUITRY

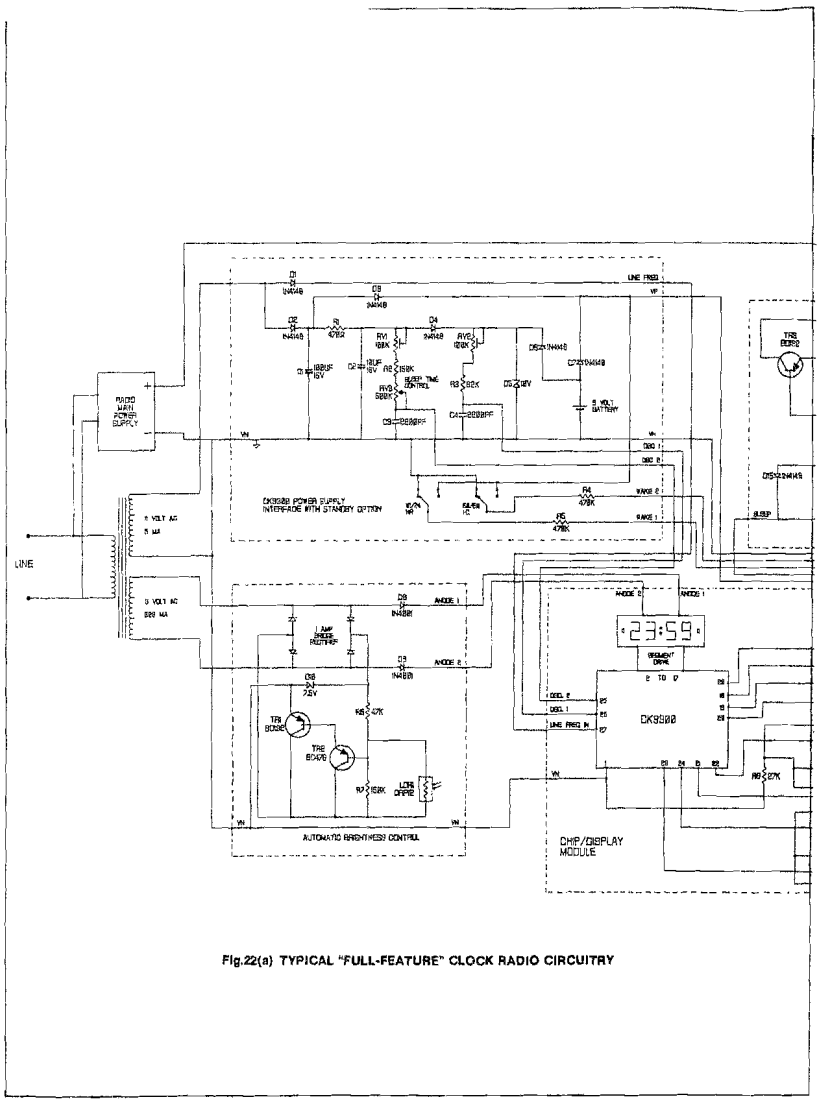


Fig.22(a) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

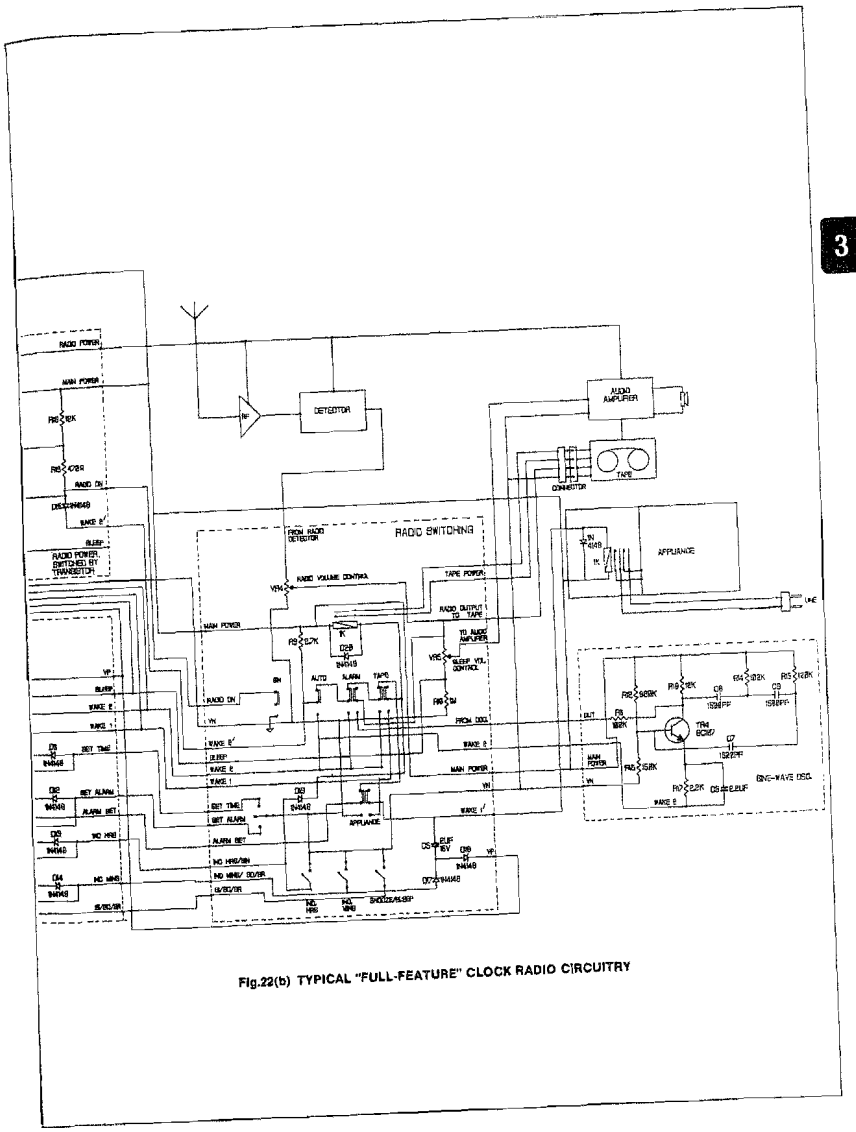


Fig.22(b) TYPICAL "FULL-FEATURE" CLOCK RADIO CIRCUITRY

Digital Clock Radio Module

MODULE FEATURES

- CK3300 N-channel clock radio circuit
- LED display: 4 Digits plus colons
- No radio frequency interference problems
- No external contact noise elimination circuits required
- No external line frequency noise rejection circuits required
- 12 or 24 hour display
- Leading zero suppression in 24 hour mode
- PM indication in 12 hour mode
- Alarm-snooze indicator
- 50Hz or 60Hz operation
- On-chip oscillator for standby operation with battery during line failure
- Line power interrupt indication
- Sleep operation indicator
- Low power dissipation

CLOCK RADIO FEATURES

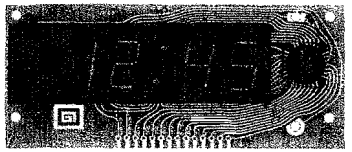
- Simple support electronics
- Analog sleep setting (user controlled 5 to 120 mins with 1 minute resolution). No necessity for daily adjustment
- Totally independent sleep and wake timing
- Independent volume of music during sleep and wake
- Radio sound muting during normal radio listening
- Wake to music or alarm tone
- Self-cancelling alarm after 80 minutes of wake
- 5 minute repeating snooze with radio and/or alarm
- Sleep override or sleep repeat
- Wake to alarm tone with quiet radio override (every 5 minutes) during snooze time (repeatable)
- Simple setting of time, alarm, and sleep
- Hold and synchronize capability for time setting
- Independent hours, minutes setting (carry propagation suppressed)
- 5 minute pre-alarm appliance switching
- Automatic tape recorder control (record programs automatically from 0-120 minutes—starting from the exact second)

DESCRIPTION

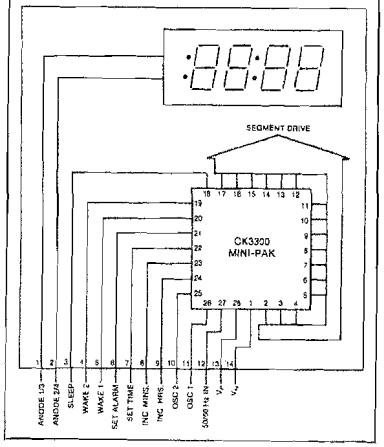
The M-3300 module contains a four digit LED display and a CK3300 LSI microcircuit featuring all the necessary logic, contact noise elimination circuits, control switching and timing circuits to implement simple-to-use, low-cost, multi-featured digital clock radios. For full information on the many features of the CK3300 microcircuit, refer to the detailed descriptions and applications suggestions contained in GI's CK3300 product data sheet.

The M-3300 module is fabricated on a single-sided printed circuit board measuring 1.500" × 3.930".

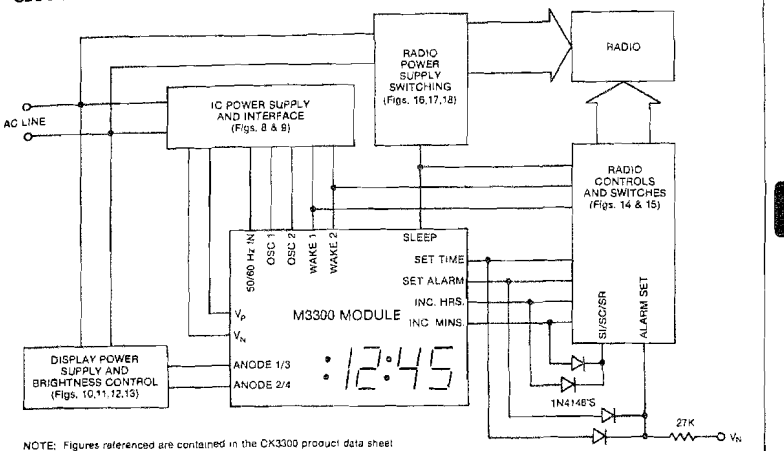
M-3300 MODULE



MODULE DIAGRAM

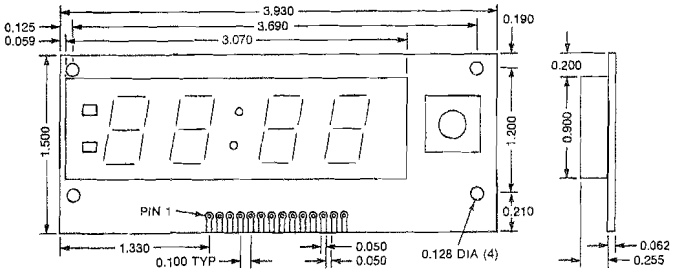


CLOCK RADIO SYSTEM DIAGRAM



NOTE: Figures referenced are contained in the CK3300 product data sheet

MODULE OUTLINE



All dimensions in inches.
All dimensions nominal.

4 Digit Automobile Clock Circuit

FEATURES

- Direct 20mA segment drive to 4 digits, two hours digits and two minutes digits.
- Timing designed for 3.58MHz color TV crystal.
- Two button setting of the time:
  1) Increment clock state
  2) Increment selected digit
- Four clock states:
  1) Set hours
  2) Set tens of minutes
  3) Set units of minutes
  4) Run
- Selected digit for setting flashes at 3.75Hz rate.
- Internal switch debounce.
- Clock resettable to 1:00.
- May be operated from a wide range of power supplies (Device is powered from a current source.)
- Can be driven from a 60Hz signal.
- Low power consumption (display off).
- Variable display intensity.

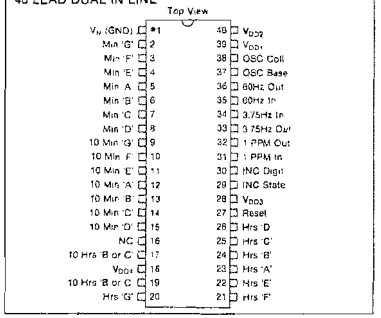
DESCRIPTION

The CK3500 is a bipolar LSI circuit utilizing General Instruments' I²L technology. The circuit contains an on-chip crystal oscillator and the logic to display hours and minutes in a 12-hour format. The time is set with two internally debounced switches. The chip also has direct LED segment drive capability, thus requiring a minimum of external components.

PIN CONFIGURATION

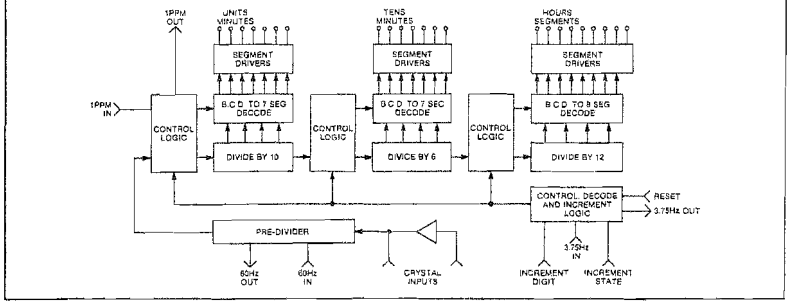
40 LEAD DUAL IN LINE

Top View



Two power connections are provided, one for the LED display drivers and one for the timekeeping function. With the display off, low power consumption is possible.

BLOCK DIAGRAM



PIN FUNCTIONS

Segment Outputs (23 pins) The segments of each digit are driven seperately. The outputs are open collector devices, and are "ON" when the segments to be displayed are selected.

V_{DD4} Positive supply to the decoders and segment drivers only (to conserve battery drain with ignition off).

V_{DD1}, V_{DD2}, V_{DD3} Positive supplies to the oscillator and count down circuits.

V_N Negative supply (normally ground).

Crystal Inputs (2 pins) Connection of external crystal (frequency source).

Increment Digit This input increments the selected digit by one for each depression of the digit increment push-button (i.e. each time inout is connected to V_{DD}).

Increment Clock State There are four clock states sequentially selectable for each consecutive depression of the increment state push-button (i.e. each time this input is connected to V_{DD}). The four clock states in order of access are as follows:

1. Set Hours
2. Set Tens of Minutes
3. Set Units of Minutes
4. Run

(NOTE: The sequence starts over with continued momentary connections of this input to V_{DD}).

Selected digits will flash at a 3.75Hz rate to indicate the clock state.

TIME SETTING OPERATION

Two switches are utlized for the time setting of the clock. They each apply a positive voltage to the appropriate pin on the chip. To describe their operation, suppose that the clock is running normally (in the RUN state). Closing the INC STATE switch causes the hours digit/digits to flash at a 3.75Hz rate. At this point, the INC DIGIT switch may be closed, causing the hours digits to increment one count each time the switch is closed. When the desired hours count is reached, the INC STATE switch is again closed, causing the tens of minutes digit to flash. Closing the INC DIGIT switch then increments the tens of minutes digit. When the desired digit is reached, the INC STATE switch is again closed, causing the units of minutes digit to flash. This digit is set as before, repeatedly closing the INC DIGIT switch. Finally, the INC STATE switch is again closed, placing the clock back in the RUN mode. When the RUN mode is entered and the units of minutes digit has been changed, the seconds are reset to zero, giving an exact minute count. In the RUN mode, closure of the INC DIGIT switch has no effect.

DISPLAY INTENSITY

When the LED is supplied from a voltage in the range of 2.5 to 5 Volts, the current into Injector 4 serves as an intensity control. For voltage over about 3.5 Volts, a resistor should be included in series with the display anode. The value should be 2.5 (V-2.5) ohms and will dissipate a maximum of 0.4(V-2.5) watts. This resistor serves to limit the chip dissipation to acceptable values.

ELECTRICAL CHARACTERISTICS

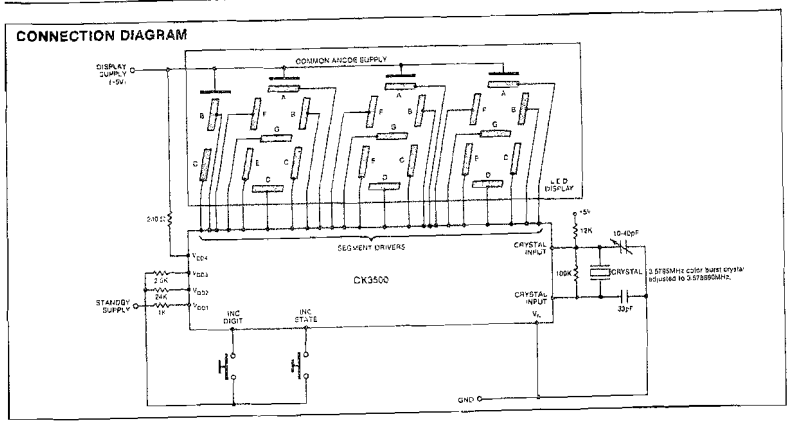
Maximum Ratings

Injector Voltage	0.55V to 0.9V
Injector Current	25mA
Input Current	10mA
Output Voltage	5.5V
Output Current: Display Drivers	20mA
Test Points	1mA
Storage Temperature	-55°C to +150°C
Operating Temperature	-20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Characteristics	Min	Typ	Max	Units	Conditions
Injector Current:					
I_{DD1}	2.5	3.0	25	mA	
I_{DD2}	.055	0.2	25	mA	
I_{DD3}	.75	1.5	25	mA	
I_{DD4}	—	10	15	mA	
Oscillator Supply	2	—	5	V	
Output Sink Current	—	—	20	mA	per segment
Switch debounce	—	50	—	ms	
Oscillator Frequency	—	3.579880	—	MHz	derived from crystal
Oscillator Beta	20	40	150	—	
Logic "1":					
Frequency Inputs	—	open	—	—	
Increment Digits/State 2	2	—	5	V	
Logic "0":					
Frequency Inuts	—	1.0	10	mA	
Increment Digits/State	—	open	—	—	

CONNECTION DIAGRAM



PRELIMINARY INFORMATION

Automobile Clock Module

MODULE FEATURES

- CK3500 I²L clock circuit
- LED display 4 Digits
- No external contact noise elimination circuits required
- All external components are contained on board
- Low power dissipation with LED's off
- Separate display supply line for dimmer control
- Two switches are only off board components
- Clock time source is a standard T.V. chroma burst crystal (on board)

DESCRIPTION

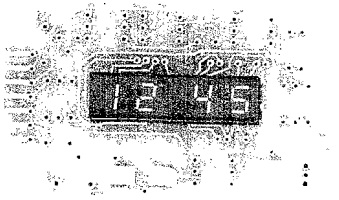
The M-3500 is a module which consists of the CK3500 I²L circuit with a four digit led display plus all other components on the P.C. board. The M-3500 is a self contained clock particularly useful in the auto clock market. The only external components necessary are the switches for setting time. It also has a separate display power line for dimmer control and saving power when display is not energized.

OPERATION

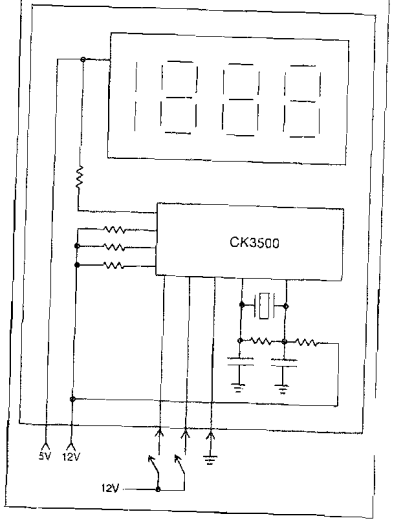
The M-3500 module is designed to operate at minimum battery current drain at all times in an automobile. Maximum current consumption is used when the display is on and this requires the ignition to be turned on. The following is a list of modes for normal operation:

1. Ignition off, lights on or off — module keeps time without display and time can't be altered.
2. Ignition on, lights off — module keeps time, display is at full brightness, time can be reset.
3. Ignition on, lights on — module keeps time, display brightness is dimmer controlled and time can be reset.

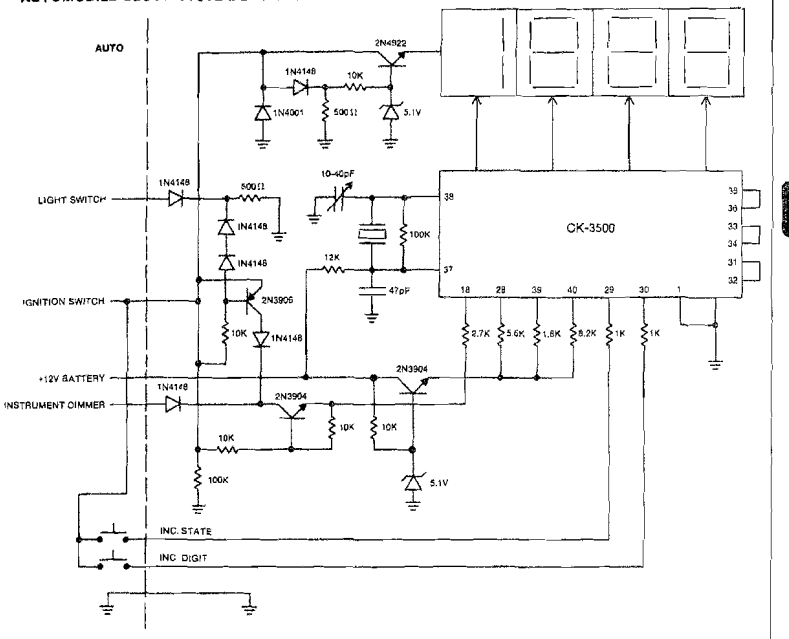
M-3500 MODULE



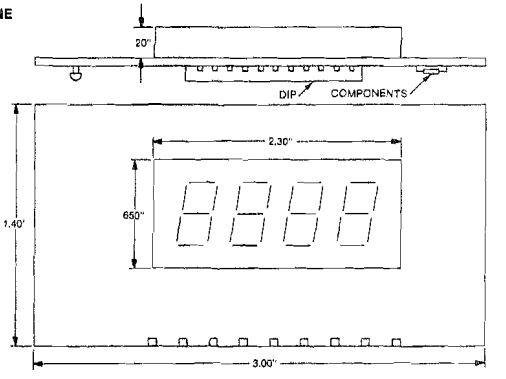
MODULE DIAGRAM



AUTOMOBILE CLOCK SYSTEM DIAGRAM



MODULE OUTLINE



RADIO/TELEVISION/REMOTE CONTROL

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
FREQUENCY COUNTER/DISPLAY	Counts & displays MW, SW, and VHF frequencies	AY-5-8100	4A-2
		AY-5-8102	4A-2
FREQUENCY COUNTER/DISPLAY WITH 4 DIGIT CLOCK	Counts & displays AM/FM frequencies with a 12 hour clock	AY-3-8110	4A-5
		AY-3-8112	4A-5
OMEGA® 82 CHANNEL DIGITAL TUNING SYSTEM	Control circuit: accepts keyboard/remote inputs to control and program system	T-1001	4A-10
	Display circuit: displays selected channel number	T-1101	4A-10
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	4A-14
	Memory circuit 100 word x 14 bit EAROM	ER 1400	4A-17
	Optional channel selector interface circuit: permits preset favorite channel selection	T-1201	4A-19
ECONOMEGA® I 16 CHANNEL DIGITAL TUNING SYSTEM	Control circuit accepts direct/remote inputs to control/ program system	AY-3-8203	4A-20
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	4A-14
	Memory circuit 100 word x 14 bit EAROM	ER 1400	4A-17
ECONOMEGA® II 20 CHANNEL DIGITAL TUNING SYSTEM	Control/memory circuit: accepts direct/remote inputs to control/ program system	AY-5-8290	4A-24
	D/A converter circuit: converts output to coarse and fine tune outputs	MEM 4956	4A-14
ON-SCREEN CHANNEL/TIME DISPLAY SERIES	Various circuits in series to display channel numbers on TV screen with some additionally featuring either separate or simultaneous time display. Selection of display position on screen, automatic display recall, BCD time inputs (see AY-5-1203A clock circuit)	AY-5-8300	4A-28
		AY-5-8301	4A-28
		AY-5-8310	4A-28
		AY-5-8320	4A-28
		AY-5-8321	4A-28
		AY-5-8322	4A-28
		AY-5-8324	4A-28
ON-SCREEN TUNING SCALE	Provides an electronic on-screen tuning scale for varactor tuned TV sets	AY-3-8330	4A-35
R/C SYSTEM I	30 Channel Transmitter	SAA 1024	4A-38
	30 Channel Receivers	SAA 1025-01	4A-40
		SAA 1025-02	4A-40
R/C SYSTEM II	23 Channel Transmitters	AY-5-8410	4A-44
		AY-5-8411	4A-44
	31/63 Channel Receiver	AY-5-8420	4A-46
R/C SYSTEM III	30 Channel Transmitter	AY-5-8450	4A-48
	16 Channel Receivers	AY-5-8460	4A-50
		AY-5-8461	4A-50

RADIO/TELEVISION & REMOTE CONTROL

MICRO ELECTRONICS

Radio Receiver Frequency Counter/Display Drivers

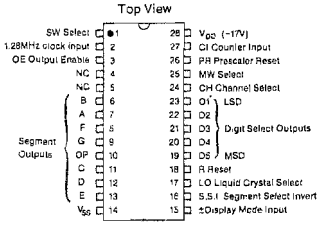
FEATURES

- Three frequency ranges: MW 2999KHz, SW 29.995MHz, VHF 299.95MHz.
- IF offset: 460KHz (AY-5-8100) or 455KHz (AY-5-8102) on MW and SW, 10.7MHz on VHF.
- Channel mode 0-99 channel spacing 300KHz. Standard part channel 0 is 87MHz.
- High voltage segment and digit outputs give direct drive of fluorescent displays.
- Inversion control for segment outputs.
- Direct drive of liquid crystal displays.
- 1.28MHz master clock input frequency.
- 300KHz input with 8ms sample time.
- TTL compatible inputs and outputs.
- 50Hz output to drive the AY-5-1200A digital clock.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

Top View



DESCRIPTION

The AY-5-8100 is a four and a half digit frequency counter for use in Radio Receivers. Three main frequency ranges are provided: 2999KHz and 29.995MHz (with a 460KHz IF offset on the AY-5-8100 and a 455KHz IF offset on the AY-5-8102) and 299.95MHz with a 10.7MHz IF offset. For use in VHF FM receivers a channel mode is available. In this mode a channel number from 0 to 99 is displayed together with a "+" or "-" sign for tuning indication. In this mode the IF is 10.7MHz and channel 0 is 87MHz.

The outputs are multiplexed in five time slots onto a seven segment bus. Digit and segment outputs have high voltage capability and will drive fluorescent displays directly. A pin option allows the driving of liquid crystal displays using the two-frequency multiplexing system.

SYSTEM DIAGRAM

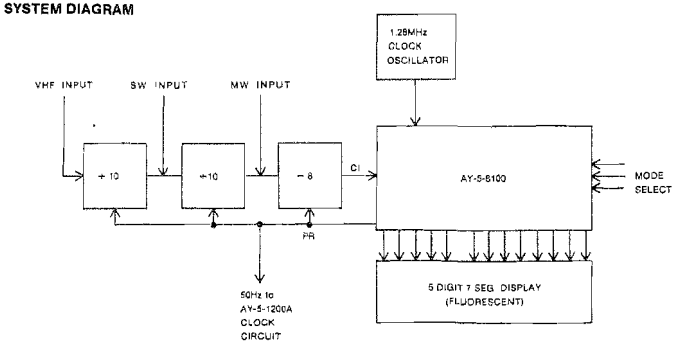


Fig.1 FREQUENCY COUNTER CLOCK CONNECTION DIAGRAM—DIRECT FLUORESCENT DISPLAY DRIVE

PIN FUNCTIONS

Pin No.	Name	Function
1	SW Select	Selects 29.995MHz counter range when at logic '0'. See Mode Select truth table.
2	1.28MHz Clock	Master clock input controls timing of whole system.
3	Output Enable	Disables the outputs when taken to logic '0'.
4	N.C.	
5	N.C.	
6-13	Segment Outputs	The digits to be displayed are output on these pins in 7 segment code. They are at logic '1' to display. These outputs will also drive fluorescent, liquid crystal and low current LED displays.
14	V_{SS}	Positive supply.
15	±Display Mode Input	Selects either combined or separate + or − display when in channel mode. Logic '0' selects combined mode. In the combined mode the horizontal bar is output on segment "g" and the vertical bar on segment "f". In the separate mode the − sign is output on segment "g" and the + sign on segment "f".
16	Segment Select Invert	When taken to logic '1' inverts the Segment Select outputs (Note 1).
17	Liquid Crystal Select	When taken to logic '1' the output timing is arranged to drive liquid crystal displays using two frequency multiplexing.
18	Reset	Master reset to all counters and registers. Resets when at logic '1'.
19-23	Digit Select Outputs D1-D5	These outputs sequentially select the digit to be displayed. They are normally at logic '1' to display. The outputs are high voltage and are capable of driving fluorescent and liquid crystal displays directly. Each digit is on for 4ms. A bonding option gives inverted outputs.
24	Channel Select	Selects channel mode when at logic '0' and SW and MW are at logic '1'. See Mode Select truth table.
25	MW Select	Selects 2999KHz counter range when at logic '0'. See Mode Select truth table.
26	Prescaler Raset	This output resets the external prescaler divider, at logic '0' during count interval.
27	Counter Input	Frequency measuring input. Frequency range 10KHz to 600KHz.
28	V_{DD}	Negative supply.

NOTE:
1. If the digit invert bonding option is used (bonding to logic '1') the SSI input logic sense will be inverted.

FREQUENCY COUNTER OPERATION

The frequency counter section is intended to work with an external prescaler. The three frequency ranges require division ratios of 8, 80 and 800. The appropriate IF offset is loaded into the counter before measuring. The local oscillator must always be at a higher frequency than the receiver frequency.

Measurement period	8msec
Reading rate	50 per second
Master clock frequency	1.28MHz

Mode	Display Range D5	D4	D3	D2	D1		Discrimination	Prescaler	IF
MW	2	9	9	9		KHz	1KHz	÷ 8	460
SW	2	9	9	9	5	MHz	5KHz	÷ 80	460
FM	2	9	9	9	5	MHz	50KHz	÷800	10.7
CH	±	9	9				300KHz	÷800	10.7
COUNT	2	9	9	9	5		0.5KHz	÷ 8	10

NOTES:
1. Leading zeros are blanked.
2. In Channel Mode the + or − signs are lit if the receiver is more than 50 KHz off tune.
3. The IF offset is mask programmed and can in principle be made to any value.
4. In Channel Mode, Channel 0 = 87 MHz.

MODE SELECTION

MW	SW	CH	OE	Mode
0	1	X	1	MW
1	0	X	1	SW
1	1	1	1	VHF
1	1	0	1	VHF/Channel
0	0	0	1	Counter mode
X	X	X	0	Clock

DISPLAY OUTPUT

The output is in 7 segment form multiplexed into five time slots at a rate of 50Hz. All the display outputs have high voltage capability and will drive fluorescent displays directly. LED displays can either be driven directly or with simple interfacing depending on the digit size.

A pin selected option allows the direct driving of liquid crystal displays using two frequency multiplexing (125Hz and 8000Hz).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin (except Segment and Digit Outputs)	+0.3V to −20V
Voltage on Segment and Digit Outputs with respect to V_{SS} pin	+0.3V to −35V
Ambient operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C
Power dissipation	600mW

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

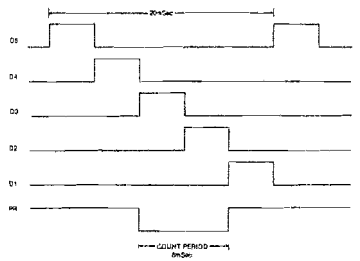
V_{SS} = +5V ±0.5V
V_{DD} = −12V ±1V
} or: $V_{SS} - V_{DD}$ = 15.5V to 18.5V
V_{II} = −28V ±2V
Operating Temperature (T_A) = 0°C to +70°C
Fc = 1.28MHz ±0.01%

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Input logic '0' level	V_{IL}	—	—	+0.8	Volts	
Input logic '1' level	V_{IH}	V_{SS} −1	—	—	Volts	
Input load current (SW, 1.28MHz, OE, MW, CI, CH)	I_{IL}	—	—	0.2	mA	$V_{IN} = -V_{DD}$ Note 1
Input sink current (DMI, SSI, LQ, R)	I_{IH}	—	—	0.2	mA	$V_{IN} = +V_{SS}$ Note 2
Input capacitance	C_{IN}	—	—	10	pF	V_{IN} = 0V f = 1MHz
Digit Select Outputs						
Logic '1' On Current		5	—	—	mA	$V_{OUT} = (V_{SS} - 2)V$ Fig. 2
Logic '0' Off Current		—	—	10	µA	$V_{OUT} = (V_{II} + 1)V$ Fig. 2
Segment Outputs						
Logic '1' On Current		2	—	—	mA	$V_{OUT} = (V_{SS} - 2)V$ Fig.2
Logic '0' Off Current		—	—	10	µA	$V_{OUT} = (V_{II} + 1)V$ Fig.2
PR Output						
Logic '0'	V_{OL}	—	—	0.5	Volts	Load = 2TTL gates (3.2mA), 3.3K resistor to V_{DD}, +20pF
Logic '1'	V_{OH}	V_{SS} −2.2	—	—	Volts	
Clock input frequency	f_c	—	1.28	1.4	MHz	Note 3
Clock pulse width		350	—	—	ns	logic '0' or '1'
Count input frequency		10	—	600	kHz	
Count input pulse width		600	—	—	ns	logic '0' or '1'
Multiplex rate		—	50	—	kHz	
Power consumption		—	450	—	mW	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These inputs have resistors of nominally 170Kohm connected to V_{SS}.
2. These inputs have resistors of nominally 170Kohm connected to V_{DD}.
3. For correct frequency readings the clock input frequency must be 1.28 MHz ± 1 in 10^5.

TIMING DIAGRAM



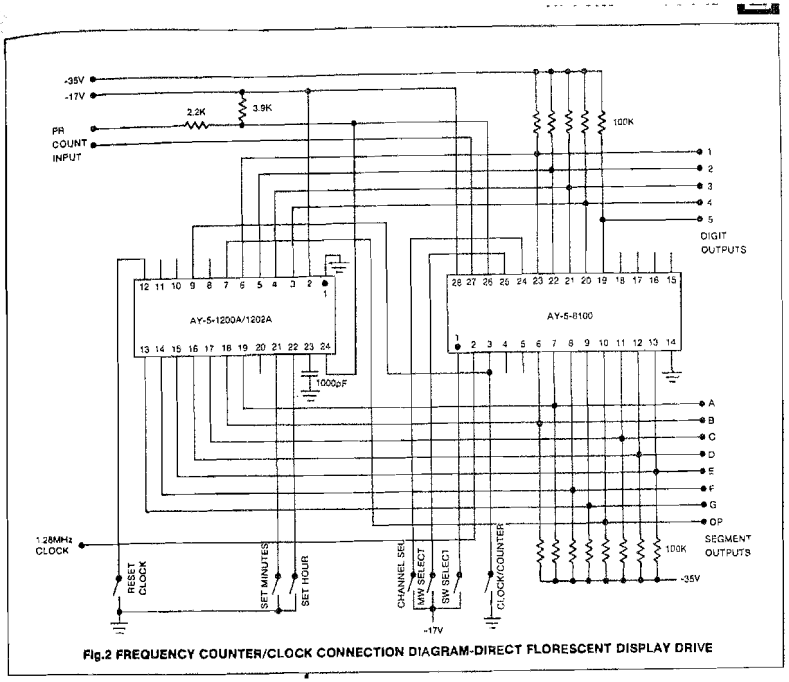


Fig.2 FREQUENCY COUNTER/CLOCK CONNECTION DIAGRAM-DIRECT FLORESCENT DISPLAY DRIVE

AY-3-8110 AY-3-8112

Radio Receiver Frequency Counter/Display Drivers with 4 Digit Clock

FEATURES

- Low current drain (10 mA)
- Wide supply voltage range (5V to 16V)
- Intensity control on-chip with external RC
- Display disable
- Mask programmable display frequency 100, 200, 400, 800 or 2 KHz
- Inter digit blanking — 10μs
- Latched outputs to avoid blanking or flashing during counting.

RADIO FEATURES

- Measures standard AM and FM frequencies
- Displays frequencies on 3½ digit display
- Externally programmable FM IF offset
- 262.5 KHz AM IF offset (AY-3-8110)
- 455 KHz AM IF offset (AY-3-8112)
- 10KHz steps on AM, 200KHz steps on FM.

CLOCK FEATURES

- 12 hour clock
- Hour and minute display
- Seconds reset control
- Easy time set controls

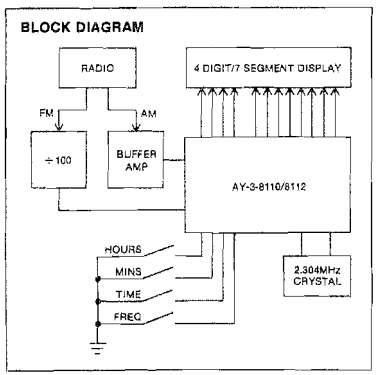
DESCRIPTION

The Clock and Radio Readout chip is an LSI system that contains all the necessary circuitry for displaying time of day or radio tuning frequency on a common 3½ digit display.

The time is derived from an on-chip crystal oscillator and internal countdown circuitry. An internal digit counter and seven segment decoder provides the signals to drive the display. The radio station frequency is determined by measuring the local oscillator of the radio and subtracting the IF frequency.

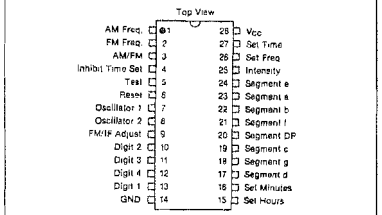
The chip is a monolithic N-channel metal gate MOS device using Ion Implant to achieve both enhancement and depletion devices.

BLOCK DIAGRAM



PIN CONFIGURATION

28 LEAD DUAL IN LINE



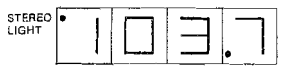
OPERATION

The keyboard consists of two momentary 2-pole switches: Time/Frequency and Set Hours/Set Minutes. The hours or minutes are advanced at 2 per second after a one second delay. A momentary depression of the set minutes resets the seconds without altering the minutes. The display switches from time to frequency and remains there on the momentary depression of the Time/Frequency switch to frequency. The display automatically switches to time when the radio is turned off.

Four external diodes program the chip to accept 16 different FM IF offset frequencies from .1046 MHz to .1076 MHz in 200 Hz steps.

The clock colon is automatically displayed using the decimal points as shown. The clock is 12 hours.

When displaying frequency the decimal points are also used to indicate stereo and the radio station. There are no decimal points in the AM mode. Below is the FM display. (The least significant digit is a LH DP. All others are RH DP.)



The FM local oscillator output of the radio must be divided by a factor of 100. The AM display is as follows:

OPERATION (Continued)

The FM frequency display always shows odd tenths. The display reads the center of the frequency band even if the radio is tuned up to ±100KHz off center. The FM IF offset is determined by the use of diodes. The program code is as follows: (A '1' represents a diode from the digit line to the IF input pin, pin 9.)

The code is shown below:

Frequency	Digit Lines 10 Hour	Hour	10 Min.	Min.
.1076	1	1	1	1
.1074	1	1	1	0
.1072	1	1	0	1
.1070	0	1	1	0
.1068	0	1	0	0
.1066	0	0	1	1
.1064	0	0	1	0
.1062	1	0	1	0
.1060	0	0	0	0
.1058	1	0	0	1
.1056	1	0	0	0
.1054	1	1	0	0
.1052	0	0	0	1
.1050	0	1	0	1
.1048	0	1	1	1
.1046	1	0	1	1

The AM display always ends in zero.

The AM IF offset is 262.5 KHz on the AY-3-8110 and 455 KHz on the AY-3-8112.

The display reads the center of the band even if the radio is tuned up to 5 KHz off center.

DISPLAY OUTPUT INTERFACE

There are twelve output lines to drive the digital display: seven to drive the segments of the display, four for the digit drive, and one for the colon, decimal point and stereo light. The decimal point, colon and stereo light follow the truth table below:

	AM	FM	Time	Digit Time
Colon	OFF	OFF	ON	10 min., hrs.
Decimal Point	OFF	ON	OFF	min.
Stereo Light	OFF	ON	OFF	10 hrs.

4A

PIN FUNCTIONS

Pin No.	Name	Function
1,2	AM Freq., FM Freq.	The local oscillator output frequencies from the radio are connected here.
3	AM/FM	A high on this pin sets the logic to expect a FM frequency in. A low sets the internal logic to AM.
4	Inhibit Time Set	A high level enables the set hours or set minutes switches. Open circuit disables these switches.
5	Tast	An 8 Hz signal can be observed here.
6	Reset	A low level resets the chip.
7,8	Oscillator 1, Oscillator 2	The crystal and associated trimmer capacitors are connected here.
9	FM/IF Adjust	The diode programming is input here.
10-13	Digit 2,3,4,1	These pins go to ground to select the appropriate digit.
14	GND	0.0V
15,16	Set Hours, Set Min.	A ground on these pins causes the hours or minutes to update at a 2 per second rate. There is a one second delay before updating starts. If set min. is grounded for more than 0.02 seconds but less than 1 second, the seconds counter is reset. (See Note 1 below).
17-24	Segments a-g & DP	These pins go positive to indicate the desired segment and decimal point.
25	Intensity	An external RC network of 1MΩ and 300pF controls the display intensity.
26,27	Select Freq., Select Time	A momentary ground on one of these pins selects frequency or time to be displayed.
28	V_{CC}	Time B+ supply, +10V to +16V (clock functions down to +5V).

NOTE 1: There is a "disable" feature — grounding pins 15 and 16 simultaneously disables the display (pins 10-13 and 17-24 become three-state).

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +18V
Storage temperature range ..... -55°C to +125°C
Ambient operating temperature range ..... 0° to +60°C

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{CC} = +10V to +16V (clock functions down to V_{CC} = +5V)
Operating Temperature (T_A) = 0°C to +60°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below

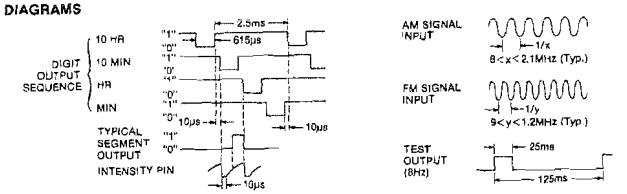
NOTE 2: Pins 3, 9, 15, 16 and 26 have on-chip pull-up resistors to V_{CC}

NOTE 3: Pins 4 and 27 have on-chip pull-down resistors to V_{SS}.

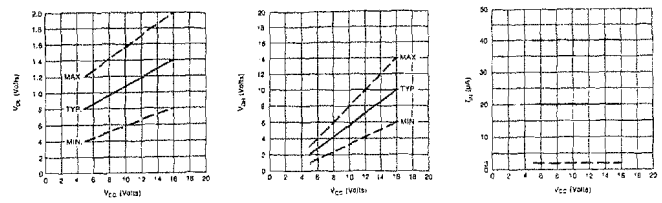
**Typical values are at +25°C and nominal voltages

Characteristic	Min	Typ**	Max	Units	Conditions
Clock					
Input Freq	—	2.304000	—	MHz	
Logic '0'	—	—	0.5	Volts	
Logic '1'	3.5	—	—	Volts	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	
Control Inputs					
Logic '0'	—	—	0.5	Volts	
Logic '1'	3.5	—	—	Volts	
Input Current (Note 2 - above)	-3	—	-40	µA	Input connected to V_{SS}
Input Current (Note 3 - above)	3	—	40	uA	Inout connected to V_{CC}
AM Freq., FM Freq., Intensity Inputs					
Logic '0'	—	—	0.5	Volts	
Logic '1'	3.5	—	—	Volts	
Leakage	—	—	10	µA	
Pulse Width - Pin 1 (AM)	180	—	—	ns	Positive or negative
- Pin 2 (FM)	360	—	—	ns	Positive or negative
Outputs					
Digit					
Logic '0'	—	—	1.6	Volts	V_{CC} = 16V
	—	—	1.2	Volts	V_{CC} = 10V
Logic '1'	15	—	—	Volts	V_{CC} = 16V
	9	—	—	Volts	V_{CC} = 10V
Logic '0' Current (calculated)	—	-3.3	—	mA	V_{CC} = 16V
	—	-1.95	—	mA	V_{CC} = 10V
Output Current with outputs disabled	—	—	0.4	mA	
Segment					
Logic '0'	—	—	0.5	Volts	V_{CC} = 16V
	—	—	0.5	Volts	V_{CC} = 10V
Logic '1'	6	—	—	Volts	V_{CC} = 16V
	3.5	—	—	Volts	V_{CC} = 10V
Logic '1' Current	—	2.65	—	mA	V_{CC} = 16V
	—	1.4	—	mA	V_{CC} = 10V
Output Leakage with outputs disabled	—	—	20	µA	
Supply Current	—	5	10	mA	Display outputs disabled

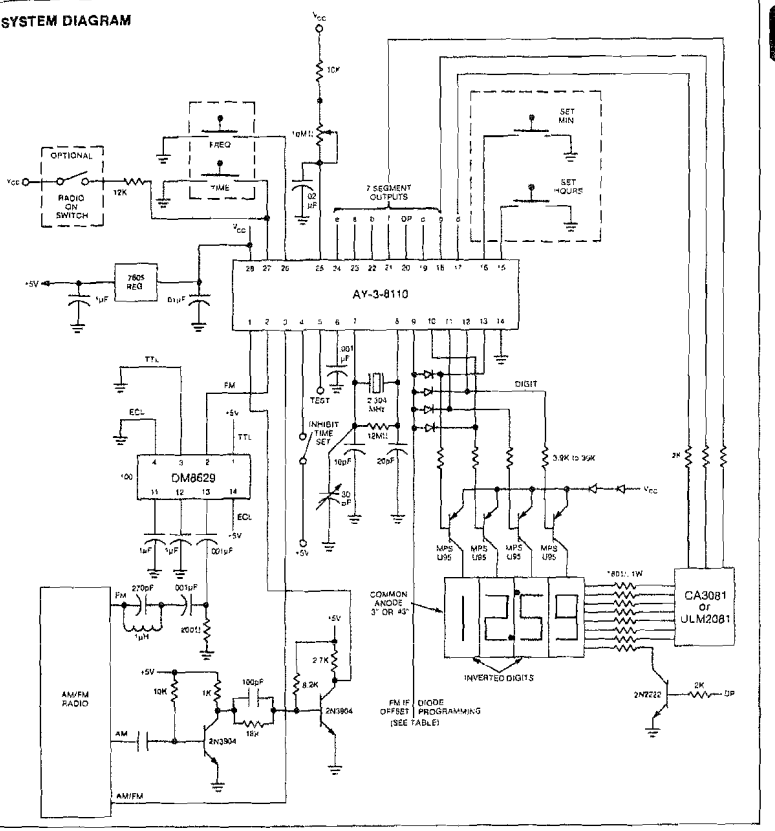
TIMING DIAGRAMS



TYPICAL CHARACTERISTIC CURVES



SYSTEM DIAGRAM



T-1001 MEM4956 T-1201
T-1101 ER1400

OMEGA/82 Channel Digital Tuning System

SYSTEM DESCRIPTION

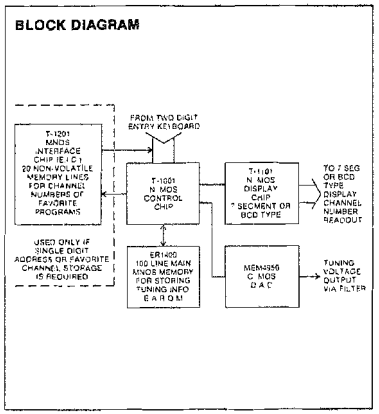
The Omega System combines an electronic solid state channel selector with a VHF/UHF varactor tuner pair. The system accepts a calculator-like 2 digit keyboard entry and provides the selected channel number on a two digit seven element display. Controls are also provided for fine-tune, coarse-tune, search, digital step tuning up and down. Single digit entry for favorite television channels is available as a design option.

The digital counterparts of the analog channel voltages corresponding to the frequencies tuned are stored in a non-volatile Electronically Alterable Read Only Memory (EAROM) which retains, without standby power, the desired coarse- and fine-tune data for all channels. The system has been designed to be extremely insensitive to supply voltage variations, component aging and environmental changes. The tuning accuracy depends only on a single well regulated reference voltage for its stability.

The method of D/A conversion used is a pulse width modulator driving a low-pass filter. The DC component out of the filter is applied to the varactor tuner. A complementary MOS device is used between the control chip and the low-pass filter to achieve the precise and stable amplitudes required at the input to the filter.

The EAROM is a 1400 bit solid state memory organized into one hundred words of 14-bits each. This technology provides a non-volatile memory for 98 channels of tuning information. Two words or lines in the EAROM are reserved to remember the two digit channel number for the last program selected by the viewer. When the set is turned on again after being off indefinitely, it automatically selects the last channel selected before shut down. Each word can be erased and rewritten without affecting the 99 other words and is updated any time the viewer adjusts the tuning of his set. Adequate space in the memory is provided for the 12 VHF and 70 UHF channels, plus 16 locations reserved for other services.

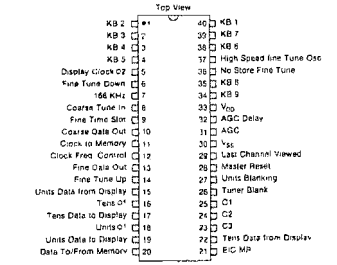
BLOCK DIAGRAM



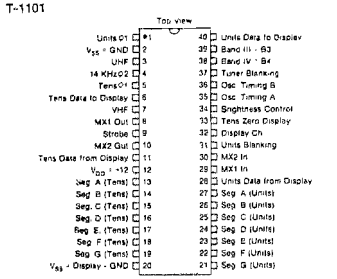
PIN CONFIGURATIONS

40 LEAD DUAL IN LINE

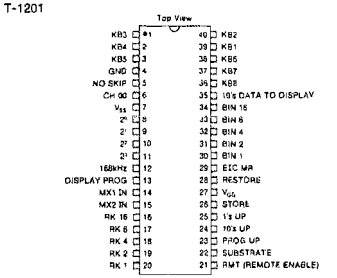
T-1001



T-1101



T-1201



Control Chip (T-1001)

The control chip scans the keyboard at a 14 KHz rate on constant alert for a switch closure. A closure may command one of the following functions:

(a) Two digit random channel selection
(b) Channel stepping (units or tens digits)
(c) Coarse-tune
(d) Fine-tune
(e) Search

The control chip also is designed to accommodate a signal input from a remote control receiver and a "power-up" signal from a power supply to trigger the last-channel-viewed function

Display Chip (T-1101)

Each digit of the channel number entry is converted into a one-out-of-ten code and serially sent to the display chip where it is stored and decoded both for a seven segment or character generator display and for band switching.

EAROM Chip (ER1400)

This channel number is also used as a two digit address (00 thru 97) for the EAROM memory to locate the corresponding memory line. This twenty bit address is sent serially to the EAROM on a single wire bi-directional data bus

The EAROM memory is designed to accept a two digit 20-bit address. This format was selected to provide ease of keyboard encoding, ease of display encoding, EAROM address decoding, and ease of address incrementation (one bit shift).

The slow speed and simple timing requirements of the memory permit address and data to flow both to and from memory on a single wire. A further economy of interconnects is achieved by using a three bit parallel code to command the memory into one of its seven modes of operation including: Input Address, Input Data, Erase, Write, Read, Data Out and Stand By

For a complete description of the operation and specifications of the ER1400, refer to the data sheet beginning on page 4A-17

D/A Converter Chip (MEM4956)

The CMOS D-to-A converter chip provides interface between the control chip outputs and the filter. In order to achieve optimum trade-off in the D/A system between clock frequency, ripple content of the filter output, and filter settling time, the 14-bit conversion is done in two parts. The 10 most significant bits generate a variable duty factor waveform with 1000 resolution elements of fixed amplitude.

The four least significant bits are used to generate a narrow pulse (equal in width to one coarse resolution element) but variable in amplitude to 15 discrete levels. The variable width and variable amplitude components are multiplexed together in the CMOS chip and drive the input to the low-pass filter. The filter integrates the area under both component waveforms and delivers a dc voltage to the varactor tuner. The ripple is kept below 100 µV and the settling time is about 50 ms. This is accomplished with a maximum clock rate of 1 MHz and with a resolution of 1 part in 15,000 of the reference supply voltage.

For a complete description of the operation and specifications of the MEM4956, refer to the data sheet beginning on page 4A-14.

Interface Chip (T-1201)

Where single digit entry is required for up to 20 favorite channels a fifth Chip (Interface Chip) is added to the system. This interface Chip is a PMNOS device incorporating a 20 line non-volatile memory (EAROM) of 12 bits per line together with all logic functions to address the 20 line memory as well as to interface directly with the rest of the Omega system via the control chip keyboard input lines.

Each memory line in this chip is capable of storing a two digit channel number ("zero" before a single digit channel number) which is entered via a tens and ones input that can be sequenced through 0 to 9 with wrap around, but without carry over and can be stored by pressing a store button.

The channel number output from the display chip always shows the correct channel number that is stored in the data registers of the interface chip whenever any function on it is selected

The tuning voltage output from the DAC also corresponds to the data stored in the main 100 line memory for that channel number. The Interface Chip uses a binary input keyboard to provide single digit access to each of up to twenty memory lines via a diode matrix or to directly interface with binary coded, remote systems for a single digit address

Provision has been made for sequencing through all 20 memory lines for simplified remote control, with the capability of introducing a skip code (0,0) to bypass any memory line. Memory line or single digit button number outputs are also available in both binary and BCD format

SYSTEM OPERATION

A. Two digit entry (4 chip OMEGA system)

To select a channel the viewer depresses two digits ("zero" before a single digit channel number) on a keyboard connected to the keyboard entry pins on the control chip. A one of six subroutine counter in the control chip is used to continuously scan the keyboard for a closure which then stops the scanner. A debounce device is used to confirm the closure after a debounce period of approximately 15 msecs. Confirmation of key closure converts the subroutine counter into a shift register which passes the data contained in it to a register in the display chip. The process is repeated when the second digit is entered. When both digits of a valid entry are received by the data registers in the display chip the following sequence occurs

a) The control chip addresses word/line 99 in the 100 line main memory (EAROM) via the EAROM address register.

b) One digit of the channel number stored in the display chip registers is shifted via the control chip to the data register of the EAROM and upon receiving a "write" signal from the control chip the data is shifted into the EAROM memory line accessed by the address register (in this case line 99). This is repeated for writing the second channel number digit into line 98 and the combination represents the storing of the last channel viewed information used during power up of the system.

c) After storing the last channel viewed information the channel number stored in the display chip register is sent via the control chip to the address register of the EAROM so that the memory line corresponding to this channel number can be read on command from the control chip.

d) The read-from-memory command causes the data in the 14 bit memory line accessed to be read into the Data register of the EAROM and from there out to a 14 bit register in the control chip which also doubles as two polynomial counters of 10 and 4 bits.

e) After receiving the information from the data register of the EAROM, the 14 bit register in the control chip becomes a ten bit and a four bit polynomial counter. The 10 bit polynomial counter is used to produce, via a set/reset flip flop, a variable duty cycle square wave (amplitude is V_{DD} to V_{ES}) which is used to generate, via the CMOS DAC, the coarse tuning voltage corresponding to the code in the line of the EAROM that was accessed.

f) The four bit polynomial counter acts similarly to the 10 bit counter, but in a different time frame, it gives a variable duty cycle square wave at a frequency of approximately 67 KHz.

g) The coarse and fine tune data is fed from the control chip to the DAC where it is amplified to the level of V_{REF} (tuning voltage reference). The fine tune information is also filtered to a DC level and then inserted at the end of each coarse tune pulse. It is this combined output of the DAC that is filtered by a 5 pole filter network to produce the tuning voltage V_T for the varactor tuners. The output impedance of the filter is approximately 47 K ohm and its rise time is about 50 msecs.

Operation of the fine tuning controls (UP or DOWN) on the control chip alters the 4 bit polynomial counter which has carry over to the 10 bit polynomial counter. Therefore use of these controls allows the user to scan through the total tuning voltage range at a speed that is determined by the time constant of the network connected to pin 37 of the control chip. Alteration of the time constant is used to provide coarse tune speed for set up, as well as equalization of the tuning rate (MHz/sec) between VHF and UHF.

The action of the store-fine-tuning command, which may be made manually, or automatically on release of the fine tune button, cause the two polynomial counters to chain together into a 14 bit shift register which then shifts its contents into the data register of the EAROM which is then written into the memory line of the EAROM corresponding to the channel number that is in its address register.

The new tuning data is still retained in the control chip register which returns to its polynomial counter mode and continues operating as previously described.

On power-up, a master reset pulse is generated in the control chip to reset all clocks. The control chip then also addresses lines 99 and then line 98 of the EAROM in sequence causing the information stored in those lines (last channel number viewed) to be out into the display chip register (if last channel viewed option is used) which then starts up the sequence described previously just as if this data came from the control chip keyboard. Read and write times of the EAROM lines are approximately 20 msecs. All times are referenced to the internally generated 1 MHz clock in the control chip.

Channel number information in the display chip register is used to automatically decode the band information which is fed out as logic signals by the 4 band outputs of the display chip. The channel number information is also available (depending on display chip used) in a form suitable for common anode type seven segment displays (units and tens digit information are separate) or for character generator type display in BCD format. Timing waveform outputs and inputs are provided on the display chip for decoding channel number information where appropriate.

B. One digit entry (5 chip option)

The use of the Interface chip for single digit entry for up to 20 favorite channels does not basically modify the operation of the system as described above. This chip interfaces with the keyboard lines on the control chip and the operational sequence is identical to that of a two digit entry from the keyboard except that the two digit information comes from the Interface chip register which is fed the two digit channel number information stored in one of its twenty memory lines (non volatile), which can be accessed by single digit entry as described above.

When the Interface chip is used there is an option available as an alternative to the obtaining the last channel viewed on power-up. This alternative option always returns the system to memory line "one" on the Interface chip on power-up.

ELECTRICAL CHARACTERISTICS

Maximum Ratings

Voltage on any pin with respect to V_{SS} ..... -20V to +.3V
Storage Temperature Range ..... -30°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

T-1001 Standard Conditions (unless otherwise stated)

V_{SS} = Ground
V_{DD} = +12V
T_A = 0°C to +70°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Voltage, V_{DD}	10.8	12	13.2	V	
Supply Current, I_{DD}		15	35	mA	V_{DD} = 12.0 VDC
Master Clock, f_m	0.7	0.8	0.9	MHz	R = 100K ± 5% to V_{DD}
Fine Tune Clock, f_f	9.7	11.2	12.5	kHz	C = 68, 75, or 82pF ± 10% to V_{SS}
Inputs:					
Logic "1"	V_{SS} +8	—	V_{DD}	V	
Logic "0"	V_{SS}	—	V_{SS} +.5	V	
Outputs:					
Logic "1"	V_{DD} -2	—	V_{DD}	V	
Logic "0"	V_{SS}	—	V_{SS} +.5	V	
Rise & Fall Time t_r, t_f			1	µs	

T-1101 Standard Conditions

V_{SS} = Ground
V_{DD} = +12V
T_A = 0°C to +70°C

Characteristic	Units	Min.	Max.	Conditions
V_{DD}	V	10.8	13.2	
I_{DD}	mA		10	With clock running
V_L	V	V_{SS}	V_{DD}	
Quiescent Current	mA		10	Clock Frequency = 0Hz
V_{LN} (Logic Low Signal In)	V	0.0	1.0	At all inputs unless otherwise specified.
V_{HN} (Logic High Signal In)	V	8.0	V_{DD}	At all inputs unless otherwise specified.
V_{LO} (Logic Low Signal Out)	V	0.0 0.0	1.0V 0.5V	For Pins 8, 9, & 10 into 1 MΩ, 20pF load
V_{HO} (Logic High Signal Out)	V	V_{DD} -2 V_{DD} -3	V_{DD} V_{DD}	For Pins 11, & 28 into 1 MΩ, 20pF load For Pins 8, 9, & 10 into 1 MΩ, 20pF load
Ø1 (Units & Tens Clock)	KHz	9.2	16.8	Pins 1, 4, 5
T_R, T_F	ns		550	Pins 1, 4, 5
Ø2	KHz	9.2	16.8	Pin 4.
Duty Cycle Ø1 (Typical)	1/12 of clock Frequency			Pins 1, 5
Duty Cycle Ø2 (Typical)	1/6 of clock frequency			Pin 4.
T_{DELAY}	µs	.45	.55	Delay between rise of Ø1 and Ø2 = 1/F
T_R, T_F	µs		1	Pins 8 thru 11 and 28 Load = 10pF
R_{OUT}	Kohms		24	I_L = 1 mA Pins 3,7,38,39
V_O	V	2.0V	Variations Between These Outputs on any 1 chip to be 1V Max	At I_O Min. = 17 mA. Additionally each output shall be capable of sustainning I_O max 25 mA pins 13, 14, 15, 16, 17, 18, 19, 21, 22, 23, 24, 25, 26, 27. For LED display only. In the off condition leakage current at +20V to be no greater than 10 µA.
I_O	mA	1.6		For indirect display drive — 13, 14, 15, 16, 24 thru 27. Outputs to be compatible to TTL or CMOS withut interface. V_o = 0.6V.

CMOS D/A Converter

FEATURES

- Combined and/or separate Coarse and Fine Tuning
- 30V Tuning Voltage Range
- High Stability
- Low Power Consumption

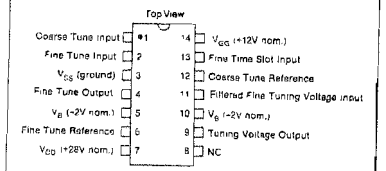
DESCRIPTION

The Mem 4956 is a CMOS D/A Converter designed to operate in conjunction with the GI Omega and Economega Digital Tuning Systems.

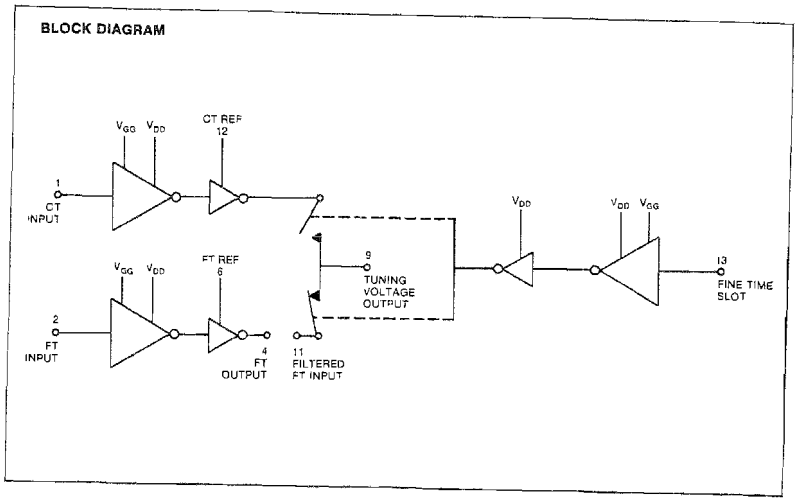
It consists of two level shifting amplifier-drivers with a common output. A control input determines which amplifier is connected to the output.

PIN CONFIGURATION

14 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1.	Coarse Tune Input	Positive going pulse. The duty cycle determines the Tuning Voltage Output.
2.	Fine Tune Input	Positive going pulse. The duty cycle determines the Fine Tuning Voltage Output.
3	V_{SS}	Negative power supply
4.	Fine Tune Output	Amplified version of Fine Tune Input. Switches between Vss and Fine Tune Reference.
5.	V_B	-2V Bias used to increase breakdown voltage.
6.	Fine Tune Reference	Power supply to Fine Tune Buffer Amplifier: 28V nom
7.	V_{DD}	Power supply for Logic: 28V nom. (Vdo must be the most positive power supply).
8.	Tuning Voltage Output	Combined Coarse and Fine tuning data which after filtering is used to tune the TV.
10.	V_B	-2V Bias used to increase breakdown voltage.
11.	Filtered Fine Tuning Voltage Input	The Filtered Fine Tuning Voltage connected to this input is combined with the Coarse Tuning Data by the action of the Fine Time Slot input.
12.	Coarse Tune Reference	Power supply to Coarse Tune Buffer Amplifier: 28V nom
13.	Fine Time Slot Input	When at logic '0' the Coarse Tuning information is connected to the Tuning Voltage Output. When at logic '1' the Fine Tuning information is connected.
14.	V_{GG}	+12V reference for input level shifting circuit.

4A

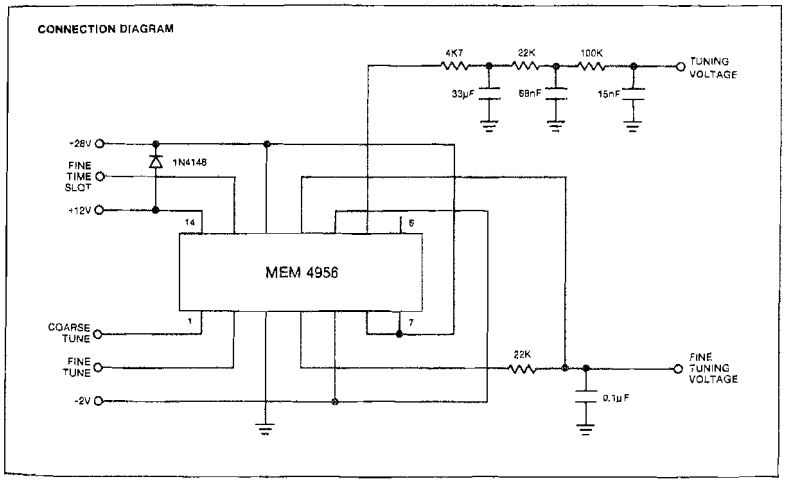
STANDBY

The -2V V_B supply may be reduced to 0V during standby provided that V_{DD}, V_{REF1} and V_{REF2} are reduced to +12V (V_{GG}). The V_B pins must not be open circuited.

BIAS SUPPLY

The -2V V_B supply must have a source impedance of 2.2Kohm or less and be decoupled to V_{SS} by a 10nF ceramic capacitor.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

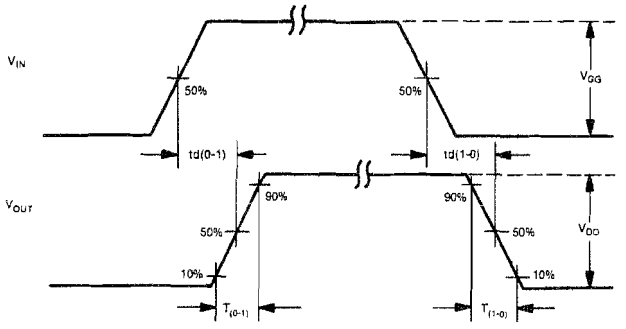
Voltage of any pin with respect to V_{SS} pin (3) (except $V_{REF.1}$, $V_{REF.2}$, V_{DD} and V_B) ..... -0.3 to +20V
Voltage on $V_{REF.1}$, $V_{REF.2}$, V_{DD} with respect to V_{SS} pin ..... V_{GG} to +36V
Voltage on V_B with respect to V_{SS} pin ..... -4 to +0.3V
Storage Temperature Range ..... -40°C to +100°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = 0V
V_{GG} = +12V ± 10%
V_{DD} = $V_{REF.1}$ = $V_{REF.2}$ = +28 to +30V
V_b = 2V ±10%
T_a = +25°C

Characteristic	Min.	Typ.	Max.	Units	Conditions
Input					
Logic '0'	-0.2	—	+0.3	Volts	
Logic '1'	10	—	V_{GG}	Volts	
Fine Tune Output on Resistance					
Logic '0'	—	100	300	Ohms	
Logic '1'	—	70	200	Ohms	
Tuning Voltage Output on Resistance					
Logic '0'	—	200	500	Ohms	Pin 4 connected to Pin 11
Logic '1'	—	300	700	Ohms	R1 = 10KOhm
Output Propogation Delay					
Logic '0' to Logic '1'	—	90	—	ns	C1 = 100pF
Logic '1' to Logic '0'	—	80	—	ns	
Output Switching Time					
Logic '0' to Logic '1'	—	80	—	ns	C1 = 100pF
Logic '1' to Logic '0'	—	70	—	ns	
Supply Current					
V_{GG}, V_{DD}, $V_{REF.1}$, $V_{REF.2}$, V_B	—	0.2	5	µA	V_{DD} = $V_{REF.1}$ = $V_{REF.2}$ = +28V V_{GG} = +12V, V_B = -2V. Pin 4 connected to pin 11; all inputs at V_{GG} or V_{SS}

TIMING DIAGRAM



1400 Bit Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 100ms/word
- Single -35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

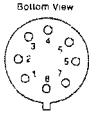
Addressing is by two consecutive one-of-ten codes.

Mode selection is by a 3 bit code applied to C1, C2 and C3.

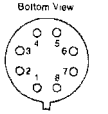
Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATION

Standard package
8 LEAD TO-99

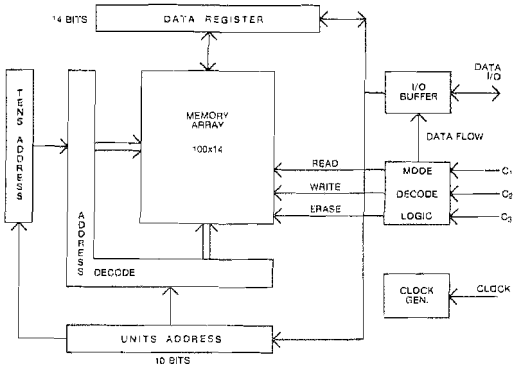


Special order package
8 LEAD TO-8



1. Data I/O
2. V_{BB}
3. V_{SS}
4. V_{GG}
5. Clock
6. C1
7. C2
8. C3

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating
2	V_M	Used for testing purposes only. Must be left unconnected for normal operation.
3	V_{SS}	Chip substrate. Normally connected to ground
4	V_{GG}	DC supply. Normally connected to -35 volt supply
5	Clock	14KHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
6,7,8	C1, C2, C3	Mode control pins. Their operation is as follows:

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse.
0	1	0	Erase - The word stored at the addressed location is erased to all zeros
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged.
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} . . . . . -20V to +0.3V
V_{GG} with respect to V_{SS} . . . . . +40V
Storage temperature (No Data Retention) . . -65°C to +150°C
Storage temperature (with Data Retention)
Operating . . . . . -25° to +75°C
Unpowered . . . . . -65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = -35V ± 8%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units
DC CHARACTERISTICS					
Input logic '1'	V_{IL}	V_{SS} -15.0	—	V_{SS} -8	Volts
Input logic '0'	V_{IH}	V_{SS} -1.0	—	V_{SS} +0.3	Volts
Output logic '1' (1 meg, 100 pf load)	VOL	—	—	V_{SS} -12.0	Volts
Output logic '0'	VOH	V_{SS} -1.0	—	V_{SS} +0.3	Volts
Power		—	—	300	mW
AC CHARACTERISTICS					
Clock Frequency	fφ	11.2	14.0	16.8	KHz
Write time	tw	16.0	20.0	24.0	ms
Erase	te	16.0	20.0	24.0	ms
Rise, fall time	tr tf	—	—	1.0	µs
Propagation delay	tpw	—	—	20.0	µs
Unpowered non-volatile data storage	T_S	10	—	—	Years
Number of erase/write cycles	N_W	—	—	10^5	—
Number of read accesses between writes	N_{RA}	10^9	—	—	—

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS

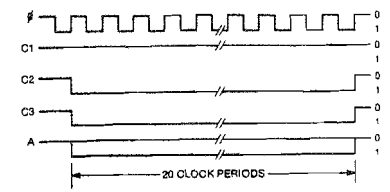


Fig.1 ACCEPT ADDRESS *

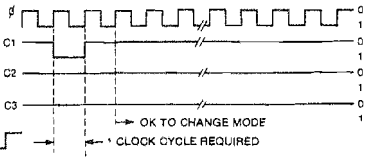


Fig.2 READ

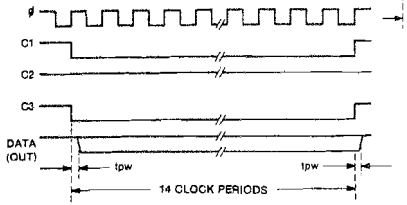


Fig.3 SHIFT DATA OUT *

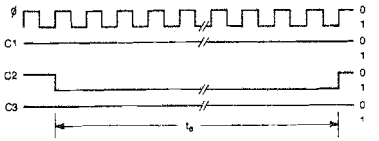


Fig.4 ERASE

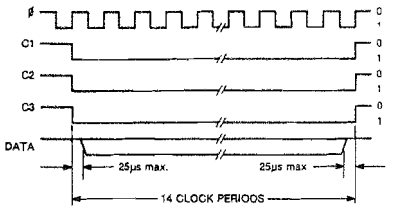


Fig.5 ACCEPT DATA *

*Output data changes on the positive-going clock edge. Data and address inputs are shifted on the negative-going clock edge.

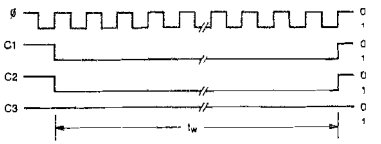


Fig.6 WRITE

ECONOMEGA I/16 Channel Digital Tuning System

FEATURES

- 8/12/16 Programs
- 4 Bands
- 10 bit Coarse-Tune
- 4 bit Fine-Tune
- Non-Volatile Memory without battery
- Auto or Manual Tuning

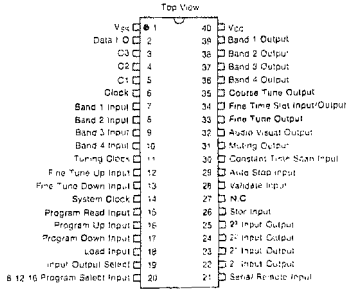
DESCRIPTION

The ECONOMEGA I Digital Tuning system is a two chip voltage synthesizer. The first chip (AY-5-8203) is an n-channel control chip which interfaces the remote control system, memory and D/A converter. The second chip (ER1400) is a non-voletile EAROM memory which stores the tuning and band information for 16 programs. For details on the ER1400 refer to the data sheet beginning on page 4A-17. For details on the MEM4956 D/A converter circuit refer to the data sheet beginning on page 4A-14.

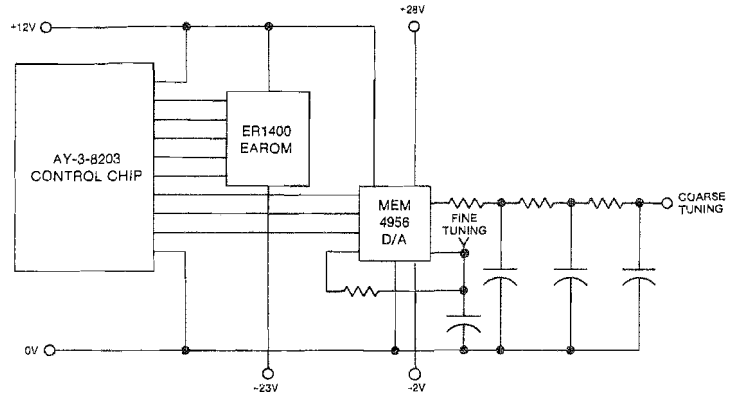
PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8203

Top View



SYSTEM DIAGRAM WITH CMOS D/A OPTION



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Ground
2	Data I/O	To ER1400 EAROM
3	C3	
4	C2	
5	C1	
6	16KHz	1.28KHz nominal.
7	Band 1 Input	When connected to V_{SS} selects Band 1 and initiates scan.
8	Band 2 Input	When connected to V_{SS} selects Band 2 and initiates scan.
9	Band 3 Input	When connected to V_{SS} selects Band 3 and initiates scan.
10	Band 4 Input	When connected to V_{SS} selects Band 4 and initiates scan.
11	Tuning Clock	Controls speed of coerse and fine tuning, set by external R-C network.
12	Fine Tune Up Input	When connected to V_{SS} causes FT to increment automatically.
13	Fine Tune Down Input	When connected to V_{SS} causes FT to decrement automatically.
14	System Clock	System clock 2.0 MHz nominal set by external R-C network.
15	Program Read Input	When connected to V_{SS} reads EAROM (includes 20ms anti-bounce delay).
16	Program Up Input	When connected to V_{SS} increments program number by 1. There is a 20msec antibounce delay on this Input.
17	Program Down Input	When connected to V_{SS} decrements program number by 1. There is a 20msec antibounce delay on this Input.
18	Load Input	When connected to V_{SS} new data is loaded into program number register from the program number inputs and the EAROM data is read. When left open the program number inputs are inhibited
19	Input/Output Select	When connected to V_{SS} selects input mode for 2^0, 2^1, 2^2, 2^3 pins.
20	8/12/16 Program Select Input	Fixes the number of programs that can be selected using the Program UP and DOWN inputs. Open circuit =12, V_{SS}=16, V_{CC}=8.
21	Serial Remote Input	Accepts a train of 0.5msec negative pulses, the number of pulses determines the program number to be selected.
22	2^0 Input/Output	Binary program numoer input/output. When used as an input accepts data in positive logic convention. (0000 = prog. 1). When used as an output the data is static and in positive logic convention. These outouts are TTL compatible.
23	2^1 Input/Output	
24	2^2 Input/Output	
25	2^3 Input/Output	
26	Store Input	When connected to V_{SS} stores Tuning and Band information in EAROM.
27	N.C.	
28	Validate Input	Confirms valid stop command. Positive for a valid TV signal.
29	Auto Stop Input	Initiates Autostop sequence on a positive going edge (except in constant time scan mode).
30	Constant Time Scan Input	When connected to V_{SS} a constant scan rate of 8 sec. per Band is selected. In addition on Band 3 stop is executed on a negative edge rather than a positive edge and the Muting output is active low with the same output specification as Band.
31	Muting Output	Active high during scan and program change (active low in constant time scan mode).
32	Audio Visual Output	Goes to logic '0' when the last program is selected (8, 12 or 16) and is on Band 3.
33	Fine Tune Output	Fine Tuning Information, 4 bits resolution.
34	Fine Time Slot Input/Output	Used by MEM4956 CMOS D/A to combine Coarse and Fine data when separate FT is not required. Connect to V_{SS} when MEM4956 is not used to invert CT and FT Outputs. The Fine Tune slot is a 2µsec pulse repeated every 250µsec on Band 3, a 10µsec pulse on Bands 2 and 4 and a 30µsec pulse on Band 1.
35	Coarse Tune Output	Coarse Tuning Information, 10 bits resolution.
36	Band 4 Output	This output goes to logic '0' when Band 4 is selected.
37	Band 3 Output	This output goes to logic '0' when Band 3 is selected.
38	Band 2 Output	This output goes to logic '0' when Band 2 is selected.
39	Band 1 Output	This output goes to logic '0' when Band 1 is selected.
40	V_{CC}	Positive power supply, +12V ±10%.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... -0.3V to +20 Volts
Ambient Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = OV
V_{CC} = +12V ± 10%
System Clock = 2MHz ± 7.5%

Parameter	Min	Typ**	Max	Units	Conditions
Control Inputs					
Logic '0' Level	—	—	1.0	Volts	
Logic '1' Level	8	—	V_{CC}	Volts	
Resistance	—	100	—	KOhm	to V_{CC}
Program No Inputs					
Logic '0' Level	—	—	0.5	Volts	
Logic '1' Level	8	—	—	Volts	
Resistance	—	50	—	KOhm	to V_{CC}
8/16/12 Input					
Logic '0' Level	—	—	0.5	Volts	
Logic 0/1 Level	—	open	—		
Logic '1' Level	10	—	—	Volts	
Input Resistance	—	100	—	KOhm	
Band, AV, Outputs					
Logic '0' Level	—	—	2	Volts	I_{Sink} = 5mA
Off Leakage	—	—	10	µA	V_{out} = V_{CC}
Muting Output					
Logic '1' Level	6	—	—	Volts	Isource = 2mA
Off Leakage	—	—	10	µA	Note 1
Program Outputs					
Logic '0' Level	—	—	0.4	Volts	Isink = 1.6mA
Logic '1' Level	8	—	—	Volts	Isource = 10µA
Supply Current					
V_{CC} (+12)	—	45	—	mA	at +25°C
	—	—	60	mA	at 13V and +70°C

**Typical values are at +25°C and nominal voltages
NOTE 1 In the constant time scan mode, the Muting Output has the same specification as the Band and AV outputs

OPERATION

1. Coarse Tune

The coarse tune resolution is 10 bits with a predominent output ripple at 4KHz

2. Fine Tune

The fine tune resolution is 4 bits with an output ripple at 15.6KHz The fine tune steps twice per second, it does not wrap around or overflow into coarse tune. During scanning it is reset to mid range.

3. Scanning

The actual tuning rates are fixed by the Tuning Clock and may oe adjusted over wide limits. Typical figures are shown below

(a) Normal Mode

Operation of a band button initiates scanning on the selected band, the scan rates are as follows:

Band	Scan Time
1	0.8 sec
2	1.6 sec
3	1.6 sec.
3	8.0 sec.
4	1.6 sec

(b) Constant Time Scan Mode

Operation of a band button initiates scanning on the selected band. The scan rate is a constant 8 seconds for each band.

4. Auto Stop and Validate

In the Normal Mode a stop is executed immediately on a positive going input transition. If validate goes positive within 256mSec the system stops, if not the scan will restart.
At the end of a band the tuning voltage goes back to zero and after a delay of 256mSec scanning restarts. In the Constant Time Scan mode in Band 3, the stop is executed on a negative going transition.

5. Manual Operation

In the Normal Mode Stop and Validate can be linked to the Band Inputs to give full manual control of the tuning operation.

6. Muting

The Muting output is active from the time that a Scan is initiated until the Validate input goes positive after a Stop command. When a program change is made the Muting output is activated for 256mSec

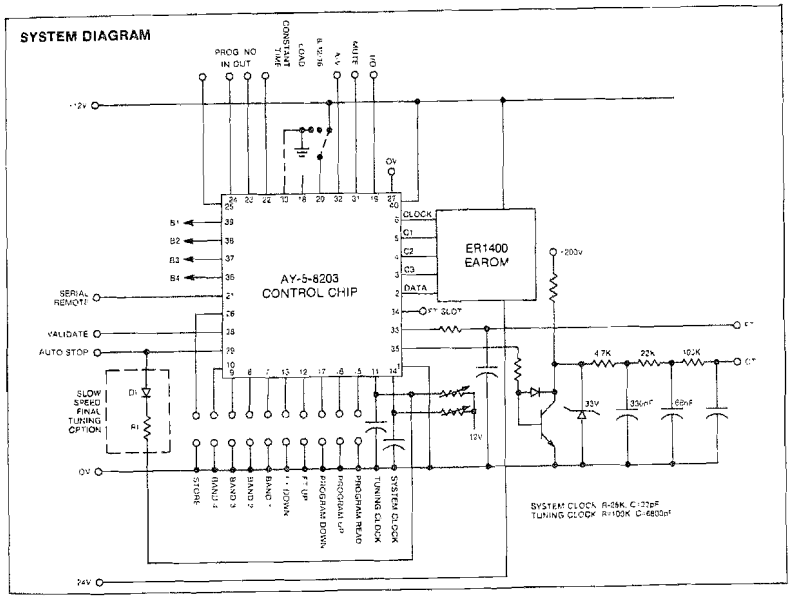
7. Tuning Procedure

1. Select required program number (1 to 16).
2. Press required band button, scanning commences from the station currently tuned, scanning stops at the next station
3. Fine tune if required.
4. Store Data

8. Fine Tune Resolution

When the MEM4956 D/A is used to combine the Coarse and Fine Data the relationship between Coarse Tune and Fine Tune is as follows:

Band 1	1 FT step = 7.5 CT steps
Band 2, 4	1 FT step = 2.5 CT steps
Band 3	1 FT step = 0.5 CT steps



PRELIMINARY INFORMATION

ECONOMEGA II/20 Channel Digital Tuning System

FEATURES

- 20 Programs
- 4 Bands
- 14 Bit Tuning Resolution
- Two digit Channel and Program Display
- Self-Contained EAROM Memory
- Most System Components Contained in Single 40 Lead DIP
- Self-Contained 500KHz oscillator
- Fully Scanned Keyboard Controls and Multiplexed Display for Pin Reduction

DESCRIPTION

The AY-5-8290 is a one chip voltage synthesizer for low-cost television tuning systems. It stores channel and voltage information for twenty programs in a self-contained non-volatile memory.

The chip is fabricated in MNOS technology and contains both P-Channel control logic and non-volatile memory within a single chip.

Channel selection is accomplished by pressing one of 20 single button program selectors or by pressing the PROGRAM UP or PROGRAM DOWN button. Provision is made for skipping unused programs. The circuit has the capability of storing and displaying two digit channel numbers from 01 to 99. A mode control permits display of the program numbers on the same two digit readout.

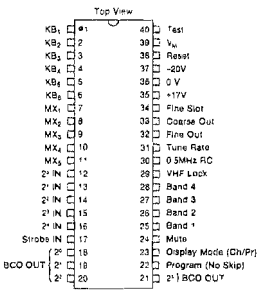
The tuning voltage is stored in memory to 14 bits of accuracy in all bands. The rate of tuning is varied automatically between bands in order to equalize the tuning rate over all bands.

Four band outputs are provided. These are automatically selected by decoding the channel number. The band decoding is done in a mask programmable ROM according to the requirements of the particular country.

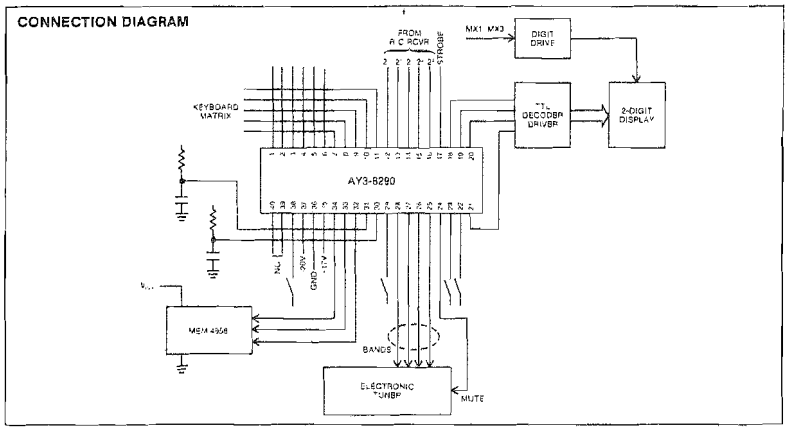
The digit to analog conversion is done by filtering a duty factor modulated waveform. The MEM 4956 CMOS D/A circuit is recommended as a buffer between the AY-5-8290 and the low pass filter. For details on the MEM 4956 refer to the data sheet beginning on page 4A-14

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-8290



CONNECTION DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1-6	KB_1 - KB_6	Six inputs from scanned keyboard matrix.
7-11	MX_1 - MX_5	Five outputs for scanning keyboard matrix and for multiplexing display.
12-16	2^0 - 2^4 IN	Five bit binary input for remote control inputs. Compatible with SAA 1025 or equivalent.
17	Strobe	Strobe for remote control inputs.
18-21	BCD Outputs	Drives TTL BCD to seven segment decoder driver. Display channel or program number according to Pin 23.
22	Program (No Skip)	A logic "1" on this pin inhibits the automatic skipping of a program if its channel number is set to "0". It also enables the "store" button.
23	Display Mode	Logic "1" causes channel number to be displayed. Logic zero causes program number to be displayed.
24	Mute	Goes to logic one during program changes
25-28	Banos 1 through 4	Single ended outputs used to activate tuner band switching. Function is internally mask-programmed according to national standards
29	VHF Lock	Logic "1" prevents user alteration of data in first 12 programs.
30	0.5MHz R/C	Pin for connection of capacitor and resistor for setting frequency on on-board clock to approximately 0.5MHz
31	Tune Rate	Pin for connection of capacitor to determine basic tuning rate.
32	Fine Out	Variable duty factor waveform proportional to 4 least significant bits of tuning data.
33	Coarse Out	Variable duty factor waveform proportional to 10 most significant bits of tuning data.
34	Fine Slot	Strobe used as input to MEM 4956 for combining fine and coarse data into single waveform.
35	+17V ± 1V	
36	Ground	
37	-20V ± 1V	
38	Reset	Resets program register to Program 1 and retrieves appropriate data from memory
39	V_M	Test pin for testing EAROM volatility
40	Test Reset	Signal provided to facilitate test of circuit.

OPERATION

A. Programming the system.

1. Switch "program" switch "on."
2. Switch rotary selection to "channel."
3. Press desired program button.
4. Operate the Channel Up/Down switch until desired channel number appears in display.
5. Operate theTuning switch until the desired program appears.
6. Press "Store."
7. Switch program switch "off".

B. Selecting a channel

1. Press desired program button.

KEY MATRIX FUNCTIONS

1-20	Single Closure selects corresponding program number and causes channel number to be retrieved and displayed and activates corresponding band output.
Pr	Increments program selector upwards and retrieves channel information each time. "1" is selected after "20". If "Program" signal (Pin 22) is a zero, programs will be skipped if they have previously been set to Channel "00".
Pr	Increments program selector downwards. "20" is selected after "1". Rest same as above.
Ch	Touching button less than 200 ms, increments the channel display upwards one count. Holding button down increments channel display at the rate of 2 counts per second.
Ch	Same as above but increments downward.
Tune	Causes tuning voltage to increase while held closed. Tunes at the rate of 1X for first 3 seconds then increases to 9X. Tune rates in UHF are both 8 times faster than VHF.
Tune	Same as above but tuning voltage decreases.
Store	Closure causes currently selected tuning voltage and channel number to be stored in memory location corresponding to currently selected program number.

KB1	KB2	KB3	KB4	KB5	KB6	
1	2	3	4	5	6	MX1
7	8	9	10	11	12	MX2
13	14	15	16	17	18	MX3
19	20	Pr↑	Pr↓	Ch↑	Ch↓	MX4
Tune↑	Tune↓	Store				MX5

Fig. 1 KEYBOARD MATRIX

ELECTRICAL CHARACTERISTICS

Power Supplies ..... +17V ± 1V at 15mA
-20V ± 1V at 5mA
GND

Clock Rate ..... 500KHz (Self contained oscillator)
D/A Converter Output Frequency ..... Predominantly 2KHz
Display Outputs ..... Drives TTL Decoder/Driver

TV Time/Channel Display Circuits

FEATURES

- Channel Display 0 to 15 or 1 to 16 or 00 to 99
- 4 Digit Clock Display option
- Color character on black background or color character on color background.
- 14 or 24 DIL package

OPTIONS

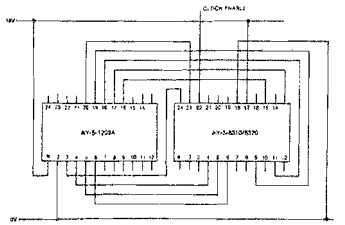
Part Number	Channel	Time
AY-5-8300	0-15	No
AY-5-8301	1-16	No
AY-5-8310/11	0-15 or 00-99	Yes
AY-5-8320/21/22/24	1-16	Yes*

*The AY-5-8320/21/22/24 are capable of either simultaneous or separate time and channel display and have automatic display enable.

DESCRIPTION

The AY-5-8300 series is a family of MOS circuits designed to display channel and time information on the screen of a TV set. The information is displayed as color characters on a black or color background. Channel information is displayed either as a single character 0 to 15 or 1 to 16 or as a dual character 00 to 99 Time is provided as a 4 digit hours and minutes display. The display is positioned at the top right hand corner or at the bottom center of the screen; the display may be permanent or momentary Any of the AY-5-8300 series except the AY-5-8324 may be used for either 525 or 625 line systems: the AY-5-8324 is for use with 625 line systems only.

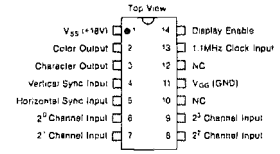
INTERCONNECT DIAGRAM FOR TV TIME DISPLAY



PIN CONFIGURATION

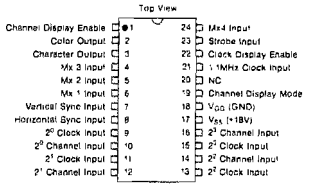
14 LEAD DUAL IN LINE

AY-5-8300/01

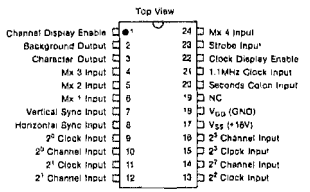


24 LEAD DUAL IN LINE

AY-5-8310/11



AY-5-8320/21/22/24



PIN FUNCTIONS

Name	Function
ALL TYPES: Vertical Sync Input	Resets the circuit at the end of each frame At logic '0' during vertical flyback
Horizontal Sync Input	Activates the line counter At logic '0' during horizontal flyback
1.1 MHz Clock Input	Determines character position and wioth. Must be synchronized by horizontal sync pulse to prevent ragged edges on character.
Channel Inputs 2^0-2^3	See table below

Code 2^3 2^2 2^1 2^0	Display AY-5-8300	Display AY-5-8301/20/21/22/24	Display AY-3-8310/11
0 0 0 0	0	1	0 0*
0 0 0 1	1	2	1 1
0 0 1 0	2	3	2 2
0 0 1 1	3	4	3 3
0 1 0 0	4	5	4 4
0 1 0 1	5	6	5 5
0 1 1 0	6	7	6 6
0 1 1 1	7	8	7 7
1 0 0 0	8	9	8 8
1 0 0 1	9	10	9 9
1 0 1 0	10	11	10 —
1 0 1 1	11	12	11 —
1 1 0 0	12	13	12 —
1 1 0 1	13	14	13 —
1 1 1 0	14	15	14 —
1 1 1 1	15	16	15 —

*00-99 MODE.

AY-5-8300/01 Display Enable	When taken to logic '0', the display is enabled. If an RC network is connected to this pin, a momentary display can be obtained
AY-5-8300/01/10/11 Character Output	Defines the background border and the character.
Color Output	Determines the character color. Goes to logic '1' during a character block.
AY-5-8310/11 Channel Display Enable	When taken to logic '0', the channel display is enabled. If an RC network is connected to this pin, a momentary display can be obtained
Clock Display Enable	When taken to logic '0', the clock display is enabled
Channel Display Mode	When at logic "0", the 0-15 channel mode is selected: logic "1" for 00-99 channel mode.
AY-5-8310/11/20/21/22/24 Clock Inputs 2^0-2^3	Multiplexed 4 digit BCD clock data inputs such as available from the AY-5-1203A clock circuit.
Mx1-Mx4	Multiplex inputs, at logic '1' during multiplex time slot For the AY-5-8310/11, when operating in the 00-99 channel mode, Mx1 and Mx2 time slots are used.
Strobe Input	This input must go to a logic '1' during the middle of each Mx time slot to load the clock data into the chip
AY-5-8320/21/22/24 Character Output	Defines the character outlines At logic '1' when displaying a character.
Background Output	Defines the background block. At logic '1' when outputting background.
Channel Display Enable	When taken to logic '1', the channel display is enabled. The display is automatically enabled when the channel is changed
Clock Display Enable	When taken to logic '1', the clock display is enabled
Seconds Colon Input	This input controls the colon between the hours and minutes display. When at logic '0', the colon is blanked. If connected to the DP output of the AY-5-1203A clock circuit, the colon will flash once per second.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin	+0.3 to −20V
Ambient Operating temperature range	0°C to +85°C
Storage temperature range.	−65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these condtions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = 0V
V_{SS} = +16V to +19V (AY-5-8300/01/10/20)
V_{SS} = +11.4V to +12.6V (AY-5-8311/21)
V_{SS} = +12.35V to +14.0V (AY-5-8322/24)
Operating Temperaturo (T_A) = 0°C to +85°C
Clock Frequency = 1.1MHz ± 10% (1.173MHz ± 10% AY-5-8322/24)

Characteristic	Min	Typ**	Max	Units	Conditions
Vertical Sync Input (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Rise & Fall Time	—	—	5	µs	10% to 90% Min slew rate 5V/µsec
Horizontal Sync Input					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	Volts	
Rise & Fall Time	—	—	1	µs	10% to 90%
1.1MHz Clock Input					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.3	Volts	
Rise & Fall Time		—	300	ns	10% to 90%
Pulse width	250	—		ns	at logic 0 and logic 1 levels
Channel Inputs (Note 1)					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −5	—	V_{SS} +0.5	Volts	
Clock Inputs, Multiplex, Strobe Inputs					
Logic '0'	0	—	7	Volts	
Logic '1'	V_{SS} −1.5	—	V_{SS} +0.3	Volts	
Input Resistance	—	20	—	Kohm	To V_{GG}
Display Enable Inputs					
Switch point positive edge	V_{SS} −8	—	V_{SS} −5	Volts	
Outputs					
On resistance	—	—	1	Kohm	$V_{OUT} = V_{SS}$ −2V
Off leakage	—	—	1	µA	V_{OUT} = 0V
Turn ON time	—	—	200	ns	10-90% load 25K & 20pF to ground
Power	—	—	400	mW	V_{SS} = +19V

**Typical values are at +25°C and nominal voltages.

NOTE:
1. These inputs are diode clamped to V_{SS}. Maximum clamp current 50µA

TIMING DIAGRAMS

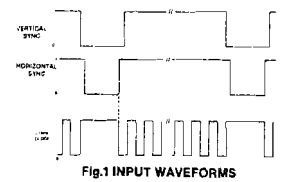


Fig.1 INPUT WAVEFORMS

TIMING DIAGRAMS

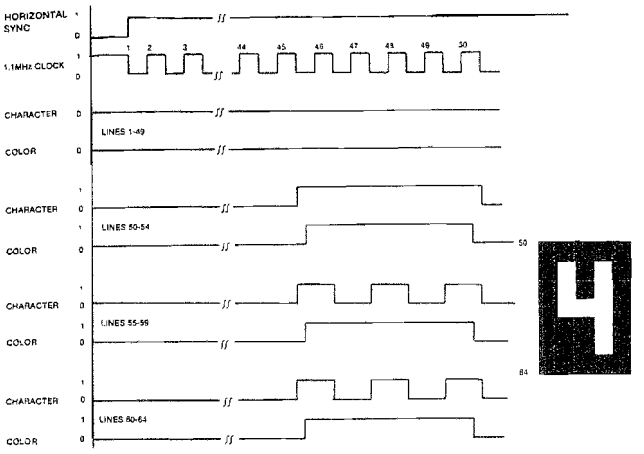


Fig.2a OUTPUT WAVEFORMS (AY-5-8300/01/10)
(AY-5-8311 AS ABOVE BUT DISPLAY STARTS AT LINE 85.)

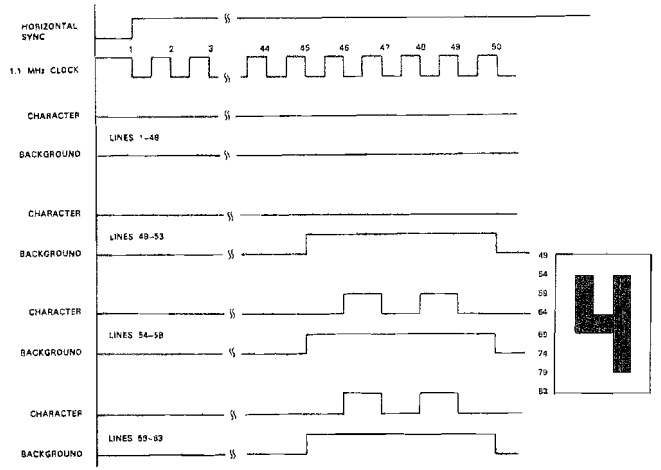


Fig.2b OUTPUT WAVEFORMS (AY-5-8320/21)
(AY-5-8322 AS ABOVE BUT DISPLAY STARTS AT LINE 165.
AY-5-8324 AS ABOVE BUT DISPLAY STARTS AT LINE 220.)

4A

OPERATION

The display is positioned digitally in both the vertical and horizontal directions. The vertical position is determined by counting horizontal sync pulses (the counting is initiated by the vertical sync pulse). The timing relationships are shown in Figs 2a and 2b. Additionally, for the AY-5-8320/21/22/24, the time display is positioned 35 lines further down so that it appears immediately below the channel display.

In the horizontal direction the display is positioned by counting pulses from an external 1.1 MHz oscillator which is synchronized with the horizontal sync pulse to prevent ragged edges on each character.

Each character is made up of 15 dots in a 3×5 matrix. With a one dot border around each character a total matrix of 35 dots in a 5×7 format is utilized. Each dot lasts 0.9μsec in the horizontal direction and is 5 lines high. This gives a rectangular dot and characters as shown in Figs. 3a and 3b.

The various channel/time display formats are illustrated in Figs 4, 6 and 7. The display positioning on the TV screen is shown in Figs 8a and 8b.

In the AY-5-8300/01/10/11, the character display is controlled by two outputs, Character and Color. The video channels are controlled in the following manner:

(a) Black/white display

Character	Color	
0	0	Normal picture
1	0	Black (luminance channel full off)
1	1	Black
0	1	White

(b) Black/Yellow display

Character	Color	Normal picture
1	0	Black (luminance full off)
1	1	Black (luminance full off and blue suppressed)
0	1	Yellow (luminance full on and blue suppressed)

Other color displays are generated by suppressing one or two chrominance channels

In the AY-5-8320/21/22/24, one video output defines the characters and the other a background block. Using these outputs, a display of any color character on a background of any color may be obtained.

The channel data is input on four lines, in the 0—15 or 1—16 channel mode, this information is applied in binary from a diode encoder attached to the varactor tuning drivers. Binary numbers greater than 9 are detected and displayed as a two digit character

In the clock mode, data is entered on a 4 line BCD bus multiplexed into 4 time slots. A strobe signal occuring in the middle of each time slot is used to read the data into the chip. When the AY-5-1203A clock is used it can be directly connected to the AY-5-8310/11/20/21/22/24 with no external components. The AY-5-8310/11 displays the time with hours and minutes (Fig.6). the AY-5-8320/21/22/24 displays the time with hours, minutes and a flashing colon for seconds (Fig.7)

In the 00-99 channel mode the data is entered as a two digit BCD number in Multiplex time slots 1 and 2 in the same manner as the clock formation.

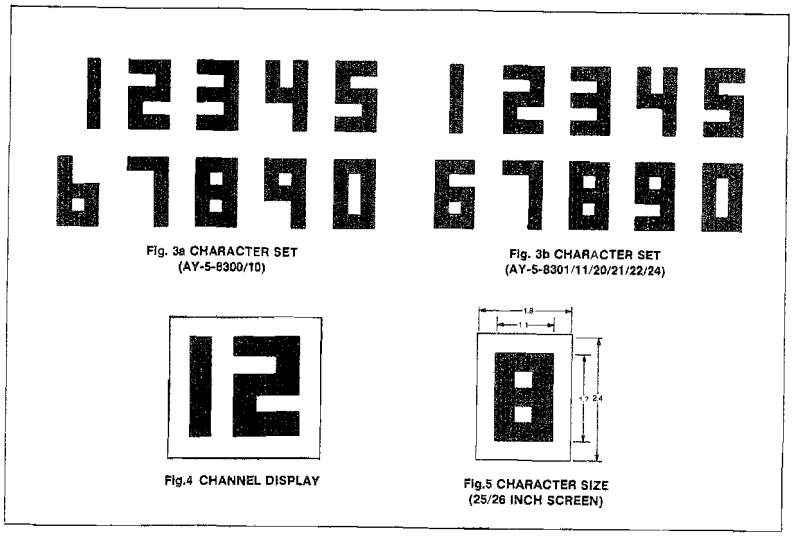


Fig. 3a CHARACTER SET (AY-5-8300/10)

Fig. 3b CHARACTER SET (AY-5-8301/11/20/21/22/24)

Fig.4 CHANNEL DISPLAY

Fig.5 CHARACTER SIZE (25/26 INCH SCREEN)

Fig.6 TIME DISPLAY (AY-5-8310/11)

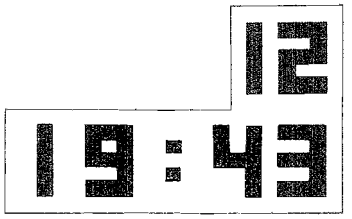


Fig.7 TIME AND CHANNEL DISPLAY (AY-5-8320/21/22/24)

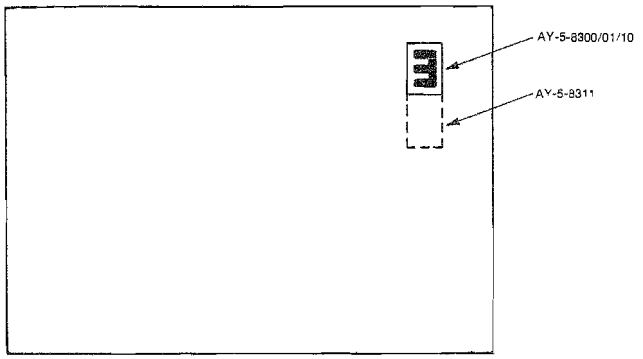


Fig.8a DISPLAY POSITION-CHANNEL (AY-5-8300/01/10/11) OR TIME (AY-5-8310/11)

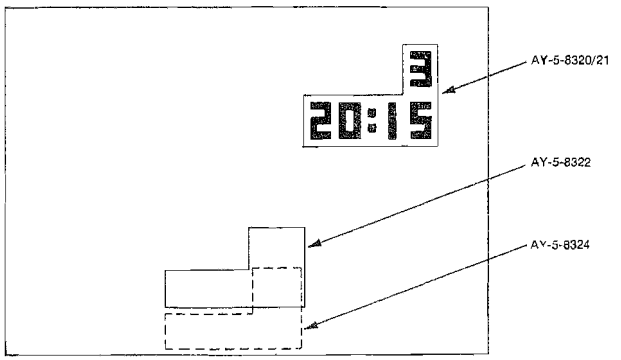


Fig.8b DISPLAY POSITION—SIMULTANEOUS CHANNEL AND TIME (AY-5-8320-21/22/24)

4A

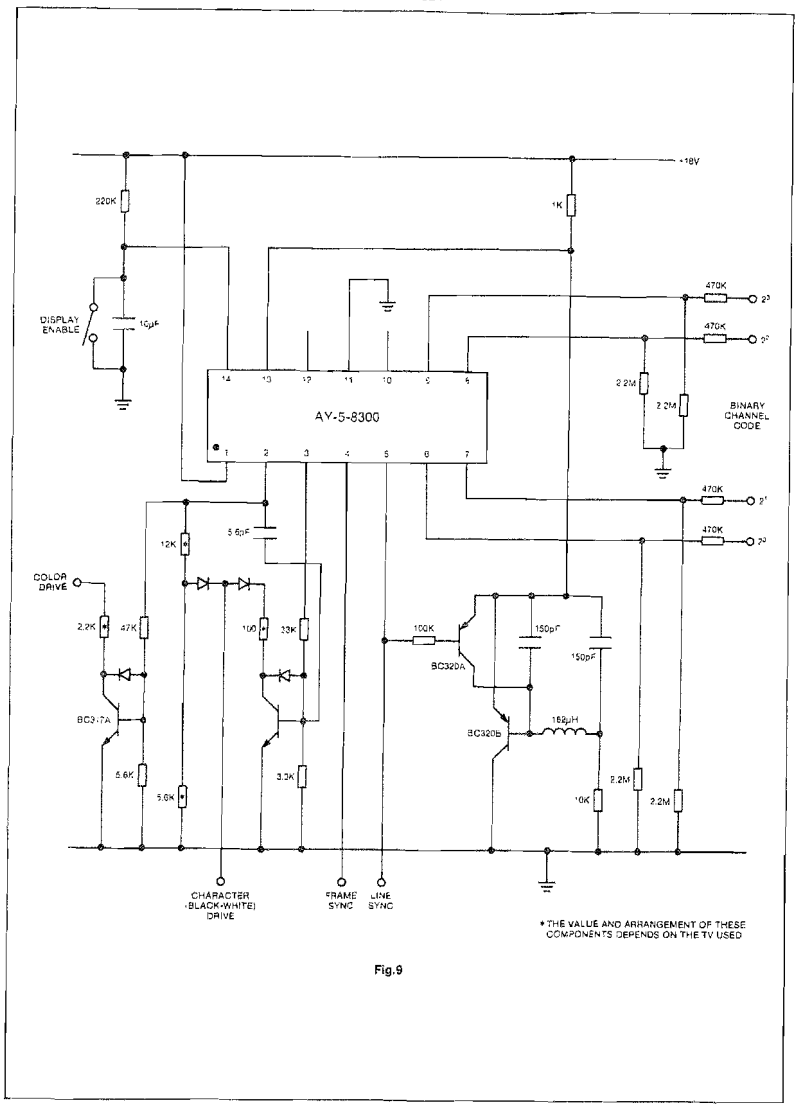

+18V
220K
1K
DISPLAY ENABLE
10µF
470K
470K
AY-5-8300
2.2M
2.2M
BINARY CHANNEL CODE
470K
470K
12K
5.6pF
COLOR DRIVE
2.2K
47K
100
33K
100K
150pF
150pF
BC320A
BC320b
BC317A
168µH
5.6K
5.6K
3.3K
10K
2.2M
2.2M
CHARACTER (BLACK-WHITE) DRIVE
FRAME SYNC
LINE SYNC
* THE VALUE AND ARRANGEMENT OF THESE COMPONENTS DEPENDS ON THE TV USED

Fig.9

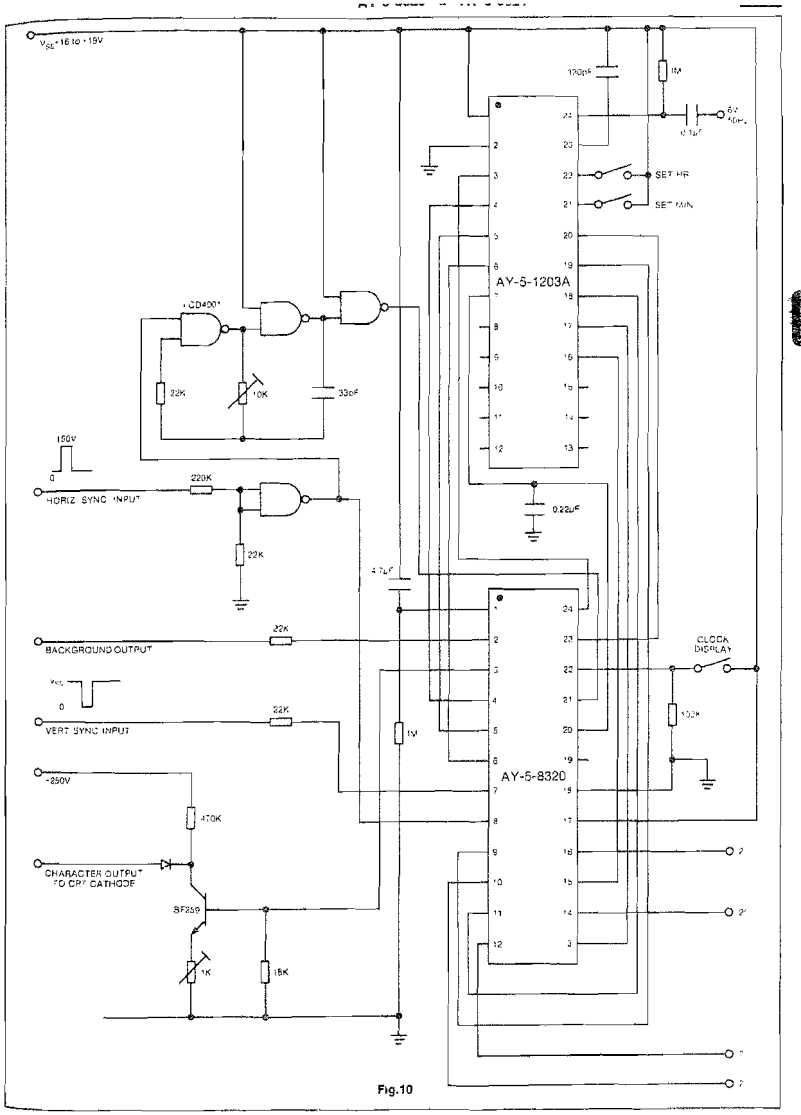

V_{SS} +16 to +19V
120pF
1M
0.1µF
SET HR
SET MIN
AY-5-1203A
CD4001
22K
10K
33pF
150V
0
HORIZ SYNC INPUT
220K
22K
0.22µF
4.7µF
22K
BACKGROUND OUTPUT
CLOCK DISPLAY
100K
0
VERT SYNC INPUT
22K
1M
AY-5-8320
-250V
470K
CHARACTER OUTPUT TO CRT CATHODE
BF259
1K
15K

Fig.10

Electronic On-Screen TV Tuning Scale

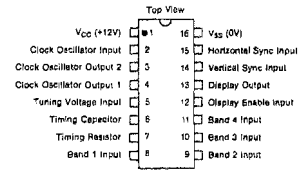
FEATURES

- Electronic tuning scale for 4 bands.
- Mask programmable for Band or Channel number display.
- Mask programmable for display position.
- 12V operation compatible with G.I. digital tuning systems.

DESCRIPTION

The AY-3-8330 is designed to provide an electronic on-screen tuning scale for varactor tuner TV sets. A horizontal line of variable length shows the tuning voltage and a scale is provided to aid tuning. Four bands are provided, band number or optionally channel number being displayed. The band or channel number display may be mask programmed as desired within the limitation of 2 blocks of 5×7 dots (see Fig.3). The graticule may also be programmed as required.

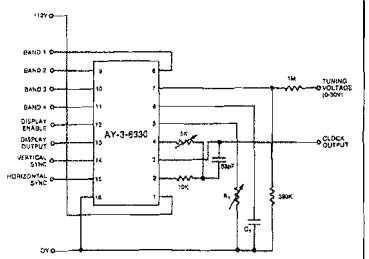
PIN CONFIGURATION
16 LEAD DUAL IN LINE



PIN FUNCTIONS

Name	Function
V_{CC}	Positive supply (+12V ± 10%)
V_{SS}	Ground
Horizontal Sync Input	Negative sync pulse from TV set
Vertical Sync Input	Negative sync pulse from TV set
Clock Input	1.1 MHz master clock which fixes display horizontal position.
Clock Output 1	Intermediate clock output
Clock Output 2	Output of on-chip oscillator synchronized by Horizontal Sync. May be used to drive AY-5-8320 Display Circuit via a CMOS invertor.
Tuning Voltage Input	Tuning voltage from Varactor diodes. Length of tuning bar is proportional to this voltage.
Timing Capacitor	Connect timing capacitor from this pin to V_{SS}.
Timing Resistor	Connect adjustable timing resistor from this pin to V_{SS}.
Band 1 Select Input	Connect to V_{SS} to select required band, either channel number or band number information will be displayed.
Band 2 Select Input	
Band 3 Select Input	
Band 4 Select Input	
Display Output	Positive going output of video information.
Display Enable Input	Connect to V_{SS} to enable display

SYSTEM DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin ..... -0.3 to +20V
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +12V ± 10%
T_A = 0°C to +70°C
Clock frequency = 1.1 MHz

Parameter	Min	Typ**	Max	Units	Conditions
Inputs					
Logic '0'	0	—	+4	Volts	
Logic '1'	+8	—	Vcc	Volts	
Analog Input	0	—	+9	Volts	
Display Output					
Logic '0'	—	—	0.5	Volts	I sink = 1mA
Logic '1'	V_{CC} -1	—	—	Volts	I source = 1mA
Ton, Toff	—	—	200	nsec	
Power Supply Current	—	10	—	mA	

**Typical values are at +25°C and nominal voltages.

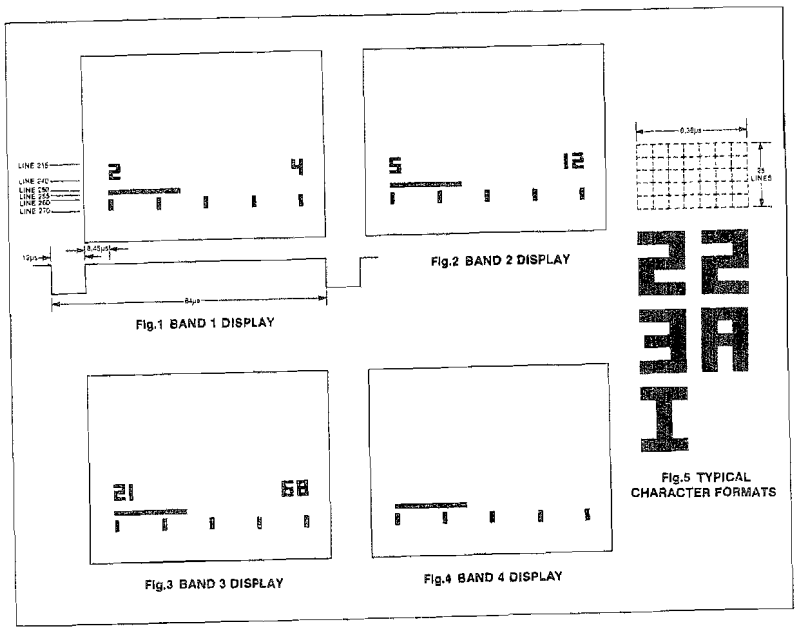


Fig.1 BAND 1 DISPLAY

Fig.2 BAND 2 DISPLAY

Fig.3 BAND 3 DISPLAY

Fig.4 BAND 4 DISPLAY

Fig.5 TYPICAL CHARACTER FORMATS

SAA1024

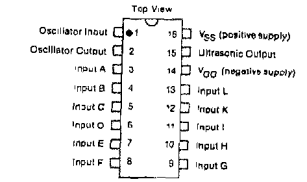
Remote Control System 1/30 Channel Transmitter

FEATURES

- 30 channels. 346.4Hz spacing in the range 34-44KHz.
- 9V battery operation.
- 4.4336MHz TV crystal master oscillator.
- Touch or mechanical keyboard, 1 of 5 and 1 of 6 coding.
- Low standby current drain (15 μA).

PIN CONFIGURATION

16 LEAD DUAL IN LINE

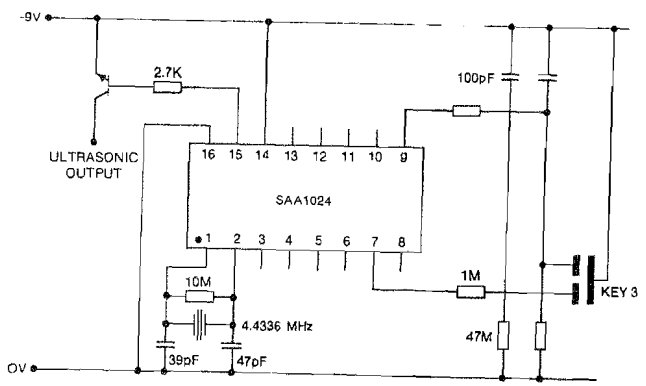


DESCRIPTION

The Transmitter allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990 KHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 15μA. As soon as a valid input code is applied the main circuit is powered up and transmission commences.

The code input can be generated by either a mechanical keyboard or a touch plate.

TRANSMITTER WITH TOUCHPLATE INPUT



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin	+0.3 to −12 Volts
Output current	10mA
Storage temperature range	−65°C to +150°C
Ambient operating temperature range	−10°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = −7 to −10V
Operating Temperature (T_A) = −10°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See diagram for external components.
Output Frequencies	—	See Table	—		
Input logic '0'	—	—	-0.5	V	
Input logic '1'	-4	—	—	V	
Input leakage	—	—	200	nA	at 70°C, Vin = −4V
Output On Resistance	—	500	—	Ω	to V_{SS}, V_{OUT} = −1V
Output Off Resistance	—	1.5	—	KΩ	to V_{DD}, V_{OUT} = V_{DD}+0.5V
Standby current drain	—	—	15	μA	
Operating current drain	—	6.0	—	mA	

**Typical values are at −25°C and nominal voltages

ULTRASONIC FREQUENCIES

Crystal = 4.4336MHz (code in negative logic)

Key	Frequency	A	B	C	D	E	F	G	H	I	K	L
1	33,945 Hz	0	0	0	0	1	0	0	1	0	0	0
2	34,291 Hz	0	0	0	0	1	0	0	0	0	0	1
3	34,638 Hz	0	0	0	0	1	0	1	0	0	0	0
4	34,984 Hz	0	0	0	0	1	0	0	0	0	1	0
5	35,330 Hz	0	0	0	0	1	1	0	0	0	0	0
6	35,677 Hz	0	0	0	0	1	0	0	0	1	0	0
7	36,023 Hz	1	0	0	0	0	1	0	0	0	0	0
8	36,370 Hz	1	0	0	0	0	0	0	0	1	0	0
9	36,716 Hz	0	1	0	0	0	1	0	0	0	0	0
10	37,062 Hz	0	1	0	0	0	0	0	0	1	0	0
11	37,409 Hz	0	0	1	0	0	1	0	0	0	0	0
12	37,755 Hz	0	0	1	0	0	0	0	0	1	0	0
13	38,101 Hz	0	0	0	1	0	1	0	0	0	0	0
14	38,448 Hz	0	0	0	1	0	0	0	0	1	0	0
15	38,794 Hz	1	0	0	0	0	0	1	0	0	0	0
16	39,141 Hz	1	0	0	0	0	0	0	0	0	1	0
17	39,487 Hz	0	1	0	0	0	0	1	0	0	0	0
18	39,833 Hz	0	1	0	0	0	0	0	0	0	1	0
19	40,180 Hz	0	0	1	0	0	0	1	0	0	0	0
20	40,526 Hz	0	0	1	0	0	0	0	0	0	1	0
21	40,872 Hz	0	0	0	1	0	0	1	0	0	0	0
22	41,219 Hz	0	0	0	1	0	0	0	0	0	1	0
23	41,565 Hz	1	0	0	0	0	0	0	1	0	0	0
24	41,911 Hz	1	0	0	0	0	0	0	0	0	0	1
25	42,258 Hz	0	1	0	0	0	0	0	1	0	0	0
26	42,604 Hz	0	1	0	0	0	0	0	0	0	0	1
27	42,951 Hz	0	0	1	0	0	0	0	1	0	0	0
28	43,297 Hz	0	0	1	0	0	0	0	0	0	0	1
29	43,643 Hz	0	0	0	1	0	0	0	1	0	0	0
30	43,990 Hz	0	0	0	1	0	0	0	0	0	0	1

Remote Control System I/30 Channel Receivers

FEATURES

- 30 Control Channels.
- 16 TV Channels.
- 3 Analog Channels
- ON/OFF Channel.
- Normalize Control
- Local Control.
- Uses 4.4MHz TV Crystal

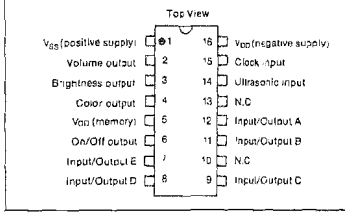
DESCRIPTION

The Receiver has 30 control channels, each channel being allocated a separate ultrasonic frequency. Sixteen of the channels are allocated to selection of TV programs, six are used to control three analog outputs, one for On/Off, one for Normalizing, one for Muting and five are left spare. All channels are output on a 5 line binary bus. The bus is also used as an input for local control.

The analog channels have a pulse width modulated output with 30 possible values, the time taken to go from maximum to minimum being 5.5 seconds. The Normalize button sets the outputs approximately to their mid-point.

The ON/OFF channel toggles every time it is activated, there is a delay of approximately 0.7 seconds to prevent accidental operation.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



To prevent false operation the frequency of the ultrasonic input is measured in the following manner. As soon as the signal appears a 23mSec. timer is started, at the end of this period the room reflections will have died away.

The frequency is then measured for 23mSec. and the appropriate output activated. If at any time a signal is received with a period shorter than 18μSec. or longer than 36μSec. the receiver is reset. Out of band and noisy signals are therefore rejected.

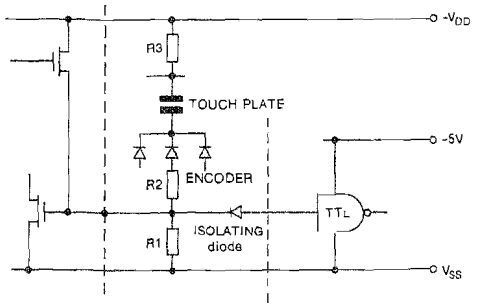


Fig.1 INPUT/OUTPUT CIRCUIT

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{SS}	Positive supply
16	V_{DD}	Negative supply 18V nominal.
5	V_{DD} (memory)	Negative supply to D/A store, allowing the analog values to be retained with very low power consumption (Typ. 0.2mA at 10V)
15	Clock Input	This pin is driven by a 4.4336MHz crystal oscillator. The input signal should be a minimum of 4V peak to peak capacitively coupled
14	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 300 mV peak to peak. The first incoming pulse triggers a 23.1ms timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1ms periods. If the measurements produce a comparison, an output pulse 23.1ms long is generated after a further pause of 46.2ms. With continuous input signals an output pulse is generated every 184.8ms. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18μSec or greater than 36μSec the signal is rejected and the receiver is set back to the start conditions and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of ±0.51% can be tolerated and at the highest ±0.39%.
2, 3, 4	Analog Outputs	These outputs are in the form of a pulse, the mark to space ratio of which can be changed in 30 steps from 1:30 to 30:1, the repetition frequency being 8.99KHz. The mark space ratio is incremented by one step about 115mSec after the start of an ultrasonic command, thereafter it is incremented every 184.8mSec. The output stage is an open drain MOS transistor which appears as a 1 KOhm (Max.) resistor connected to V_{SS} when ON and an open circuit when OFF. At power ON the outputs are normalized to the following mark:space ratios: Color Output 16:15 Brightness Output 18:13 Volume Output 10:21 When command 4 (Normalize) is received, Color and Brightness are reset to their normalized values. Volume is unchanged. When command 2 (Mute) is received Volume is turned OFF, a further command re-enables the output. A delay of approximately 0.7 seconds is built in to this control to prevent false operation. When the Volume output is muted, the Volume Up and Down commands are blocked. The Muting is cancelled if either the Muto command is repeated or an ON command is received.
6	ON/OFF Output	In the SAA-1025-01 version this output is toggled ON and OFF by the reception of command 1. In the SAA-1025-02 version, command 1 will only turn the output OFF. The command must be present for 0.7 sec. At power ON the output is set to the OFF condition. When in the OFF condition the Analog outputs are prevented from changing. Also, when OFF, any one of the 16 channels for selecting TV programs, if present for 0.7 seconds, will change this output to the ON condition. However, these channels will not switch the output to OFF. The output can also be switched ON by connecting pin 6 to V_{SS} for 10 microseconds.
7, 8, 9, 11, 12	Input/Output A, B, C, D, E	These pins have the dual function of receiving input commands from a local keyboard or touch plate and for providing output control signals in response to commands from the transmitter or the keyboard. When the receiver is inactive the pins are held to within 1 Volt of Vss by R1 (Fig. 1), if a touch contact is activated current flows through R3 and R2 (Safety isolating resistors) into R1 driving the input negative. When the input voltage exceeds 4 Volts for at least 10uSec the command is accepted and after a processing time of 46.2mSec an output pulse 23.1mSec long is generated. During the output pulse the output pin is driven negative by the output transistor. The output current is sufficient to drive TTL. When commands are received from both the remote transmitter and the local keyboard the local command takes precedence.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin	+0.3 to -20V
Output Current	10mA
Storage Temperature Range	-65°C to +150°C
Ambient Operating Temperature Range	-20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = OV Fc = 4.4336MHz

V_{DD} = -16.5 to -19.5V Operating Temperature (T_A) = -20°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Logic '0'	+0.3	—	-1	Volts	
Logic '1'	-4	—	-19.5	Volts	
Capacitance	—	—	10	pF	
Ultrasonic Input	0.3	—	V_{DD}	Vp-p	capacity coupled
Inputs A-E					
Logic '0'	+0.3	—	-1	Volts	
Logic '1'	-4	—	-19.5	Volts	
Outputs A—E					
Logic '0'	—	—	-0.5	Volts	RL = 4.7M to V_{SS}
Logic '1'	-5.5	—	—	Volts	Iout = 1.8mA (Fig.1)
On/Off Output					
Off leakage	—	—	10	µA	Vout = -19.5 Volts
On resistance	—	—	1	KOhm	Vout = -1V (resistance to V_{SS})
Analog Outputs					
Off leakage	—	—	10	µA	Vout = -19.5 Volts
On resistance	—	—	1	KOhm	Vout = -1V (resistance to V_{SS})
Output frequency	—	8.99	—	KHz	
Increment time per step	—	184.8	—	mSec	
Memory Supply Current	—	0.2	—	mA	V_{DD}(mem) = -10V
Chip Supply Current	—	20	—	mA	

**Typical values are at +25° C and nominal voltages.

TYPICAL CHARACTERISTIC CURVE

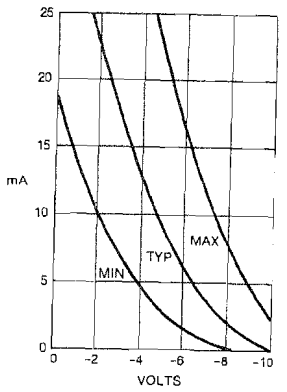


Fig.2 OUTPUT CHARACTERISTICS

FREQUENCY/CHANNEL ALLOCATIONS

F = Channel Select Clock frequency 4.4336 MHz Output in Negative logic

CH	Frequency Hz	Channel Function	Output Code A	B	C	D	E
1	33,944.89	ON/OFF (-01) or OFF (-02)	1	0	0	0	0
2	34,291.21	Mute	1	0	0	0	1
3	34,637.85	Color up	0	1	0	0	0
4	34,984.02	Normalize	0	1	0	0	1
5	35,330.40	Color down	1	1	0	0	0
6	35,676.76	Z1	1	1	0	0	1
7	36,023.15	Brightness up	0	0	1	0	0
8	36,369.53	Z2	0	0	1	0	1
9	36,715.91	Brightness down	1	0	1	0	0
10	37,062.28	Z3	1	0	1	0	1
11	37,408.66	Volume up	0	1	1	0	0
12	37,755.03	Z4	0	1	1	0	1
13	38,101.41	Volume down	1	1	1	0	0
14	38,447.79	Z5	1	1	1	0	1
15	38,794.16	F1	0	0	0	1	0
16	39,140.54	F2	0	0	0	1	1
17	39,486.92	F3	1	0	0	1	0
18	39,833.29	F4	1	0	0	1	1
19	40,179.67	F5	0	1	0	1	0
20	40,526.05	F6	0	1	0	1	1
21	40,872.42	F7	1	1	0	1	0
22	41,218.80	F8	1	1	0	1	1
23	41,565.18	F9	0	0	1	1	0
24	41,911.55	F10	0	0	1	1	1
25	42,257.93	F11	1	0	1	1	0
26	42,604.31	F12	1	0	1	1	1
27	42,950.68	F13	0	1	1	1	0
28	43,297.06	F14	0	1	1	1	1
29	43,643.43	F15	1	1	1	1	0
30	43,989.81	F16	1	1	1	1	1

These channels also give an ON command

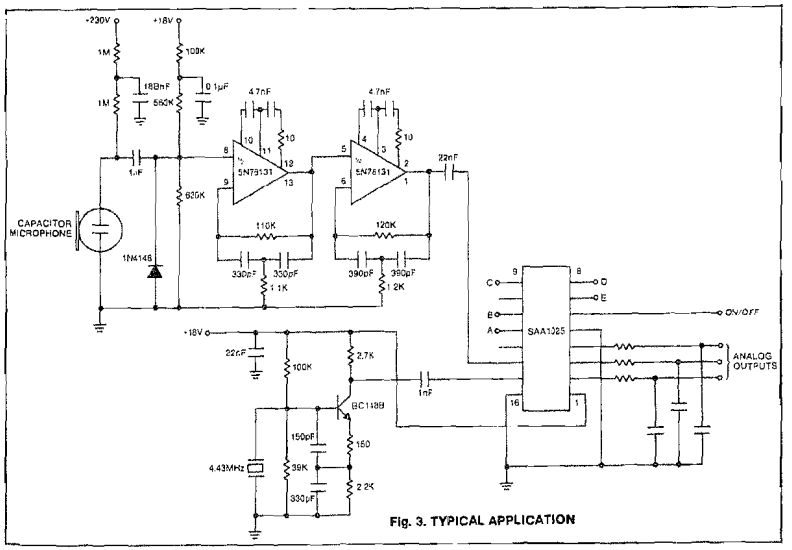


Fig. 3. TYPICAL APPLICATION

Remote Control System II/23 Channel Transmitters

FEATURES

- Ultraaonic or Infrared transmission
- 23 Direct channels of information
- Direct drive for 40KHz transducer
- Power consumption only during keying of information.
- AY-5-8410 — local control at receiver
  AY-5-8411 — remote control operates on 9V battery
- Keyboard bounce protection built in.
- No external oscillator is required
- Local transmitter wire-OR'ed to receiver

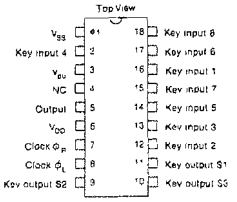
DESCRIPTION

The AY-5-8410/8411 transmitter provides the electronics to transmit 23 channels of information. The transmission is in pulse code modulated form suitable for either ultrasonic or infrared transmission. The transmitter will drive a 40KHz transducer either directly or via a step-up transformer. When any key is depressed, battery power is applied to the chip; power is removed at the end of the code sequence following the release of the key. The requirement for a separate on/off switch is avoided. The keyboard is an 8 × 3 matrix as shown on the next page. Key bounce protection is incorporated. A stable on-chip oscillator is also provided.

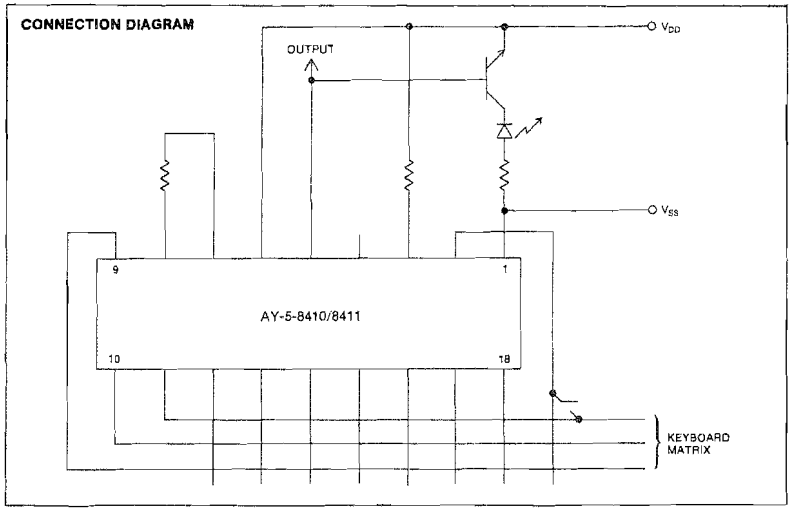
If an local keyboard is required, an additional transmitter chip can be used to encode the local keyboard and the chip output can be wire-OR'ed with the output from the receive transducer amplifier before being fed to the receiver chip.

PIN CONFIGURATION

18 LEAD DUAL IN LINE



CONNECTION DIAGRAM



PIN FUNCTIONS

Key Lines S1, S2, S3
These key lines form part of the key matrix as shown above and are strobe signals which each go to logic '0' in sequence.

Key Inputs K1-K8
Those key lines form part of the key matrix as shown above and they are connected to strobe lines S1, S2 or S3 when appropriate keys are depressed.

Ultrasonic Output
The ultrasonic output is a three state push pull output which goes to logic 1 between trains of pulse in a data block
A transducer or step up transformer can be connected between the ultrasonic output and V_{DD}.

ϕR and ϕL
These are the oscillator input pins. The chip frequency is not critical except in so far as is necessary to satisfy the requirements of the ultrasonic transducers.
The chip may be driven from an external clock by connecting the clock to both ϕR and ϕL linked together

V_{SS}
Ov or positive supply

V_{DD}
Negative supply (nominelly 9 volts for the AY-5-8411)

V_{pu}
This pin is concerned with automatic circuit start up and should be connected to V_{DD} by a 2.2Mohm resistor.

4A

TRANSMITTER KEY MATRIX

Key Strobe / Input Line	S 2	S 3	S 1
1	Ch 24	16	16
2	9	17	25
3	10	18	26
4	11	19	27
5	12	20	28
6	13	21	29
7	14	22	30
8	15	23	31

NOTE:
Channels are the codes that are output by the AY-5-8420 receiver.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature range ..... -65°C to +150°C
Ambient Operating Temperature range ..... 0°C to +70°C

*Exceeding these retings could cause permanent damage Functional operation of these devices at the conditions is not implied — operating ranges are specified below

Standard Conditions (unless otherwise noted

V_{SS} = 0V
V_{DD} = -9V Nominal (AY-5-8411)
-15V Nominal (AY-5-8410)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min.	Typ*	Max.	Units	Conditions
Inputs					
Clocks, Key lines 1-8					
Logic 0	-0.3	—	-1	Volts	
Logic 1	-3	—	V_{DD}	Volts	
Outputs					
Strobes S1, S2, S3	—	2.5	—	Konms	Output at -7V
Ultrasonic output	—	100	—	ohms	
Supply Current:					
Standby Mode	—	6	—	µA	
Transmitting Mode	—	2	—	mA	Chip alone

*Typical values are at -25°C and nominal voltages

AY-5-8420

PRELIMINARY INFORMATION

Remote Control System II/31-63 Channel Receiver

FEATURES

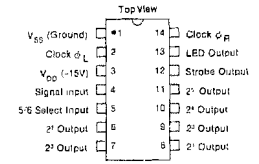
- Ultrasonic or Infrared reception.
- Up to 31 or 63 channels of information
- On board oscillator — external oscillator optional
- Automatic power on clear
- Local control from wire-OR of transmitter
- Error detection is contained
- Output provided to show informtin being received

DESCRIPTION

The AY-5-8420 provides the elctronics to produce an ultrasonic or infrared remote control receiver which, with an appropriate transmitter, can accept up to 63 channels of information. An on chip oscillator is provided, the frequency of which is non critical (≈66KHz). The oscillator frequency is set by one external resistor; an external oscillator can be used if required. Two outputs are provided to indicate that data has been received and is ready for use. Automtic internal power-on-clear is provided.

Error checking bits are transmitted with the code, these are interrograted by the receiver and prevent it from accepting incorrect data caused by attenuation, reflection or multiple path propagation effects. If the first received block of data is not accepted due to introduced errors, the receiver logic resets and attempts to accept the next block. Data blocks are repeatedly transmitted whenever the transmitter is keyed.

PIN CONFIGURATION
14 LEAD DUAL IN LINE



PIN FUNCTIONS

V_{SS}
0 Volts or positive supply.

V_{DD}
Negative supply (15V nominal).

Clock Inputs ϕR, ϕL

The clock frequency is determined by the value of a resistor connected between ϕR and ϕL.

ϕR and ϕL may be connected together and overdriven by an external clock input.

Signal Input

The input should be driven from an amplifier output stage. The receiver is insensitive to input frequency except in so far as is necessary to satisfy the requirements of the transducers.

A local keyboard input can be wire-OR'ed. The frequency is set to approximately 66KHz with a single resistor.

5/6 Select Input

This pin alters the function of the receiver to enable it to accept data from either a 5 bit (31 channel) or 6 bit (63 channel) transmitter. With the pin not connected the receiver functions in the 5 bit mode. With the pin connected to V_{SS} the receiver functions in 6 bit mode.

Outputs 2^5, 2^1, 2^2, 2^3, 2^4, 2^5

The six outputs are latching outputs which retain the data until it is replaced by new input data. The outputs are open ended and clamp to 0 Volts with no output data present.

The output codes change state midway through the end code following correct reception of a data block.

Power-on-clear sets the outputs to an all ones state when power is first applied.

LED

This signal can be used to drive an indicator to show that new data has been received.

The LED output is normally at 0 Volts and goes open circuit simultaneous with the outputs changing. The signal remains in this state during the time that the transmitter is keyed and the receiver is receiving input signals. The signal goes to 0 volts 32ms after the input signals cease.

By gating the LED output with a discrete decode of the outputs 1,2,4,8,16,32 a signal is obtained to drive an analog function i.e. volume up. Such a signal would be present only during the time that the transmitter was keyed.

Strobe

The strobe output is open ended and clamps to 0 Volts.

The clamp is released 60μsec after the data on outputs 1,2,4,8,16,32 has changed and is re-applied 60μ sec later.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -15V nominal
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min.	Typ*	Max	Units	Conditions
Inputs					
Clock,					
Signal,					
5/6 Select:					
Logic 0	+0.3	—	-1	Volts	
Logic 1	-3	—	V_{DD}	Volts	
Outputs					
A-F,					
LED,					
STROBE:					
Logic 0 sink current	—	2	—	mA	2V drop
Oscillator frequency	—	66	—	kHz	

*Typical values are at +25° C and nominal voltages.

4A

Remote Control System III/30 Channel Transmitter

FEATURES

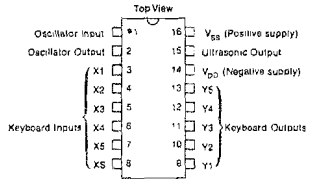
- 30 channels 346.4Hz spacing in the range 34-44KHz.
- P-channel 9V battery opertion.
- 4.4336MHz TV crystal master oscillator.
- 5 × 6 matrix keyboard input.
- Low standby current drain (10μA), max.
- Compatible with SAA1025, SAA1130, AY-5-8460 and AY-5-8461 receivers.

DESCRIPTION

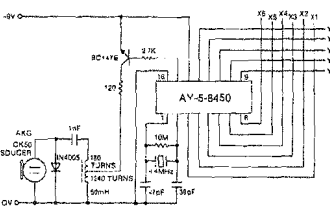
The AY-5-8450 allows the transmission of 30 commands using 30 different ultrasonic frequencies in the range 33.945 to 43.990KHz. It is designed for battery operation and uses a low cost TV crystal as the master oscillator. When inactive the circuit is in a standby mode having a current drain of less than 10μA. As soon as a key is depressed the main circuit is powered up and transmission commences.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



CONNECTION DIAGRAM



OUTPUT FREQUENCIES Clock Frequency: 4.4336MHz

Key	Frequency (Hz)	SAA1025 Receiver Command
X1 Y1	33944.89	Off/On
X1 Y2	37062.28	Z3
X1 Y3	37408.66	Volume Up
X1 Y4	37755.03	Z4
X1 Y5	38101.41	Volume Down
X2 Y1	34291.21	Mute
X2 Y2	38447.97	Z5
X2 Y3	38794.16	F1
X2 Y4	39140.54	F2
X2 Y5	39486.92	F3
X3 Y1	34637.65	Color Up
X3 Y2	39833.29	F4
X3 Y3	40179.67	F5
X3 Y4	40526.05	F6
X3 Y5	40872.42	F7
X4 Y1	34984.02	Normalize
X4 Y2	41218.80	F8
X4 Y3	41565.18	F9
X4 Y4	41911.55	F10
X4 Y5	42257.93	F11
X5 Y1	35330.40	Color Down
X5 Y2	35676.78	Z1
X5 Y3	3602315	Brightness Up
X5 Y4	42604.31	F12
X5 Y5	42950.68	F13
X6 Y1	36369.53	Z2
X6 Y2	36715.91	Brightness Down
X6 Y3	43297.06	F14
X6 Y4	43643.43	F15
X6 Y5	43989.81	F16

PIN FUNCTIONS

Pin No.	Name	Function
1.	Oscillator Input	The Quartz crystal network is connected to these pins.
2.	Oscillator Output	
3.	X1	The keys are in the form of an XY matrix. As soon as a key closure is detected the chip is powered up and the keyboard is scanned at 3KHz. When it has been determined what key has been pressed the appropriate frequency is transmitted. If more than one key is pressed the chip ceases to transmit.
4.	X2	
5.	X3	
6.	X4	Keyboard Inputs
7.	X5	
8.	X6	
9.	Y1	
10.	Y2	
11.	Y3	Keyboard Outputs
12.	Y4	
13.	Y5	
14.	V_{DD}	Negative supply (-8V nom)
15.	Ultrasonic output	Off until key pressed
16.	V_{SS}	Positive supply (ground)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -12 Volts
Output current 10mA
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... -10°C to +70°C

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -7 to -10V
F clock = 4.4336MHz
T_A = 0°C to 70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Frequency	—	4.4336	—	MHz	See the Connection Diagram for external components
Key Contact Resistance:					
ON	—	—	100	Ω	
OFF	1	—	—	MΩ	
Key Capacitance	—	—	20	pF	
Output:					
On Resistance	—	—	600	Ω	To V_{SS}, V_{OUT} = -1V
Off Resistance	—	—	3	KΩ	To V_{DD}, V_{OUT} = V_{DD} +0.5V
Standby Current Drain	—	5	10	μA	
Operating Current Drain	—	12	—	mA	

Remote Control System III/16 Channel Receivers

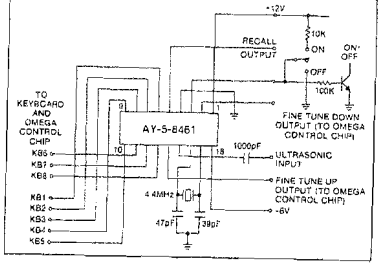
FEATURES

- 16 Control Channels; 0 to 9, Volume up and down (AY-5-8460), Recall, ON/OFF, Fine Tune up and down (AY-5-8461), channel up and down.
- Outputs in 3×5 matrix format for driving Omega.
- On chip oscillator using 4.4336MHz TV Crystal.

DESCRIPTION

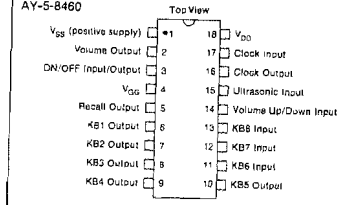
The AY-5-8460/8461 is a 16 channel ultrasonic remote control receiver designed to be compatible with the GI Omega TV digital tuning system. It can be operated by either the AY-5-8450 or the SAA 1024 remote control transmitters.

AY-5-8461 CONNECTION DIAGRAM

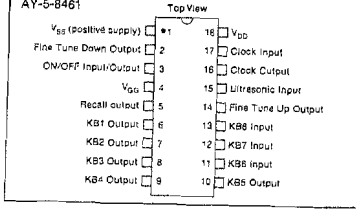


PIN CONFIGURATIONS
18 LEAD DUAL IN LINE

AY-5-8460 Top View



AY-5-8461 Top View



FREQUENCY ALLOCATIONS

AY-5-8460

Frequency Hz	Function	Output Code
37 0620	0	KB1/KB6
37 409	Recall	—
37 755	On/Off	—
38 101	Channel Down	KB4/KB8
38 448	1	KB2/KB6
38 794	2	KB3/KB6
39 140	3	KB4/KB6
39 487	Channel Up	KB5/KB8
39 833	4	KB5/KB6
40 180	5	KB1/KB7
40 526	6	KB2/KB7
40 872	Volume Down	—
41 219	7	KB3/KB7
41 565	8	KB4/KB7
41 912	9	KB5/KB7
42 258	Volume Up	—

AY-5-8461

Frequency Hz	Function	Output Code
37 0620	0	KB1/KB6
37 409	Recall	—
37 755	On/Off	—
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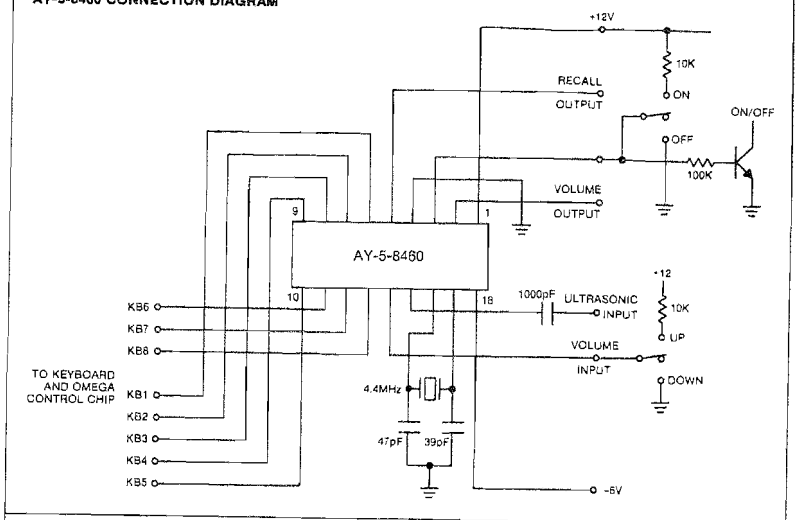
39 487	Channel Up	KB5/KB8
39 833	4	KB5/KB6
40 180	5	KB1/KB7
40 526	6	KB2/KB7
40 872	Fine Tune Down	—
41 219	7	KB3/KB7
41 565	8	KB4/KB7
41 912	9	KB5/KB7
42 258	Fine Tune Up	—

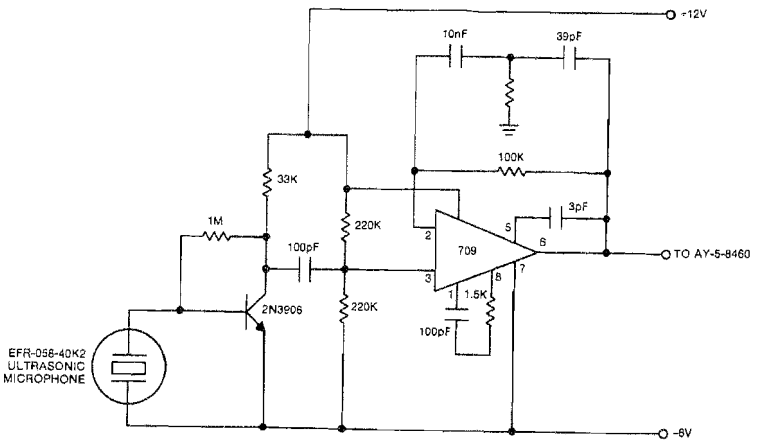
PIN FUNCTIONS

Pin No.	Name	Functions
1	V_{SS}	Ground
1	Volume Output (AY-5-8460)	This output is in the form of a pulse, the mark of space ratio of which can be changed in 125 steps from 1:126 to 126:1, the repetition frequency being 8.79KHz The mark space ratio is incremented by one step about 115mSec after the start of an ultrasonic command, thereafter it is incremented every 46.2mSec. At power ON the output is normalized to a mark space ratio of 63:64. The output is also controlled by pin 14
2	Fine Tune Down Output (AY-5-8461)	This output is connected to the corresponding pin on the Omega system. It is at logic '1' for the duration of the ultrasonic command.
3	ON/OFF Output/Input	This output is toggled ON and OFF by reception of the corresponding ultrasonic command. At power up the output is set to the OFF state. When in the OFF state the Volume output is prevented from changing and the KB outputs are at logic '1', the Fine Tune outputs are at logic '0'. The output may be turned ON by connecting it to V_{SS} via a 10KOhm resistor for 10µs, it may be turned OFF by connecting it to V_{GG}. The Ultrasonic command must be present for at least 0.7 sec. to activate the output.
4	V_{GG}	This pin is externally maintained at V_{DD} +(6V ± 5%), to serve as a ground reference for logic signals which interface with the Omega system.
5	Recall Output	This output is at logic "0" for the duration of the ultrasonic command.
6	KB1 Output	These outputs and inputs are connected to the corresponding pins on the Omega system. A 3×5 matrix keyboard may be connected to the same pins. Maximum capacitance between intersecting matrix lines 20pF.
7	KB2 Output	
8	KB3 Output	
9	KB4 Output	
10	KB5 Output	
11	KB6 Output	
12	KB7 Output	
13	KB8 Output	
14	Volume Up/Down Input (AY-5-8460)	This is a tristate input which provides local control of the Volume Output function of pin 2. Connecting this pin to V_{SS} (V_{DD}) via a 10KOhm resistor causes the mark space ratio to increment (decrement). The input must be activated for 23mSec before the Volume Output begins to change. This input has oriority over any ultrasonic command.
14	Fine Tune Up Output (AY-5-8461)	This output is connected to the corresponding pin on the Omega system. It is at logic '1' for the duration of the corresponding ultrasonic command.
15	Ultrasonic Input	The ultrasonic signal should be capacitively coupled and be at least 500mV peak to peak. The first incoming pulse triggers a 23.1ms timer and after a delay of this period, two measurements of the ultrasonic signal are made over the following two 23.1ms periods. If the measurements produce a comparison an output is generated after a further pause of 46.2ms. The outputs are present for the duration of the ultrasonic command. During the complete receiving time the period of the ultrasonic signal is measured. If it is less than 18usec or greater than 36usec the signal is rejected and the receiver is set back to the start condition and a new measuring cycle commences. The input signals need not be completely accurate for satisfactory reception. At the lowest frequency an error of ± 0.51% can be tolerated and at the highest ± 0.39%.
16	Clock Output	This is the output of the clock oscillator. One side of the crystal is connected to this pin.
17	Clock Input	This is the input of the clock oscillator. The other side of the crystal is connected to this pin.
18	V_{DD}	Negative power supply.

AY-5-8460 CONNECTION DIAGRAM



AY-5-8460 ULTRASONIC PREAMP



ELECTRICAL CHARACTERISTICS

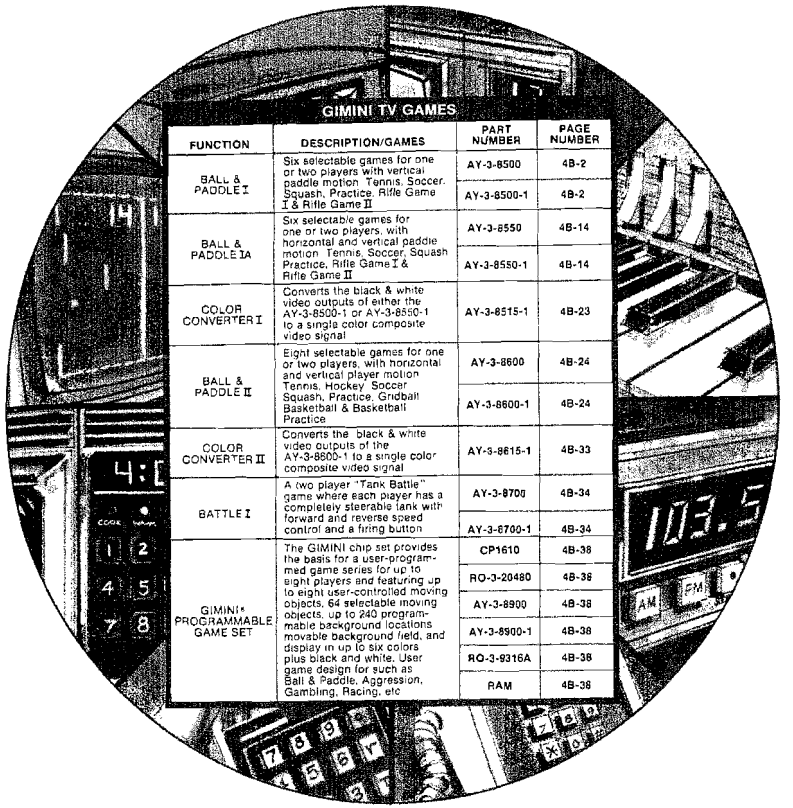
Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -20 Volts
Storage temperature range ..... -65°C to +150°C
Ambient operating temperature range ..... 0°C to +70°C

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{GG} = -12V ± 10%
V_{DD} = V_{GG} — (6V ± 5%)
F = 4.4336MHz
T_{amb} = 0°C to +70°C

Characteristic	Min.	Typ	Max.	Units	Conditions
Clock Oscillator Frequency	—	4.4336	—	MHz	
Ultrasonic Input					
Sensitivity	500	—	25	mVp-p	
Impedance	10	—	—	KOhm	
Keyboard Inputs (KB6-8)					
Pull up resistance	200	—	—	KOhm	to V_{SS}
Logic '0'	—	—	V_{SS} -8	Volts	
Logic '1'	V_{SS} -1.5	—	—	Volts	
Volume Input					
Increment Up	—	—	V_{SS}	Volts	10KOhm to V_{SS}
Increment Down	V_{GG}	—	—	Volts	Short to V_{GG}
No Movement	—	—	—	—	Open Circuit
ON/OFF Input					
ON	V_{SS} -1	—	V_{SS}	Volts	Load 10KOhm to V_{SS} & 100KOhm to V_{GG}
OFF	V_{GG}	—	V_{GG} +0.5	Volts	Short to V_{GG}
Keyboard Outputs (KB1-5)					
Logic '0'	V_{GG}	—	V_{GG} +0.5	Volts	Load 100KOhm to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	Volts	
Recall Output					
Logic '0'	V_{GG}	—	V_{GG} +0.5	Volts	Load 100KOhm to V_{SS}
Logic '1'	V_{SS} -1	—	V_{SS}	Volts	
Fine Tune Outputs					
Logic '0'	V_{GG}	—	V_{GG} +0.5	Volts	Load 100KOhm to V_{GG}
Logic '1'	V_{SS} -1	—	V_{SS}	Volts	
Volume Output					
On Level	V_{SS} -1	—	V_{SS}	Volts	Load 68KOhm to V_{GG}
Off Level	V_{GG}	—	V_{GG} +0.5	Volts	
Pulse Frequency	8.73	—	—	kHz	
ON/OFF Output					
Off	V_{GG}	—	V_{GG} +0.5	Volts	Load 100KOhm to V_{GG}
On	V_{SS} -1	—	V_{SS}	Volts	
Supply Current	—	—	25	mA	



GIMINI TV GAMES

FUNCTION	DESCRIPTION/GAMES	PART NUMBER	PAGE NUMBER
BALL & PADDLE I	Six selectable games for one or two players with vertical paddle motion. Tennis, Soccer, Squash, Practice, Rifle Game I & Rifle Game II	AY-3-8500	4B-2
		AY-3-8500-1	4B-2
BALL & PADDLE IA	Six selectable games for one or two players, with horizontal and vertical paddle motion. Tennis, Soccer, Squash Practice, Rifle Game I & Rifle Game II	AY-3-8550	4B-14
		AY-3-8550-1	4B-14
COLOR CONVERTER I	Converts the black & white video outputs of either the AY-3-8500-1 or AY-3-8550-1 to a single color composite video signal	AY-3-8515-1	4B-23
BALL & PADDLE II	Eight selectable games for one or two players, with horizontal and vertical player motion Tennis, Hockey, Soccer Squash, Practice, Gridball Basketball & Basketball Practice	AY-3-8600	4B-24
		AY-3-8600-1	4B-24
COLOR CONVERTER II	Converts the black & white video outputs of the AY-3-8600-1 to a single color composite video signal	AY-3-8615-1	4B-33
BATTLE I	A two player "Tank Battle" game where each player has a completely steerable tank with forward and reverse speed control and a firing button	AY-3-8700	4B-34
		AY-3-8700-1	4B-34
GIMINI® PROGRAMMABLE GAME SET	The GIMINI chip set provides the basis for a user-programmed game series for up to eight players and featuring up to eight user-controlled moving objects, 64 selectable moving objects, up to 240 programmable background locations, movable background field, and display in up to six colors plus black and white. User game design for such as Ball & Paddle, Aggression, Gambling, Racing, etc	CP1610	4B-38
		RO-3-2048O	4B-38
		AY-3-8900	4B-38
		AY-3-8900-1	4B-38
		RO-3-9316A	4B-38
		RAM	4B-38

GIMINI TV GAMES

MICRO ELECTRONICS

Ball & Paddle I

FEATURES

- Full **COLOR** operation (see page 4B-13)
- 6 Selectable Games - Tennis, soccer, squash, practice and two rifle shooting games.
- 625 Line (AY-3-8500) and 525 Line (AY-3-8500-1) versions.
- Automatic Scoring
- Score display on T.V. Screen. 0 to 15
- Selectable Bat Size
- Selectable Angles
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Realism Sounds
- Shooting Forwards in Soccer Game
- Visually defined area for all Ball Games

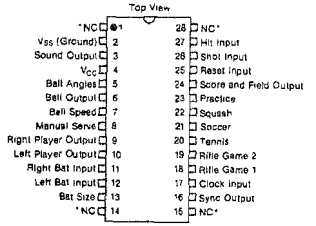
DESCRIPTION

The AY-3-8500 and AY-3-8500-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver

The circuit is intended to be battery powered and a minimum number of external components are required to complete the system. A system diagram is shown below.

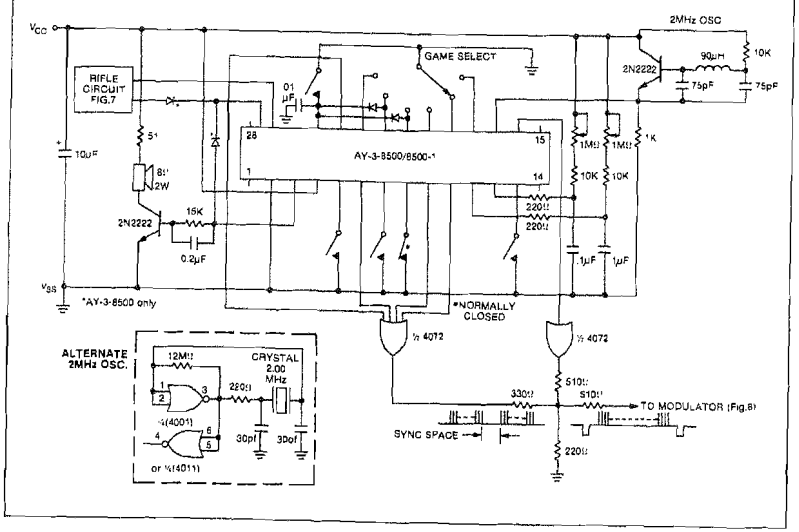
PIN CONFIGURATION

28 LEAD DUAL IN LINE



*Do not use as tie point

SYSTEM DIAGRAM



PIN FUNCTIONS (Pin numbers in parentheses)

Vss (2)
Negative supply input, nominally 0V(GND).

Sound Output (3)
The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds are output on this pin.

Vcc (4)
Positive supply input.

Ball Angles (5)
This input is left open circuit (Logic '1') to select two rebound angles and connected to Vss (Logic '0') to select four rebound angles. When two angles are selected they are ± 20°, when four are selected they are ± 20° and ± 40°. See Fig. 9.

Ball Output (6)
The ball video signal is output on this pin.

Ball Speed (7)
When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to V_{SS} (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8)
This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting this input to V_{SS}.

Right Player Output/Left Player Output (9,10)
The video signals for the right and left players are output on separate pins.

Right Bat Input/Left Bat Input (11,12)
An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot

Bat Size (13)
This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high.

Sync Output (16)
The T.V. vertical and horizontal sync signals are output on this pin. See Fig. 10.

Clock Input (17)
The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 ±1%

Rifle Game 1, Rifle Game 2, Tennis, Soccer, Squash, Practice (18 thru 23)
These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game.

Score and Field Output (24)
The score and field video signal is output on this pin.

Reset (25)
This input is connected momentarily to Vss (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26)
This input is driven by a positive pulse output of a monostable to indicate a "shot"

Hit Input (27)
This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to Vss. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to Vcc.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +12V
Storage Temperature Range ..... -20°C to +70°C
Ambient Operating Temperature Range ..... 0°C to +40°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0°C to +40°C

Characteristics at 25°C and Vcc = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance
Frequency	1.99	2.01	2.03	MHz	of 1K to V_{CC} or V_{SS}.
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V, F = 1MHz
Leakage	—	100	—	µA	
Control Inputs					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Input Impedance	—	1.0	—	M Ohms	Pull up to V_{CC}
Rifle Input	—	1.0	—	M Ohms	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1.0	Volt	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	Volts	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +8.5V

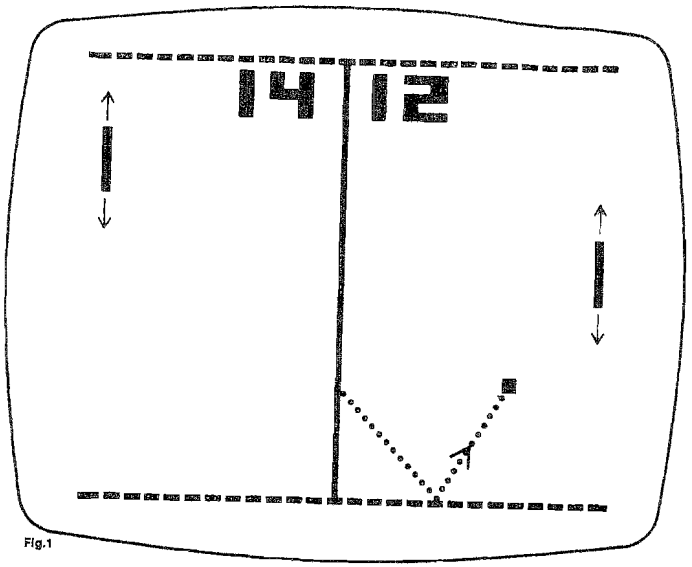


Fig.1

Tennis

With the tennis game the picture on the television screen would be similar to Figure 1 with one 'bat' per side, a top and bottom boundary and a center net. The individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes his 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically towards the side which had just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

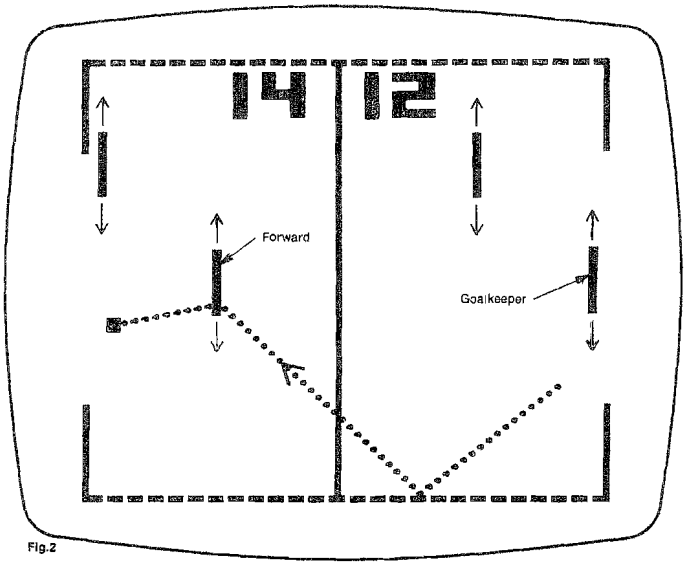


Fig.2

Soccer

The "soccer" type game is shown in Figure 2. With this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' is positioned in the opponent's half of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can intercept the ball, (Figure 2a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used (Figure 2b). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal'.

A 'score' is made in the "soccer" game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

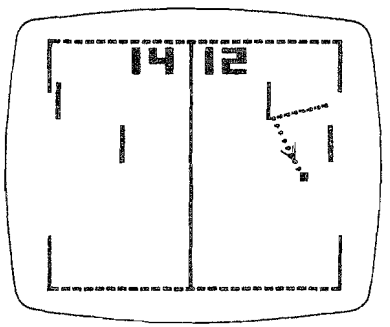


Fig.2a Return of "Goal Save"

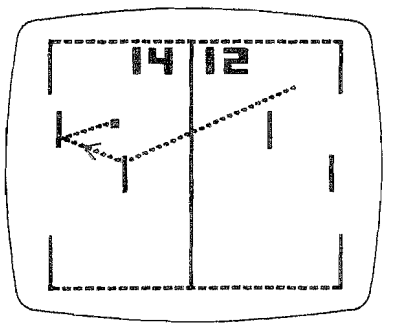


Fig.2b "Shooting" Forward

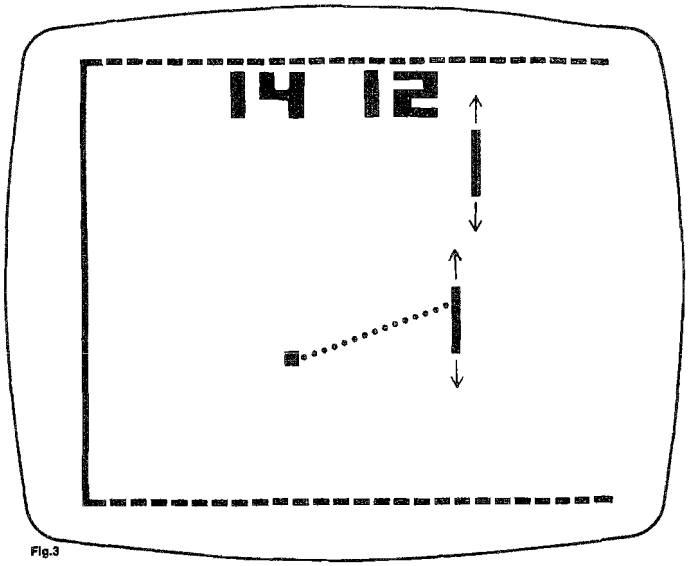


Fig.3

Squash

This game is illustrated in Fig.3. There are two players who alternatoly hit the bell into the court. The right hand player is the one that hits first; it is then the left hand player's turn. Each player is enabled alternately to ensure that the proper sequence of play is followed.

Practice

This game is similar to squash except that there is only one player. See Fig. 4.

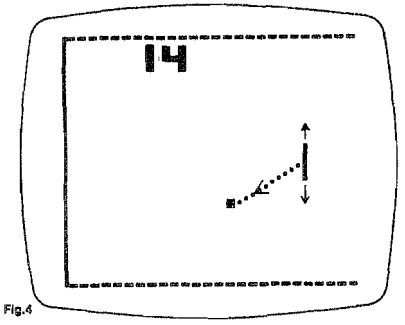


Fig.4

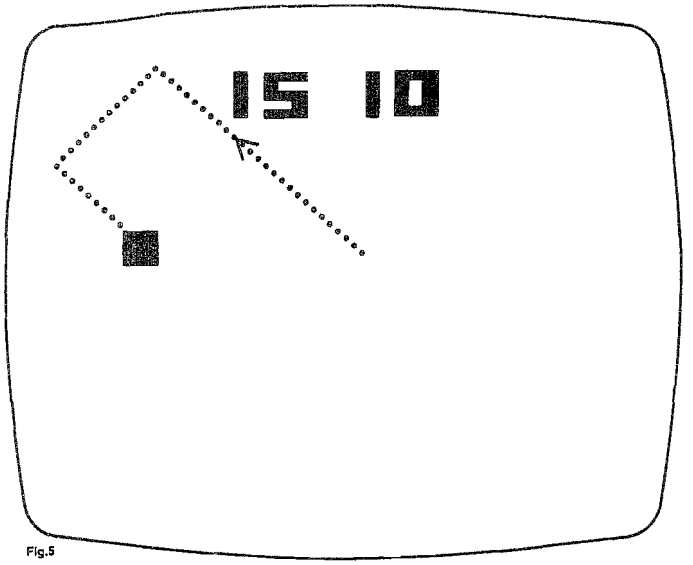


Fig.5

Rifle Game No. 1

This game is illustrated in Fig. 5. It has a large target which bounces randomly about the screen. A photocell in the rifle is aimed at the target. When the trigger is pulled, the shot counter is incremented and, if the rifle is on target, the hit counter is incremented, a hit noise is generated and the target is blanked for a short period. After 15 shots the score appears but the game can still continue without additional scoring.

Rifle Game No. 2

In this game illustrated in Fig. 6, the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as described for Rifle Game No. 1.

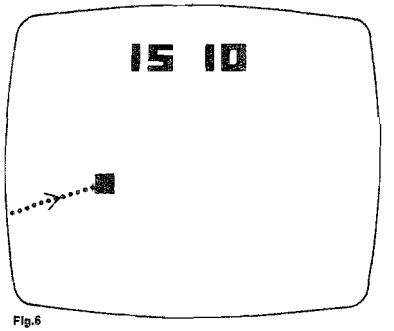
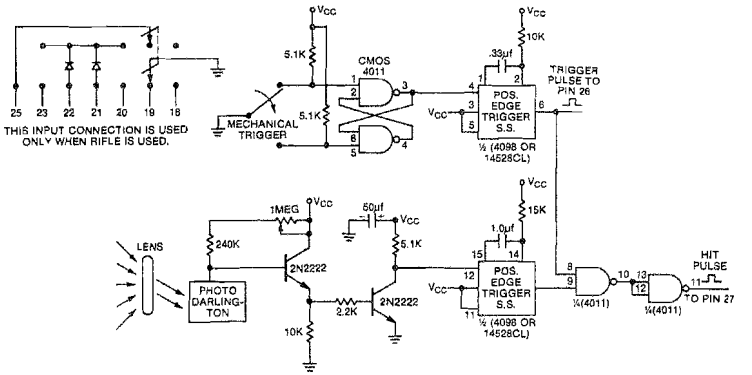
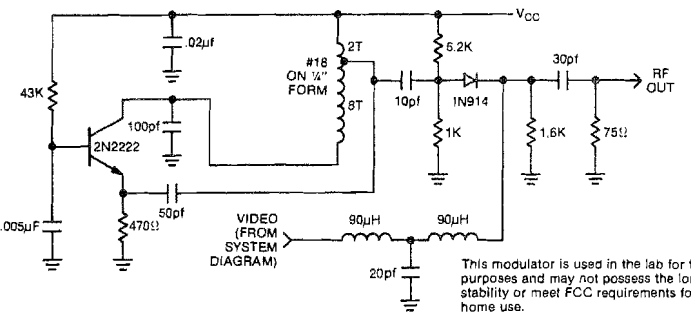


Fig.6



NOTE: Aim rifle at score on TV and adjust 1 meg pot. for max. voltage on pin 12 of the 4098 at a 6 ft. distance. The Voltage at pin 12 should be 0 when there is no light on the TV screen.

Fig.7 RIFLE INTERFACE

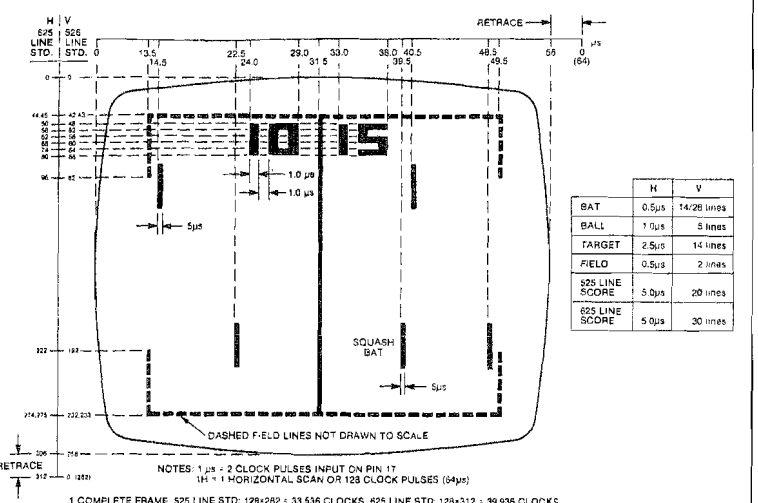


This modulator is used in the lab for test purposes and may not possess the long term stability or meet FCC requirements for home use.

Fig.8 VHF MODULATOR

	Horizontal	Vertical
Slow	± .5µs	2 angles ± 1 line 4 angles ± 3 lines
Fast	± 1µs	2 angles ± 2 lines 4 angles ± 5 lines

Fig.9 ANGULAR MOTION



	H	V
BAT	0.5µs	14/28 lines
BALL	1.0µs	5 lines
TARGET	2.5µs	14 lines
FIELD	0.5µs	2 lines
525 LINE SCORE	5.0µs	20 lines
625 LINE SCORE	5.0µs	30 lines

Fig.10 LOCATION OF DATA OUTPUT PULSES

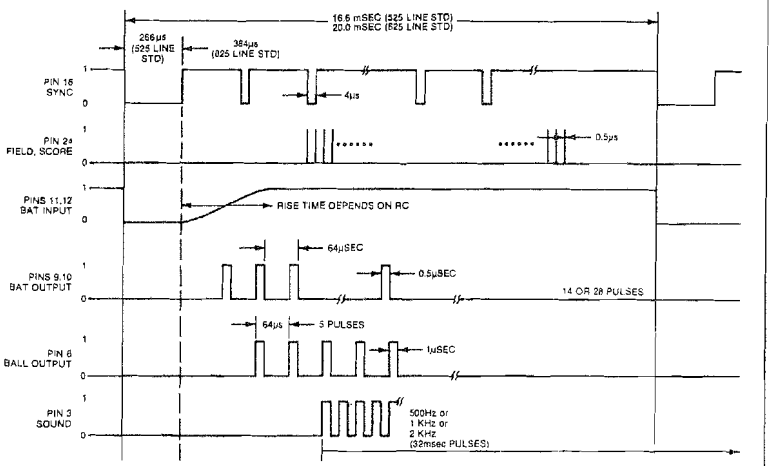


Fig.11 TIMING DIAGRAM

FOUR PLAYER CONFIGURATION

With this option, the basic two player tennis game can be expanded to true four player doubles. Each player is capable of playing the full width of the court.

A variation of this option allows for a three player handicap game with two players against one.

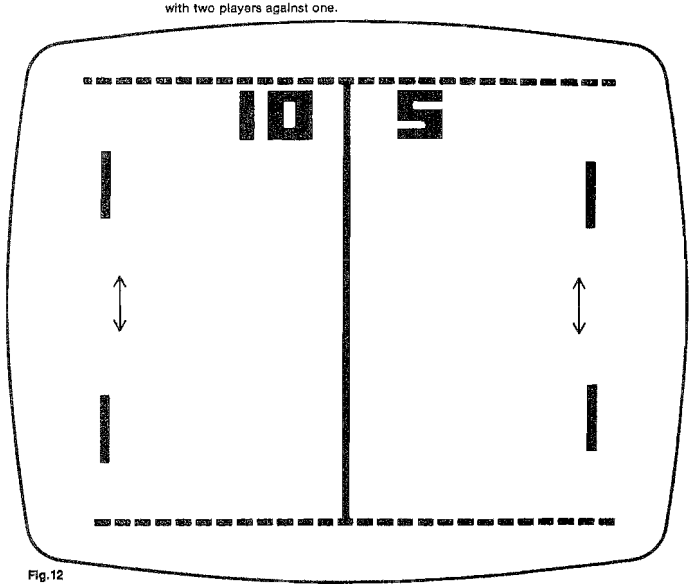


Fig.12

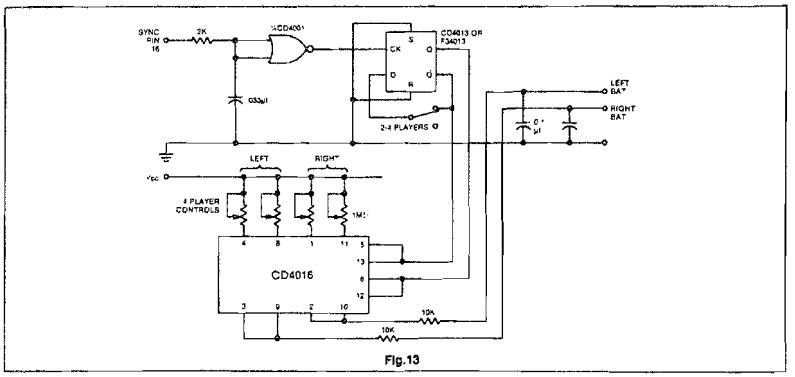


Fig.13

RANDOM BALL SPEED/RANDOM ANGLES

To enhance the excitement and challenge of the various games, this option provides random variations of the ball speed and random changes in the ball rebound angle as the games are being played.

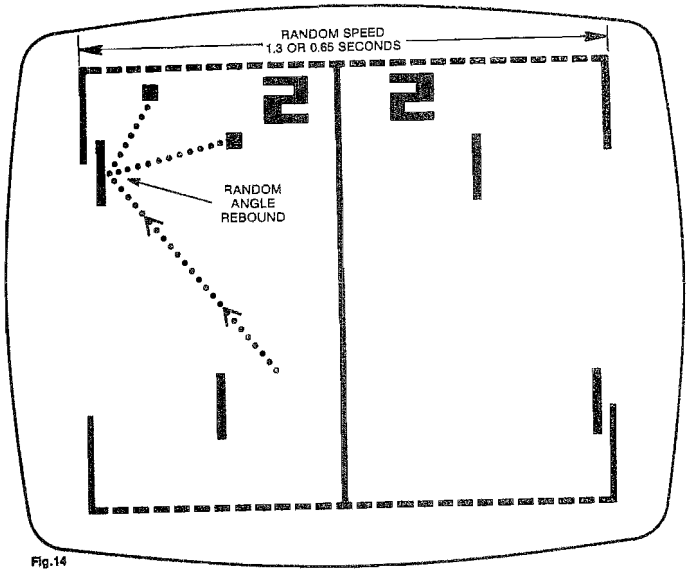


Fig.14

4B

Soccer

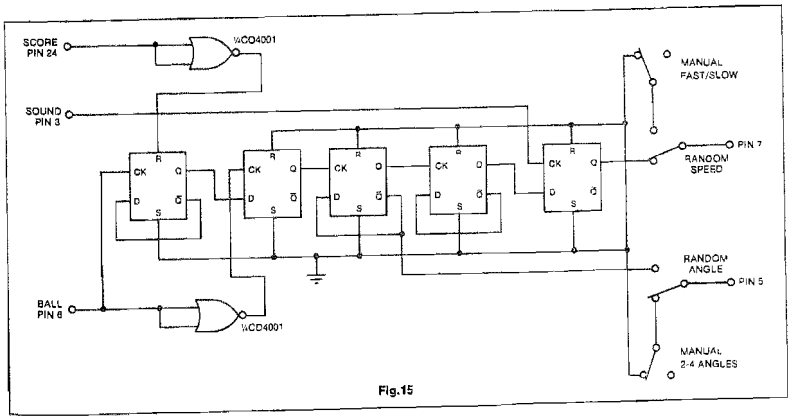


Fig.15

BLACK AND WHITE BATS/GRAY BACKGROUND

This option provides an added factor for player team recognition. The field or court is produced as a gray background with the bats in black and white. This option is particularly helpful for the squash game where the players are positioned close together.

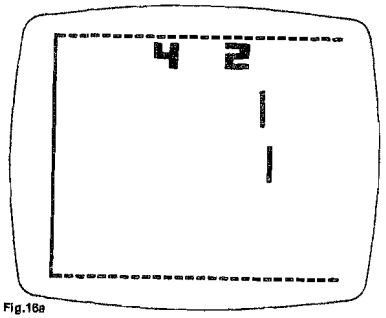


Fig.16a

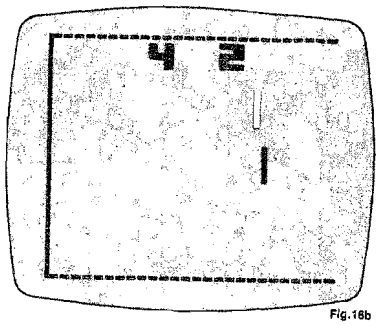


Fig.16b

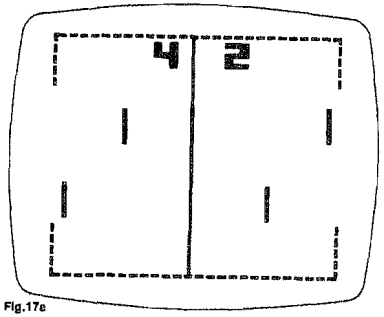


Fig.17a

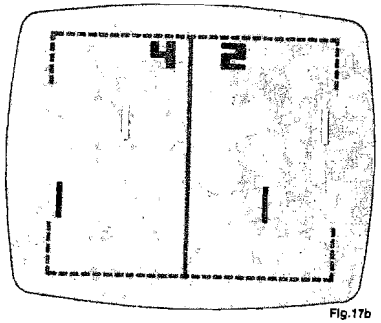
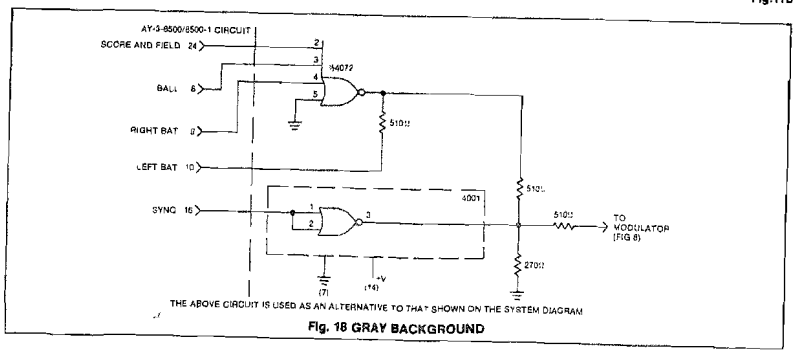


Fig.17b



THE ABOVE CIRCUIT IS USED AS AN ALTERNATIVE TO THAT SHOWN ON THE SYSTEM DIAGRAM

Fig. 18 GRAY BACKGROUND

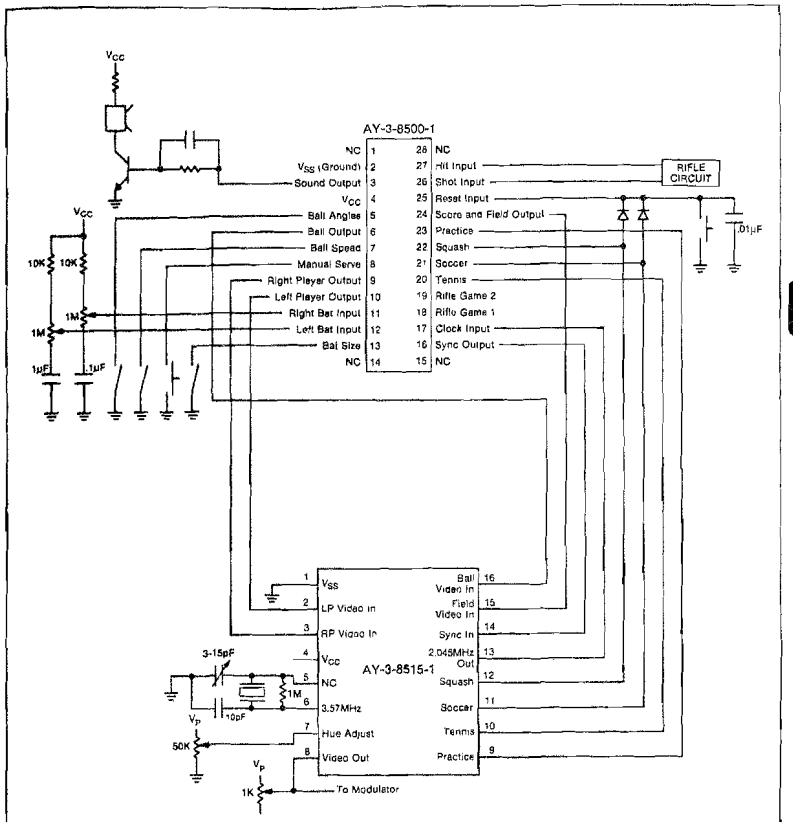


Fig. 19 AY-3-8500-1 FULL COLOR IMPLEMENTATION USING AY-3-8515-1 COLOR CONVERTER CIRCUIT (SEE PAGE 4B-23)

4B

Ball & Paddle IA

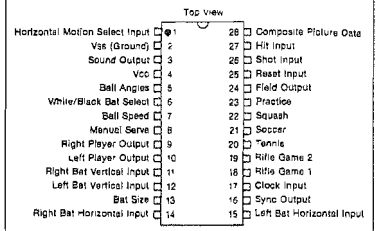
FEATURES

- Full **COLOR** Operation (see page 4B-22)
- 6 Selectable Games - Tennis, soccer, squash, practice and two rifle shooting games
- 625 Line (AY-3-8550) and 525 Line (AY-3-8550-1) versions
- Selectable horizontal motion
- Special Composite outputs for color coding, players and score, ball and boundaries.
- Automatic Scoring
- Score display on T.V Screen. 0 to 15.
- Selectable Bat Size.
- Selectable Angles.
- Selectable Ball Speed
- Automatic or Manual Ball Service
- Realism Sounds.
- Shooting Forwards in Soccer Game.
- Visually defined area for all Ball Games.
- Score color-coded to player.
- Ball output coded to player in Squash
- Practice game scores both hits and misses
- Composite picture data on one pin, and individual video signals for color.
- Pin compatible with AY-3-8500/8500-1

DESCRIPTION

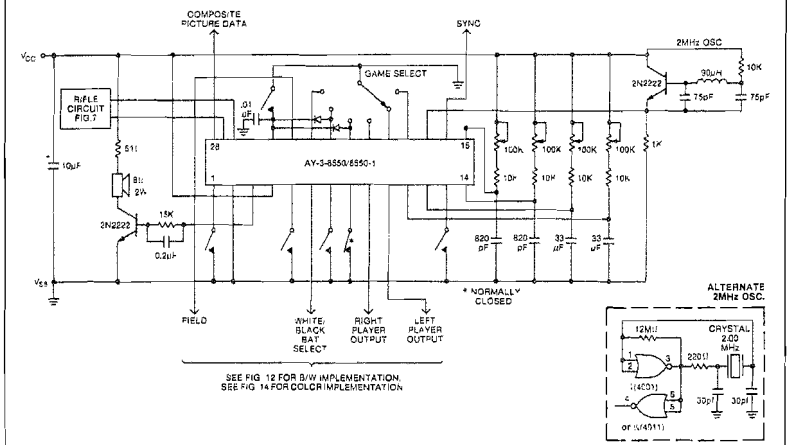
The AY-3-8550 and AY-3-8550-1 circuits have been designed to provide a TV 'games' function which gives active entertainment using a standard domestic television receiver.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



The circuit is intended to be battery powered and a minimum number of external components are required to complete the system. A system diagram is shown below

SYSTEM DIAGRAM



PIN FUNCTIONS

Horizontal Motion Select (1) When connected to V_{SS} (Logic '0'), the horizontal motion controls are enabled. Open circuit fixes paddles at baselines for vertical motion only.

Vss (2) Negative supply input, nominally 0V(GND).

Sound Output (3) The hit (32ms pulse/976Hz tone), boundary reflection (32ms pulse/488Hz tone) and score (32ms pulse/1.95KHz tone) sounds ere output on this pin.

Vcc (4) Positive supply input.

Ball Angles (5) This input is left open circuit (Logic '1') to select two rebound angles and connected to V_{SS} (Logic '0') to select four rebound angles. When two angles are selected they are ± 20°, when four are selected they are ± 20° and ± 40°. See Fig. 9.

White/Black Bat Select (6) Connection to Vcc (Logic '1') inverts the right player output for black right player. This input is pulled to Vss so this circuit may be used in AY-3-8500/8500-1 sockets.

Ball Speed (7) When this input is left open-circuit, low speed is selected (1.3 seconds for ball to traverse the screen). When connected to V_{SS} (Logic '0'), the high speed option is selected (0.65 seconds for ball to traverse the screen).

Manual Serve (8) This input is connected to V_{SS} (Logic '0') for automatic serving. When left open circuit (Logic '1') the game stops after each score. The serve is indicated by momentarily connecting the input to V_{SS}.

Right Player Output/Left Player Output (9,10) Normally positive going video signals representing the right hand player (paddle, score, and when playing Squash, the ball when it is the right hand player's turn to hit) and the left hand player (paddle, score, and ball — except that in Squash the ball is output only when it is the left hand player's turn to hit). When connected to V_{CC}, the output is negative going with the "off" state at V_{CC}.

Right bat Vertical Input/Left Bat Vertical Input (11,12) An R-C network connected to each of these inputs controls the vertical position of the bats. Use a 10K resistor in series with each pot.

Bat Size (13) This input is left open circuit (Logic '1') to select large bats and connected to V_{SS} (Logic '0') to select small bats. For a 19" T.V. screen, large bats are 1.9" and small bats are 0.95" high

Right Bat Horizontal Input/Left Bat Horizontal Input (14,15) An R-C network connected to each of these inputs controls the horizontal position of the bats. Use a 10K resistor in series with each pot.

Sync Output (16) The T.V vertical and horizontal sync signals are output on this pin. Sync must always be one of the signals included in the composite video to the modulator. See Fig. 10.

Clock Input (17) The 2MHz master timing clock is input to this pin. The exact frequency is 2.012160 ± 1%

Rifle Game 1, Rifle Game 2, Tennis, Soccer, Squash, Practice (18 thru 23) These inputs are normally left open circuit (Logic '1') and are connected to V_{SS} (Logic '0') to select the desired game

Field Output (24) The field video signal is output on this pin.

Reset (25) This input is connected momentarily to V_{SS} (Logic '0') to reset the score counters and start a new game. Normally left open circuit.

Shot Input (26) This input is driven by a positive pulse output by a monostable to indicate a "shot"

Hit Input (27) This input is driven by a positive pulse output of a monostable which is triggered by the shot input if the target is on the sights of the rifle

Composite Picture Data (28) This positive going output is the sum of the picture data for the bats, ball, field and score and can be used in lieu of the data on pins 9, 10 and 24. This signal and Sync are the only signals required for black and white operation (see Fig. 12)

NOTE: The "Shot" and "Hit" inputs have on-chip pull-down resistors to V_{SS}. All other inputs (except the "Bat" inputs) have on-chip pull-up resistors to V_{CC}.

ELECTRICAL CHARACTERISTICS (PRELIMINARY INFORMATION)

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... -0.3 to +12V
Storage Temperature Range ..... -20°C to +70°C
Ambient Operating Temperature Range ..... 0°C to +40°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{CC} = +6 to +7V
V_{SS} = 0V
Operating Temperature (T_A) = 0°C to +40°C

Characteristics at 25°C and V_{CC} = +6 Volts	Min	Typ	Max	Units	Conditions
Clock Input					Maximum clock source impedance of 1K to V_{CC} or V_{SS}.
Frequency	1.99	2.01	2.03	MHz	
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	Vcc	Volts	
Pulse Width — Pos.	—	200	—	ns	
Pulse Width — Neg.	—	300	—	ns	
Capacitance	—	10	—	pF	V_{IN} = 0V F = 1MHz
Leakage	—	100	—	µA	
Control Inputs					Max. contact resistance of 1K to V_{SS}
Logic '0'	0	—	0.5	Volts	
Logic '1'	V_{CC}-2	—	V_{CC}	Volts	
Input Impedance	—	1.0	—	M Ohms	Pull up to V_{CC}
Rifle Input	—	1.0	—	M Ohms	Pull down to V_{SS}
Outputs					
Logic '0'	—	—	1.0	Volt	Iout = 0.5mA
Logic '1'	V_{CC}-2	—	—	Volts	Iout = 0.1mA
Power Supply Current	—	40	60	mA	at V_{CC} = +8.5V

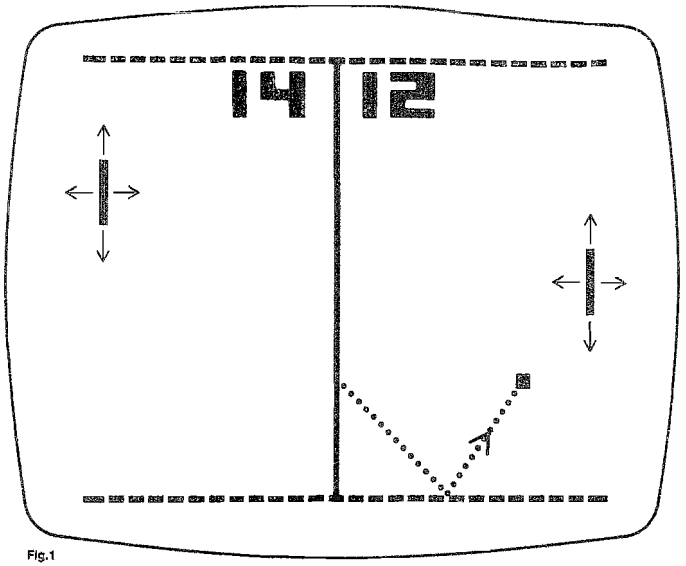


Fig.1

Tennis

With the tennis game the picture on the television screen would be similar to Figure 1 with one 'bat' per side, a top and bottom boundary and a center net. The individual scores are counted and displayed automatically in the position shown. The detail of the game will depend upon the selection of the options. Considering the situation where small bats are used and all angles, after the reset has been applied, the scores will be 0, 0 and the ball will serve arbitrarily to one side at one of the angles. If the ball hits the top or bottom boundary it will assume the angle of reflection and continue in play. The player being served must control his bat to intersect the path of the ball. When a 'hit' is detected by the logic, the section of the bat which made the hit is used to determine the new angle of the ball.

To expand on this, all 'bats' or 'players' are divided logically into four adjacent sections of equal length. When using the four angle option it is the quarter of bat which actually hits which defines the new direction for the ball.

The direction does not depend upon the previous angle of incidence. With the two angle option the top and bottom pairs of the bats are summed together and only the two shallower angles are used to program the new direction for the ball.

When horizontal motion is selected, the players are restricted to the proper side of the net.

The ball will then traverse towards the other player, reflecting from the top or bottom as necessary until the other player makes his 'hit'. This action is repeated until one player misses the ball. The circuitry then detects a 'score' and automatically increments the correct score counter and updates the score display. The ball will then serve automatically towards the side which had just missed. This sequence is repeated until a score of 15 is reached by one side, whereupon the game is stopped. The ball will still bounce around but no further 'hits' or 'scores' can be made. While the game is in progress, three audio tones are output by the circuit to indicate top and bottom reflections, bat hits and scores.

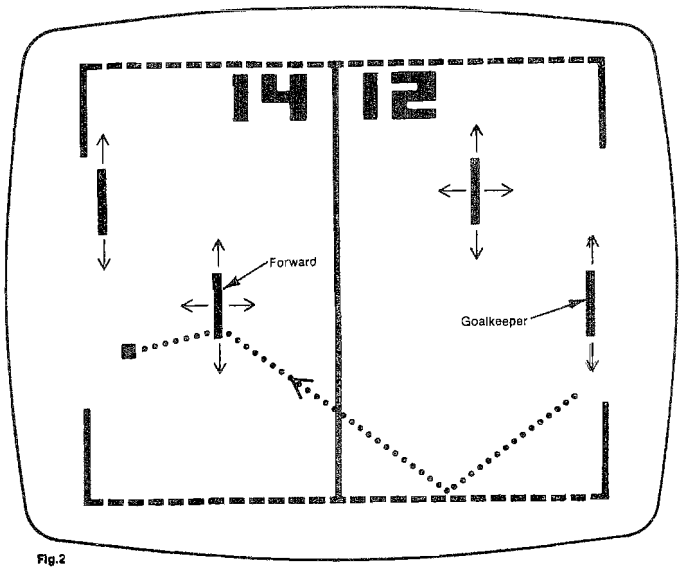


Fig.2

Soccer

The 'soccer' type game is shown in Figure 2. With this game each participant has a 'goalkeeper' and a 'forward'. The layout is such that the 'goalkeeper' is in his normal position and the 'forward' can be positioned in any part of the playing area.

When the game starts, the ball will appear travelling from one goal line towards the other side. If the opponent's forward can intercept the ball, (Figure 2a), he can 'shoot' it back towards the goal. If the ball is missed it will travel to the other half of the playing area and the first team's forward will have the opportunity of intercepting the ball and redirecting it forward at a new angle according to the 'player' section which is used, (Figure 2a). If the ball is 'saved' by the 'goalkeeper' or it reflects back from the end boundary, the same forward will have the opportunity to intercept the outcoming ball and divert it back towards the 'goal'.

A 'score' is made in the 'soccer' game by 'shooting' the ball through the defined goal area. The scoring and game control is done automatically as for the tennis game. The same audio signals are used to add atmosphere to the game.

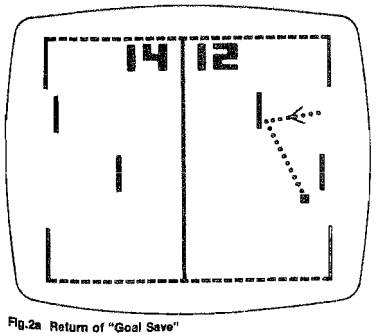


Fig.2a Return of "Goal Save"

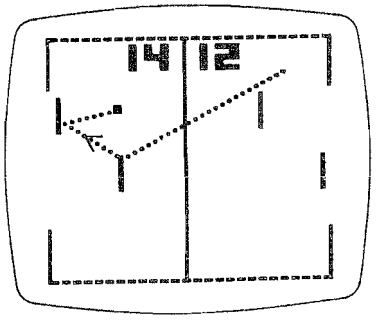


Fig.2b "Shooting" Forward

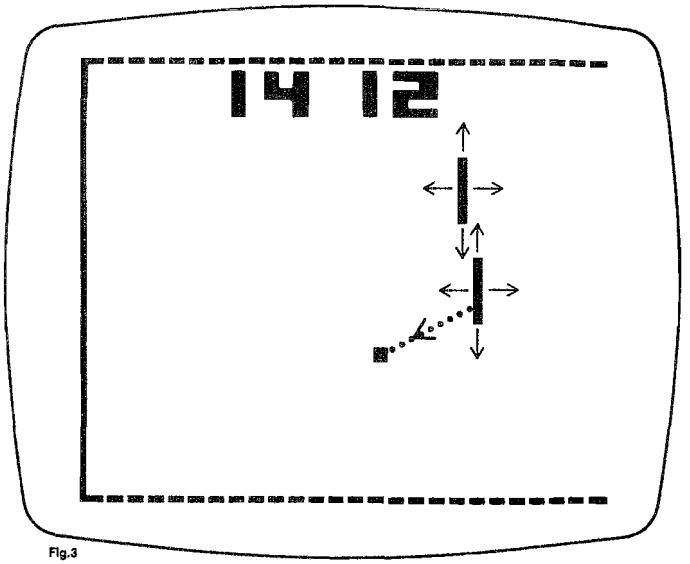


Fig.3

Squash

This game is illustrated in Fig 3. There are two players who alternately hit the ball into the court. The right hand player is the one that hits first; it is then the left hand player's turn. Each player is enabled alternately to ensure that the proper sequence of play is followed. The ball is colored to the color of the bat of the next player who's to hit the ball.

Practice

This game is similar to squash except that there is only one player. See Fig. 4. The left score counts misses; the right score counts hits The game ends when either 15 misses occur or when 15 consecutive hits are made without a miss. The right score is reset if it is not 15 and a miss occurs

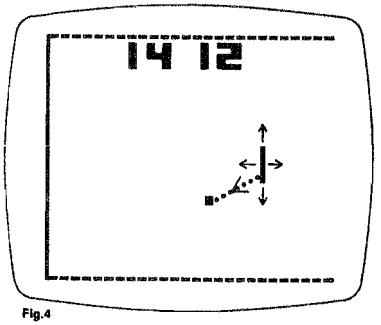


Fig.4

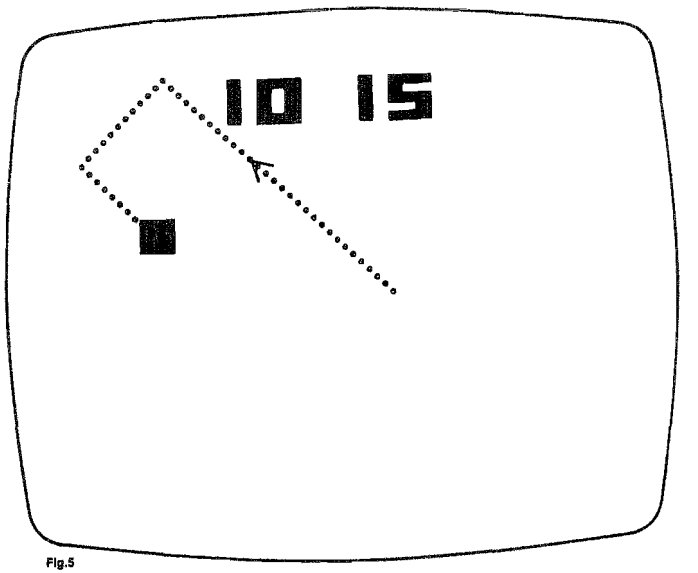


Fig.5

Rifle Game No. 1

This game is illustrated in Fig. 5. It has a large target which bounces randomly about the screen. A photocell in the rifle is aimed at the target. When the trigger is pulled, the shot counter is incremented and, if the rifle is on target, the hit counter is incremented, a hit noise is generated and the target is blanked for a short period. After 15 shots the score appears but the game can still continue without additional scoring

Rifle Game No. 2

In this game, illustrated in Fig. 6, the ball traverses the screen from left to right under control of the manual serve button. Otherwise the game is as described for Rifle Game No. 1.

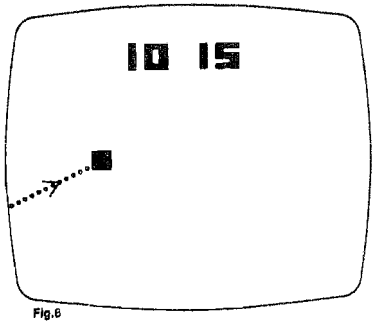
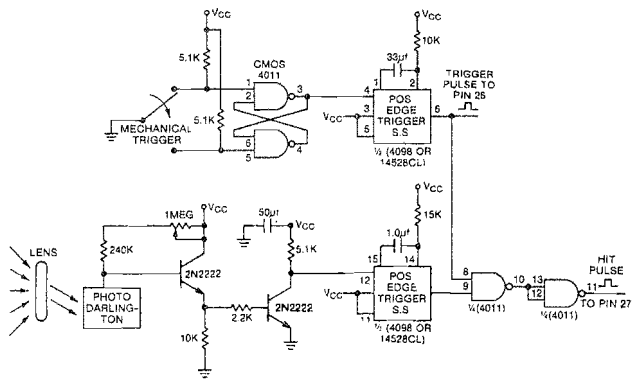
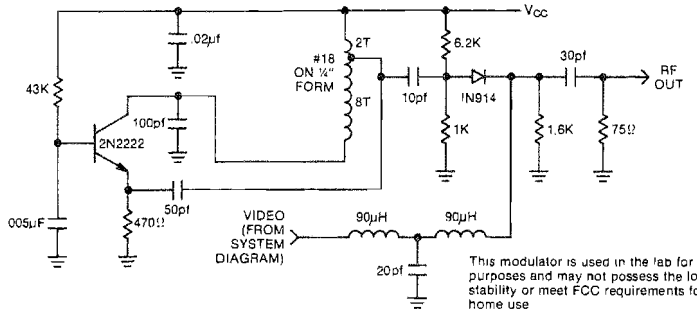


Fig.6



NOTE: Aim rifle at scope on TV and adjust 1 meg pot. for max voltage on pin 12 of the 4098 at a 8 ft. distance. The voltage at pin 12 should be 0 when there is no light on the TV screen

Fig.7 RIFLE INTERFACE

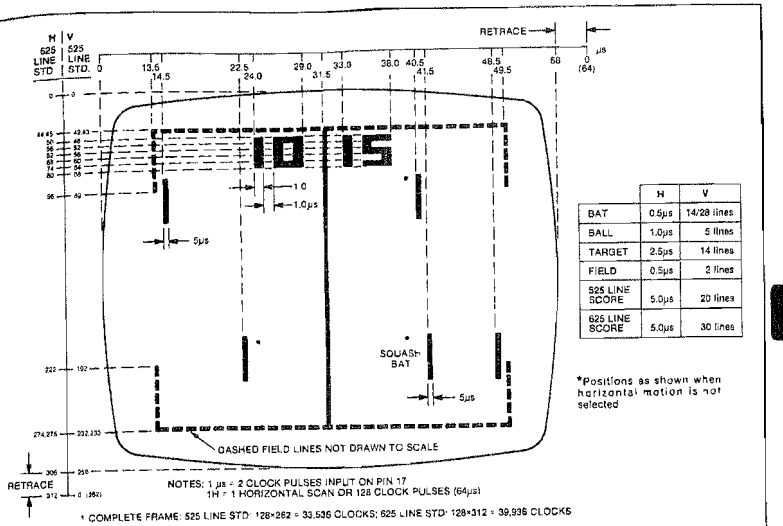


This modulator is used in the lab for test purposes and may not possess the long term stability or meet FCC requirements for home use

Fig.8 VHF MODULATOR

	Horizontal	Vertical
Slow	± 5µs	2 angles = 1 line 4 angles = 3 lines
Fast	± 1µs	2 angles = 2 lines 4 angles = 5 lines

Fig.9 ANGULAR MOTION



	H	V
BAT	0.5µs	14/28 lines
BALL	1.0µs	5 lines
TARGET	2.5µs	14 lines
FIELD	0.5µs	2 lines
525 LINE SCORE	5.0µs	20 lines
625 LINE SCORE	5.0µs	30 lines

*Positions as shown when horizontal motion is not selected

NOTES: 1 µs = 2 CLOCK PULSES INPUT ON PIN 17
1H = 1 HORIZONTAL SCAN OR 128 CLOCK PULSES (64µs)
1 COMPLETE FRAME: 525 LINE STD: 128×262 = 33,536 CLOCKS; 625 LINE STD: 128×312 = 39,936 CLOCKS

Fig.10 LOCATION OF DATA OUTPUT PULSES

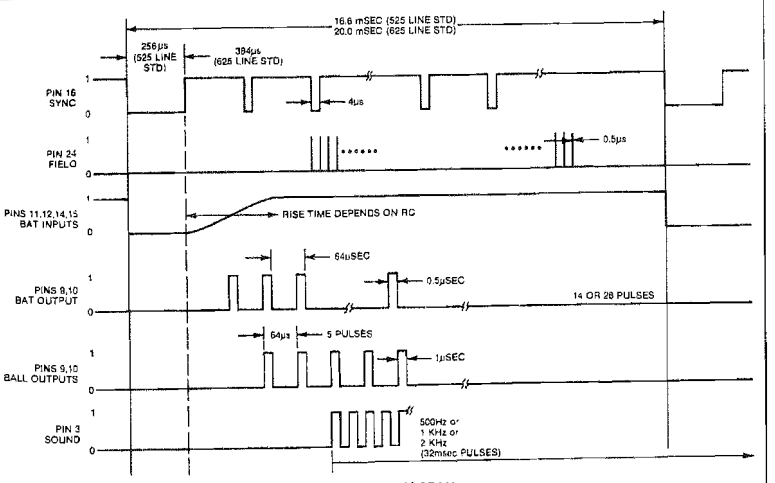


Fig.11 TIMING DIAGRAM

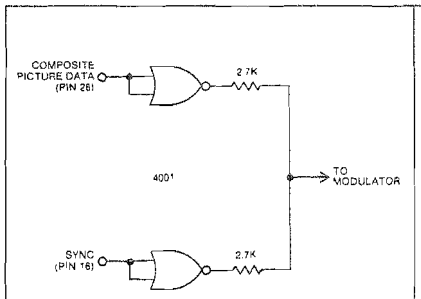


Fig. 12 BLACK AND WHITE IMPLEMENTATION USING COMPOSITE PICTURE DATA SIGNAL (White Bats)

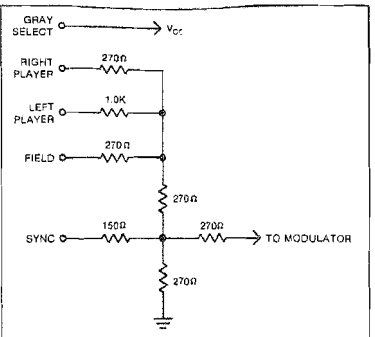


Fig. 13 BLACK AND WHITE IMPLEMENTATION USING INDIVIDUAL PLAYER SIGNALS (Black and White Bats/Gray Background)

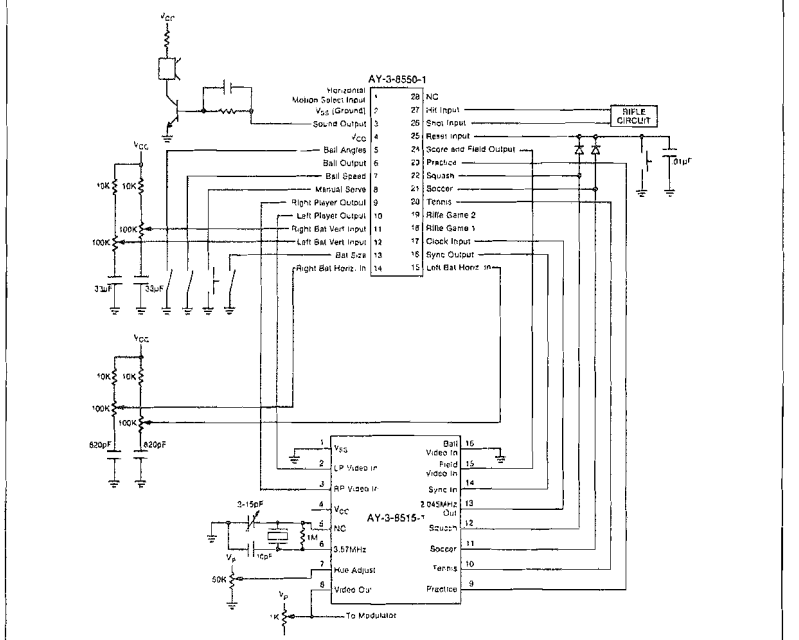


Fig. 14 AY-3-8550-1 FULL COLOR IMPLEMENTATION USING AY-3-8515-1 COLOR CONVERTER CIRCUIT (SEE PAGE 4B-23)

Color Converter I

DESCRIPTION

The AY-3-8515-1 is a single N-Channel MOS circuit which accepts the video outputs of the AY-3-8500-1 and AY-3-8550-1 game circuits and converts the black and white signals to a single color composite video output. The colors of the background and paddle outputs are selectively changed directly by the game select inputs. The circuit also provides, as an output, a 2.045MHz clock for the game chip.

OPERATION

The AY-3-8515-1 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from the AY-3-8500-1 or AY-3-8550-1 is reconstructed in the color circuit and provides both front and back porchs to insure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference, is supplied after sync. The color phase of the burst is internally selected by the game select inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components for ball and paddle games and only requires the addition of two diodes when target games are also selected.

The color burst is followed by an appropriate blanking interval so the TV set will not lock on to the background phase.

Video Inputs: Four video inputs are provided on the AY-3-8515-1 These are: field and score, left player, right player and ball. When operated with the AY-3-8550-1, the ball input should be grounded.

Video Output: After sync, color burst and blanking, the video consists of background, field and score, right player, left player and ball. The ball output is always white. In the absence of other signals, the background is output.

The color outputs are:

Grounded Select Input	Back-ground	Field	Right Player	Left Player
1 Tennis	Green	Yellow	Orange	Magenta
2 Soccer	Blue	Cyan	Cyan	Yellow
		Blue	Green	
3 Squash	Brown	Magenta	Blue	Cyan
				Green
4 Practice	Cyan	Green	Yellow	Brown
	Green			

Colors may be adjusted for system veriations by the chip hue control which varies the phase delay of the color outputs.

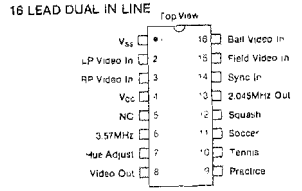
For games incorporating rifle, select input 3 may be connected by diodes to the squash select and practice select inputs of the game circuit, and select input 4 may be connected by diodes to the two rifle inputs

Luminesence Levels: The luminesence levels of the various signals in the composite video output have been selected to provide black and white compatiblity. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray

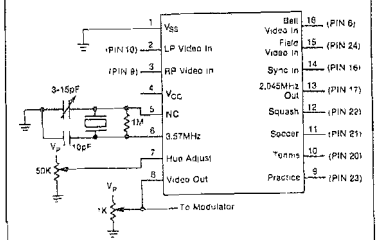
Figure 1 shows the typical composite video waveform from the circuit.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



CONNECTION DIAGRAM



NOTE AY-3-8500-1/8550-1 PINS shown in parentheses

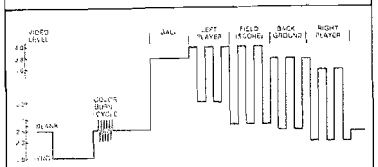


Fig. 1 COMPOSITE VIDEO OUTPUT

In order to assure the correct video levels, a 1K variable potentiometer should be used to adjust the output to a maximum pf 4 volts and a minimum of 2 volts.

CLOCK INPUT

The AY-3-8515-1 operated directly from a 3.579MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8515-1 generates a low impendance 2.045MHz clock to directly drive the game chip without external components

Ball & Paddle II

FEATURES

- Full **COLOR** Operation (see page 4B-32)
- Eight selectable games — tennis, hockey, soccer, squash, practice, gridball, basketball and basketball practice.
- 625 Line (AY-3-8600) and 525 Line (AY-3-8600-1) versions.
- T.V. raster generator
- Color or black and white operation
- Two axis player motion
- Automatic on-screen scoring, 0-15
- End of game indication (flashing score)
- Realistic ball service and scoring
- Score color keyed to player
- Independent player selectable bat size for handicapping
- Fast ball speed inhibit
- Five segment bats giving ± 40°, ± 20°, and horizontal
- Sound outputs for hit, rebound and score
- Shooting forwards in hockey and soccer

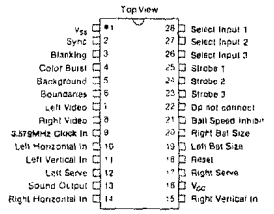
DESCRIPTION

The AY-3-8600 and AY-3-8600-1 circuits have been designed to provide a TV 'game' function which gives active entertainment using a standard color or black and white domestic television receiver.

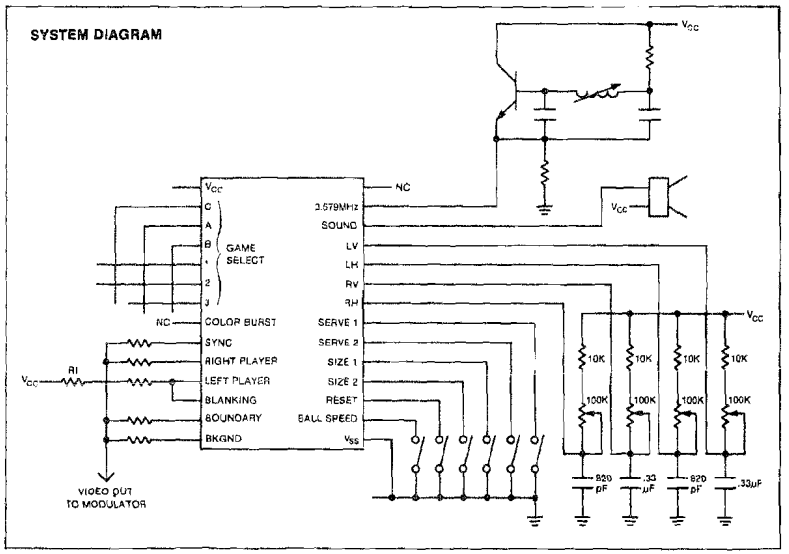
The circuit is intended to be battery powered and a minimum number of external components are required to complete the system. A system diagram is shown below

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



PIN FUNCTIONS

Power

V_{CC} positive supply input
V_{SS} negative (substrate) supply input

Control Inputs

Right player vertical control
Right player horizontal control
Left player vertical control
Left player horizontal control
Right player serve
Left player serve
Right player bat size
Left player bat size
High speed ball inhibit
Game reset

The game is reset with scores set to zero and ball returned to the service position by momentarily connecting the reset input to V_{SS}.

Bat size can be selected as either 15 or 30 lines in height individually for handicapping purposes. Connection of the bat size input to Vss selects small bat

Bat position is set by a variable resistor and capacitor connected as shown in the System Diagram. A 10K ohm resistor must be placed in series with the potentiometer.

Game Select Inputs/Outputs

Strobe 1
Strobe 2
Strobe 3
Select Input 1
Select Input 2
Select Input 3

Game selection is made by the interconnection of one of the output strobes, STR 1, STR 2, or STR 3 with one of the three input selection lines SEL 1, SEL 2, or SEL 3

The game selections are defined as

STR 1/SEL 1	Tennis
STR 1/SEL 2	Hockey
STR 1/SEL 3	Squash
STR 2/SEL 1	Practice
STR 2/SEL 2	Gridball
STR 2/SEL 3	Soccer
STR 3/SEL 1	Basketball
STR 3/SEL 2	Basketball Practice

Video Outputs

Right bat, score and ball
Left bat, score and ball
Boundaries
Background
Sync
Blanking
Color burst locator

All signals are present in the circuit to generate a composite video signal with sync, color burst, and blanking. This single video signal provides the input to the game RF modulator

Video outputs are provided for each of the two player bats and their scores, the boundaries, background, sync and blanking. As shown in the System Diagram, the ratio of the particular output resistor with R_L sets the luminance level

In addition to the above outputs, a color burst locator output is provided for use where external color generation is desired. The signal locates the position in the waveform behind the sync pulse

Clock Input — 3.579MHz

OPERATION

Ball Motion

In all games, the ball starts at slow speed. If the high speed mode has been selected the ball will switch to high speed after 7 consecutive hits by the players without a goal being scored.

The bats will be segmented into 5 zones, each zone defining a different rebound angle. The zones listed from top of bat to bottom are nominally 40° up, 20° up, horizontal, 20° down, 40° down. A ball passing through a forward from behind will have its angle influenced as above, but not its left/right direction

Scoring

All two player games will terminate when one player has 15 points at which time the score will flash and the bats have no further effect on the ball.

Sound

Tone of approximately 500Hz, 1Kz and 2KHz will be output for a nominal period of 32msecs for ball hits wall, ball hits bat and score. The output is capable of directing driving 100 ohm soeakers

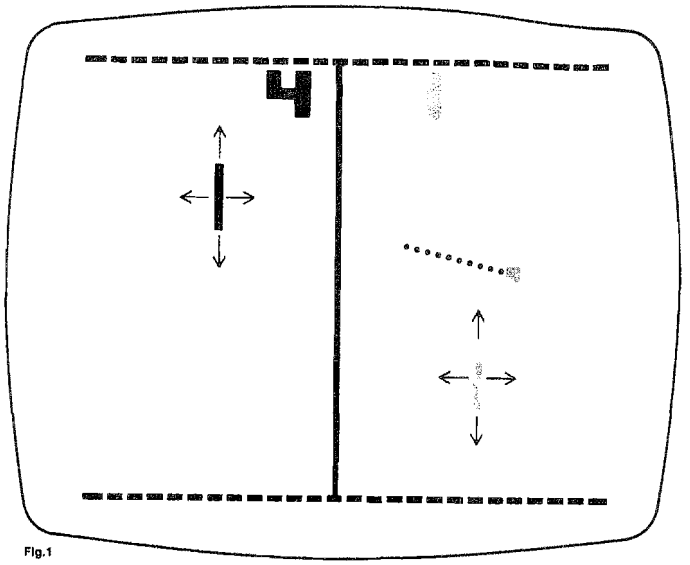


Fig.1

Tennis

This game uses a playing area as shown in Fig. 1. Each player can only move around his side of the court. The game will start when the player whose turn it is to serve, depresses his service button. The service will automatically change every five points scored. At service the ball will move away from the service point with a random angle but always toward the net.

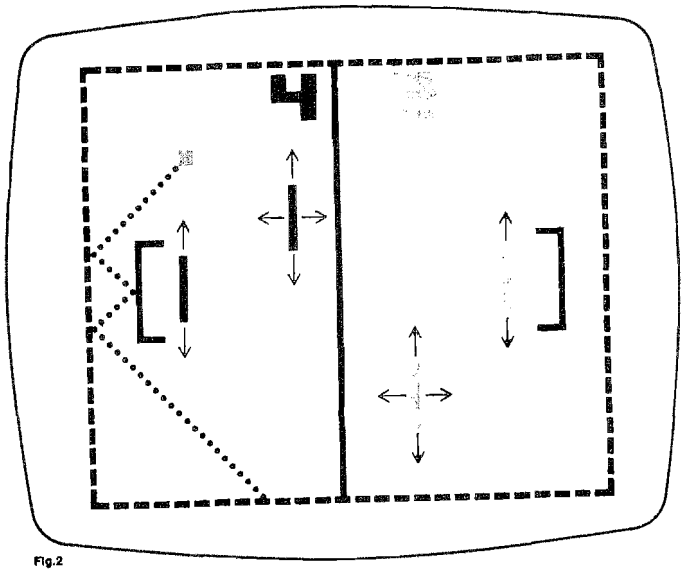


Fig.2

Hockey

This game uses a playing area as shown in Fig. 2. The forwards on both sides have freedom to move over the entire playing area. The goal keepers will be locked in the horizontal axis in front of their respective goals but will move in the vertical axis in the same manner as the forwards.

The game starts when both players have depressed their service buttons. The ball will move away from the face off point with a randomly selected angle in either direction.

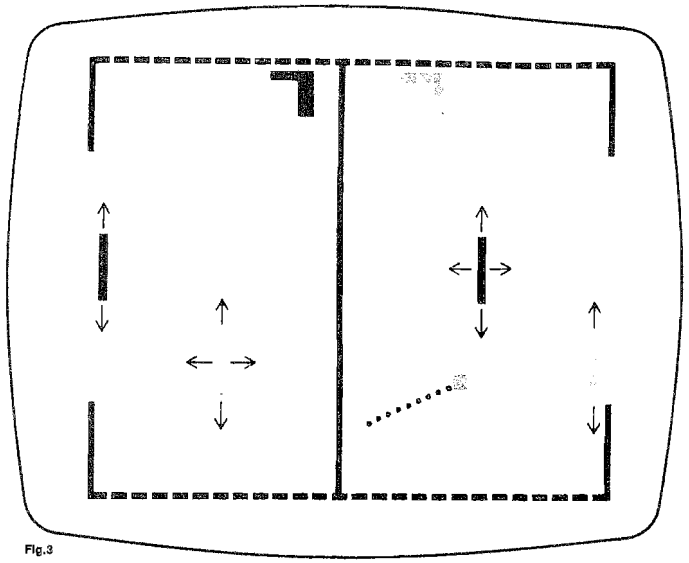


Fig.3

Soccer

This game uses a playing area as shown in Fig. 3. The motion of the players is as in the hockey game. The game will start when the loser of the previous goal depresses his service button. The ball will move away from the kickoff point with a randomly selected angle but always towards the goal of the winner of the previous goal

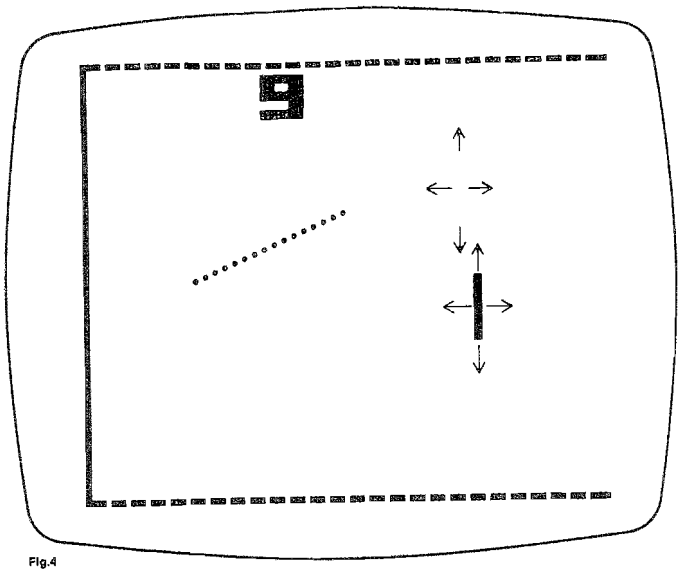


Fig.4

Squash

This game uses a playing area as shown in Fig. 4. Each player can move over the whole court. The game will start when the player whose service it is, depresses his service button. The ball moves off with a random angle toward the front wall. The color of the ball will change to the color code of the next player to hit the ball Should the wrong player intercept or be hit by the ball it will be considered a fault Points will only be given if won on player's own service Points won on opponents serve will only cause a service change

Practice

This game is a single player squash (See Fig. 5) The right score counts the number of successive hits in the current game (to a maximum of 15), the left score the number of volleys played.

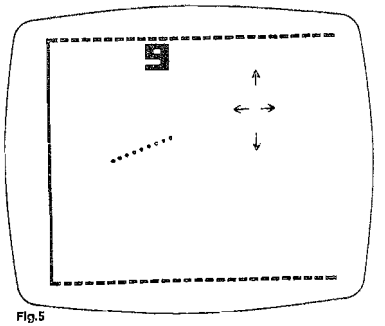


Fig.5

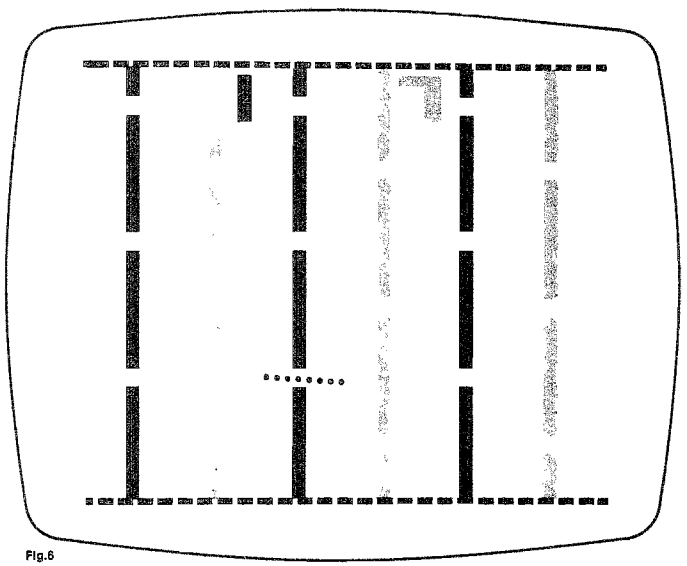


Fig.6

Gridball

This game uses a playing area as shown in Fig. 6. Each player has three sets of vertically moving barriers to block the ball from approaching his end and opening in the barriers to permit the ball to advance toward the opponent's end. The game starts when both players have depressed their service buttons. The ball moves away from the face off point with a random angle in either direction.

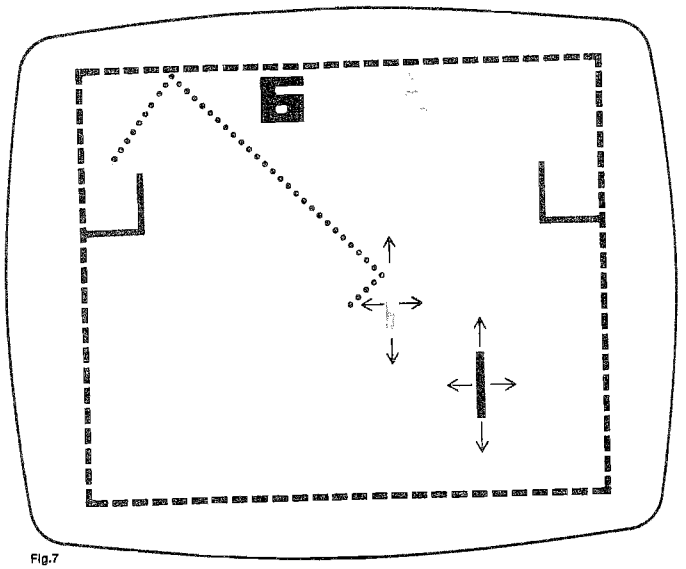


Fig.7

Basketball

The basketball games use the closed playing area as shown in Fig. 7. The players must deflect the ball and cause it to enter the top of the goal to score. The game starts when both players depress the service buttons. The ball moves from the serve point with a random angle in either direction

Basketball Practice

Basketball practice is a one player game which utilizes only the left basket as shown in Fig. 8. The right counter displays the number of hits the player makes without scoring while the left counter shows the number of baskets made. Play starts when the right serve button is depressed.

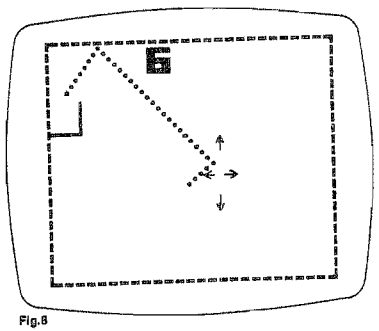


Fig.8

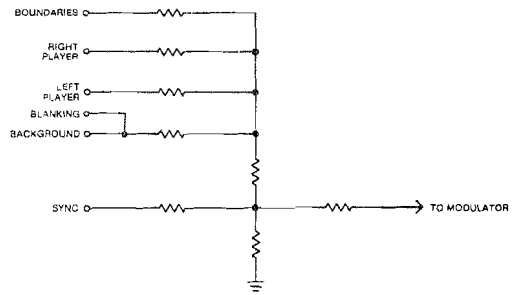


Fig. 9. BLACK AND WHITE IMPLEMENTATION USING INDIVIDUAL PLAYER SIGNALS

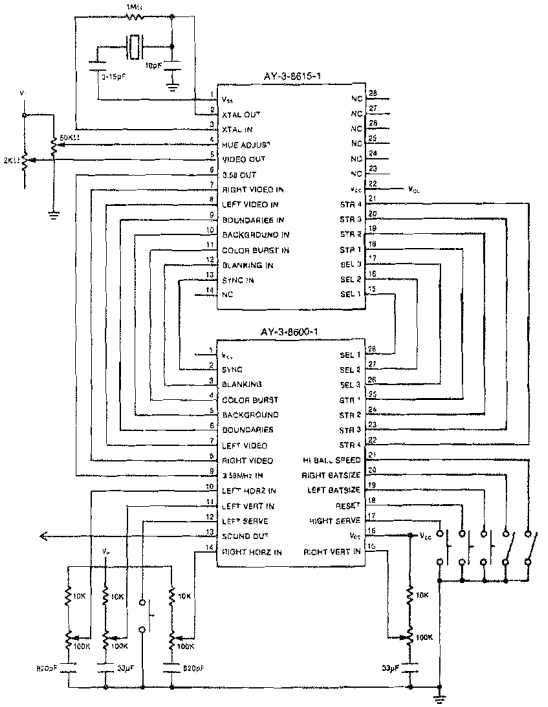


Fig. 10 AY-3-8600-1 FULL COLOR IMPLEMENTATION USING AY-3-8615-1 COLOR CONVERTER CIRCUIT (SEE PAGE 4B-33)

Color Converter II

DESCRIPTION

The AY-3-8615-1 is a single N-Channel MOS circuit which accepts the video outputs of the AY-3-8600-1 game circuit and converts the black and white signals to a single color composite video output. The colors of the background and paddle outputs are selectively changed directly by the game select matrix. The circuit also provides, as an output, a buffered 3.579MHz clock for the game chip.

OPERATION

The AY-3-8615-1 provides a color composite video signal with color burst envelope and sync for input to the RF modulator of a TV game.

Sync: The sync input from the AY-3-8600-1 is reconstructed in the color circuit and provides both front and back porches to insure correct operation in color TV circuits.

Color Burst: A color burst signal, containing ten cycles of the 3.579MHz color reference is supplied after sync. The color phase of the burst is internally shifted by the game matrix inputs with respect to the phases of the background, right player and left player so that different colors may be rendered for each game. This color change may be affected with no external components.

The color burst is followed by an appropriate blanking interval so the TV set will not lock on to the background phase.

Video Inputs: Six video inputs are provided on the AY-3-8615-1. These are: field, background, color burst locator, left player, right player and blanking.

Video Output: After sync, color burst and blanking, the video consists of background, field, scores, right player, left player and ball.

Colors may be adjusted for system variations by the chip hue control which varies the phase delay of the color outputs.

Luminesence Levels: The luminesence levels of the various signals in the composite video output have been selected to provide black and white compatibility. The field and left player signals are set to near white levels, the right to near black, and the background is set at a mid level to show gray.

Figure 1 shows the typical composite video waveform from the circuit.

In order to assure the correct video levels, a 1K variable potentiometer should be used to adjust the output to a maximum of 4 Volts and a minimum of 2 Volts.

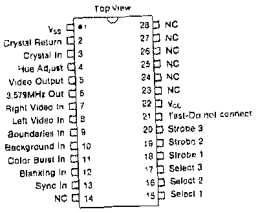
CLOCK INPUT

The AY-3-8615-1 operated directly from a 3.579MHz crystal input. A variable capacitor with a range of 3 to 15 pF should be used to tune the crystal.

CLOCK OUTPUT

The AY-3-8615-1 generates a low impedance 3.579MHz clock to directly drive the game chip without external components.

PIN CONFIGURATION
28 LEAD DUAL IN LINE



Grounded Select Input	Background	Field	Right Player	Left Player
1 Tennis, Soccer	Green	Yellow	Orange	Magenta
2. Gridball, Hockey	Blue	Cyan Blue	Cyan Green	Yellow
3. Squash, Basketball2	Brown	Magenta	Blue	Cyan Green
4 Practice, Basketball1	Cyan Green	Green	Yellow	Brown

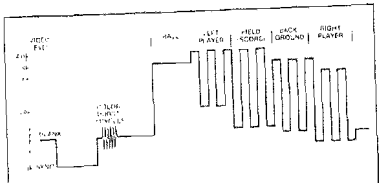


Fig. 1 COMPOSITE VIDEO OUTPUT

Battle I

FEATURES

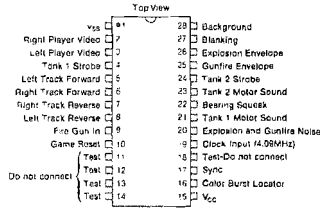
- Two independently controllable tanks
- Tank explosion and sounds when hit by shell or mine
- Exploding mines
- Shell firing and burst video and sound
- Three forward and reverse tank speeds
- 32 rotational angles
- Fixed terrain barriers
- Realistic tank sounds
- Automatic on-screen scoring
- Scores color keyed to player
- 625 Line (AY-3-8700) and 525 Line (AY-3-8700-1) Versions

DESCRIPTION

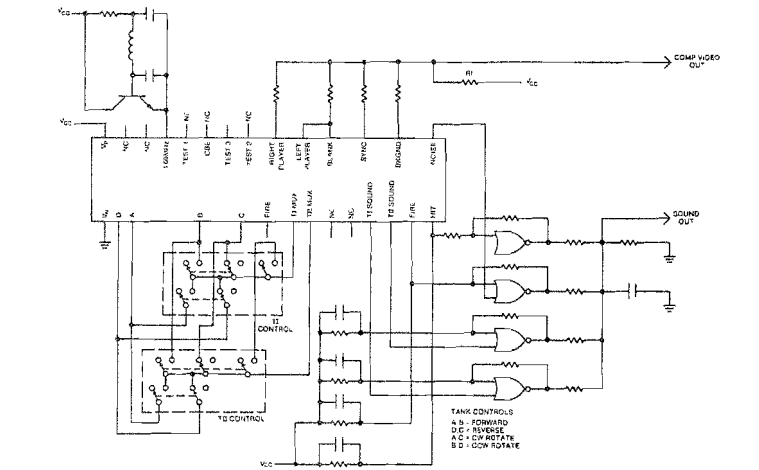
The AY-3-8700/8700-1 circuit is a "tank battle game" and has been designed for two players where each player has a completely steerable tank with forward and reverse speed control and a firing button. Anti-tank barricades and mines are in the battlefield to retard each tank's progress while under battle conditions. The object of the game is to score as many hits on the enemy tank as possible. The first player to reach 31 hits ends game. The circuit is designed to be used with standard domestic television receivers. The AY-3-8700/8700-1 is manufactured in a 28 pin dual-in-line package and can be used in battery systems with a minimum number of components to provide a complete game.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



SYSTEM DIAGRAM



PIN FUNCTIONS

Sound Outputs

Tank 1 motor
Tank 2 motor
Bearing and track squeak
Explosion envelope
Gun fire envelope
Explosion and gun fire noise

Power Input

V_{CC} positive voltage
V_{SS} substrate (negative) voltage

Control Inputs and Outputs

Left track forward
Left track reverse
Right track forward
Right track reverse
Fire gun
Control strobe 1
Control strobe 2
Game reset

Video outputs

Right player tank, shell, shell burst, score and mines
Left player tank, shell, shell burst, score and fixed barriers
Blanking
Background
Sync
Color burst locator

Clock Input

4.09MHz clock input

VIDEO SIGNAL OUTPUT

All signals are present in the circuit to generate a composite video signal with a waveform which includes composite blanking and color burst envelope. This simple video signal provides the input to the game RF modulator.

The luminance levels are set by the ratios of the resistors shown in the System Diagram. This output configuration provides maximum flexibility to the user who can set, at his option, either a positive or negative sync.

Five outputs are provided: sync, right player, left player, background and blanking. The right player output includes the tank control, right player score, shells fired by the right tank, shell bursts from right tank shells and mines. The left player output includes the left tank, left player score, shells fired by the left tank, left tank shell bursts and fixed barriers.

It is recommended that one tank be displayed in white, one in black, and the background in grey.

The blanking and black outputs are shown connected to a single resistor since the modulation level is approximately the same for both.

In addition to the preceding five outputs, a color burst locator is provided to enable users who wish to provide a color background to locate the color burst envelope at the correct waveform position after the sync output

CLOCK 4.09MHz

4B

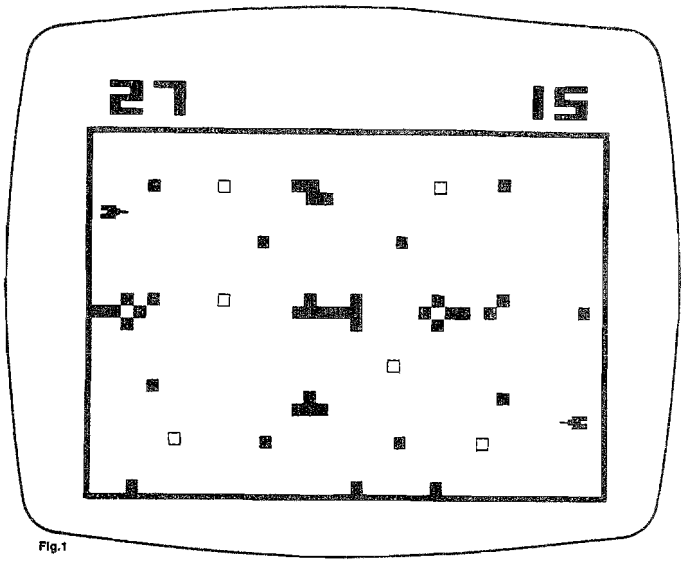


Fig.1

Battle I

DISPLAY SYMBOLS AND CONTROL

TANKS

Control — The tanks are controlled by connecting the appropriate strobe outputs to the track inputs. Forward motion is achieved when both the right and left track forward inputs are connected to the strobe. On connection, the tank will advance in low speed. If the connection is held, the medium speed will select after one half second. After another one second of connection, high speed is selected. Breaking the connection when any speed is achieved will cause the tank to remain at the selected speed. The controls should each be single pole double throw center off momentary switch.

The tank can be made to go through the three reverse speeds at one second intervals by connection of the left and right reverse track inputs to the appropriate strobe output. Tank rotation in a clockwise (right turn) direction is caused by connection of the left forward and right reverse track inputs to the strobe while counterclockwise (left turn) direction is caused by connection of the left reverse and right forward track inputs to the strobe. The tanks are able to turn while either in forward or reverse speed and rotate when stationary

Tank Details

Definition and resolution	64 bits (8×8) or 8/100 of TV screen width
Orientations	32
Direction of travel and firing angles	32
Forward speeds	3
Reverse speeds	3

SHELLS

Firing — connection of the gun fire input to a strobe output with a SPST normally open pushbutton switch causes the firing of a tank gun and release of a projectile. The firing rate is approximately once every four seconds and the refire requires release of the button and redepression. Depression made during the four second interfiring time are ignored by the circuit.

When a shell is in flight, the rotation of the tank will cause the shell to follow a curved trajectory in the direction of tank rotation.

Range — the range of a shell is aproximately 2/3 of the screen length or width dependent on firing angle.

Size — the shell is a 2×2 bit dot

BATTLEFIELD BARRIERS

Fixed Terrain Barriers — a minimum of twelve pseudorandom fixed terrain barriers are on the battlefield to both impede the progress of the tanks and provide protection from shells. When coming in contact with a barrier, the tank stops and cannot be restarted for two seconds. The operator must then reverse his direction or turn the tank to clear the barrier before proceeding.

Mines — six mines are distributed on the battlefield. Hitting a mine with a tank causes the tank to explode and become stationary with its gun inactive for a period of 2 to 4 seconds. The mine then venishes for the duration of battle. A mine being hit scores a hit for the enemy tank.

Barrier Sizes — barriers and mines are 4×4 bit square minimum size.

EXPLOSIONS (VIDEO)

Shell Bursts — shell burst patterns are produced when a shell is at end of range or when the shell makes contact with a barrier.

Tank Explosions — a tank will explode and fragment when a tank hits a mine or is struck by a shell.

SCORING

Separate scores, color coded to the tank, are indicated for each player. A player's score is incremented when his tank scores a hit on his opponent's tank or the opponent's tank hits a mine. The game ends when either player scores 31 points.

RESET

The game is reset by momenterily connecting Reset input to V_N through an SPST pushbutton. On reset, the scores are cleared to zero, mines replaced and the tanks reset to the upper left and lower right corners in the stationary condition.

SOUND OUTPUT

GENERAL

The sound outputs produced by the circuit are low frequency typical of those associated with heavy equipment motors and of explosions. it is recommended that the sound be reproduced through the TV set or in a large speaker so the full richness of the sound can add the proper atmosphere to the game.

ENGINE SOUND

Outputs are provided for the engine sound associated with each tank. Four motor frequencies are provided; three for the three speed ranges and one for stationary condition. A typical sound circuit for filtering each output is shown in the System Diagram.

GUN FIRE SOUND

Gun fire sounds are produced mixing the noise output with the fire output. The fire output should be filtered and mixed with the noise output as shown in the System Diagram.

SHELL BURST AND TANK EXPLOSION SOUNDS

Shell burst sounds are produced when a shell reaches the end of its range or hits a barrier. Tank explosion sounds are produced when a tank hits a mine or is struck by a shell. These sounds are generated by filtering the hit output which is an open drain FET to V_N and using the filtered output to gate the noise output. A typical circuit is shown in the System Diagram.

GIMINI Programmable Game Set

FEATURES

- User game design capability
- Up to eight player operation
- Up to eight moving screen objects controlled by user
- 64 selectable moving objects
- Up to 240 selectable background objects
- 64 text symbols
- Movable background field
- Six colors plus black and white

DESCRIPTION

The GIMINI Cassette Programmable Game Set is a multichip set which can accept different program chips, programmed by the user to provide an unlimited number of games including aggression games, ball and paddle games, gambling games, racing games, etc. The set consists of a CP1610 microprocessor, 20K ROM game program chips, a standard television interface chip and a 16K ROM graphics storage chip. In addition the user will have to provide five 256×4 bit RAM circuits.

The games can accept up to eight player inputs, and the set is designed for operation in color or black and white with standard domestic television receivers.

SYSTEM COMPONENTS

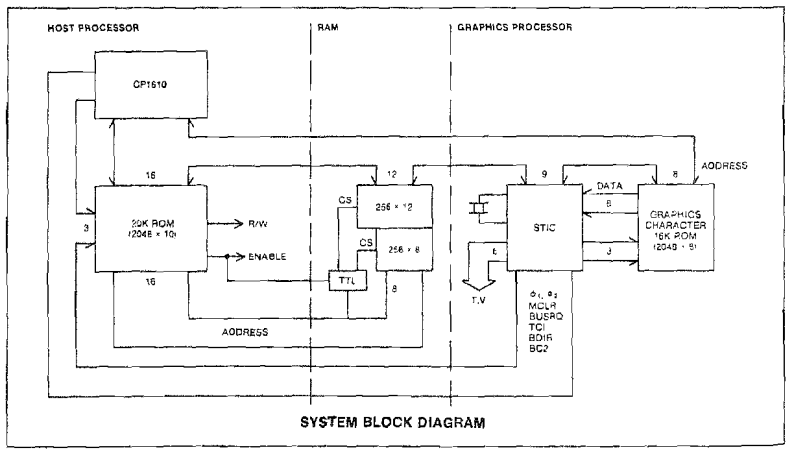
CP1610 Microprocessor: The CP1610 is a variant of the General Instrument CP1600 microprocessor and is designed for game operation. The chip is a 16 bit utilizing eight general purpose registers for fast and efficient processing of all game data. The processor operates only when picture data is not being presented and controls the addresses in both the program 20K ROM and the scratchpad memory according to the game rules.

20K ROM (RO-3-20480): The program ROM is organized as 2048 × 10 bit and contains all game rules. Because the set is organized on a data bus principle, additional ROM for more complex games may be added, or ROM may be interchanged to provide a user selectable game format. The unit also stores all symbol locations, color and velocity and direction data.

RAM: Up to five (5) 256 × 4 bit RAMS are required in the system. These are standard units with a 320 nanosecond access time.

STIC (AY-3-8900/8900-1): The STIC (Standard Television Interface Chip) provides the video signals including sync and blanking in a non-interlaced pattern for the TV deriving its output from graphics data specified by the microprocessor and obtained from the graphics ROM. The unit is functional only during picture time and obtains new graphics data between picture lines. The video output will consist of the six colors, black, white, sync, blanking and color burst. In addition, the STIC will provide an audio output signal for most game sounds.

Graphics ROM (RO-3-9316A): The 16K graphics ROM will contain a series 8 × 8 dot matrices for a large variety of game symbols; composite background sections to complete field outlines and 64 alpha-numeric characters. Special graphic symbols may be specified by the user for inclusion in custom processors.



SYSTEM BLOCK DIAGRAM

SYSTEM DESCRIPTION

The Gimini Programmable Game Set consists of three major sub systems (refer to the System Block Diagram)

1. **The host processor consisting of:**
   (a) C.P.U. (CP1610)
   (b) System instruction ROM (RO-3-20480)
2. **Random access memory consisting of:**
   (a) 256 — 12 bit words
   (b) 256 — 8 bit words
3. **The graphics processor consisting of:**
   (a) STIC, Standard Television Interface Chip (AY-3-8900/8900-1)
   (b) Graphics ROM (RO-3-9316A)

The host processor, via the system instruction ROM, executes a fixed program using a specific area of RAM for variables and a second area for graphics instructions. The graphics instruction area is common to the graphics processor.

The graphics processor, using the common RAM area, fetches data from RAM, decodes it and fetches from the graphics ROM the picture to be displayed and displays it on the screen at the required position.

During the drawn picture time any interactions of shapes are recorded. Then, at the end of the picture time, they are made available to the host processor for decoding of the picture status.

For the system to operate, each 1/60 sec is divided up into five time slots which relate closely to the timing and synchronizing of the TV.

Time Slot 1: A time slightly greater than the TV frame blanking, approximately 4.5 ms is dedicated to host processor. (This time can be increased by the host processor on a frame stealing basis)

Time Slot 2: Active-picture-time consisting of 45 µs of each 63.5 µs line for 192 lines.

Time Slot 3: A time slightly greater than the line-blanking-time, 17.8 µs, which is used by the graphics processor for processing the moving object data.

Time Slot 4: Consisting of the last two lines before the active picture when the graphics processor fetches the instructions from RAM of all the next-moving-object data into its internal scratch pad area.

Time Slot 5: The first two lines after the active picture when the interaction data and the picture status is available for the host processor.

TYPICAL OPERATION

1. System on.
2. Current game library displayed. (Automatic switch or routine ROM programmed).
3. User presses select input. (Host processor seeking external branch.)
4. If game has subset selection, i.e., 1, 2, 3 or 4 player modes, new library displayed.
5. The host processor computes the start-game-picture instructions and writes to common RAM; it also computes the start condition of variables involved in the strategy of the game or motion constants. This setup could, in some games, take several picture frames. Therefore, the TV picture is presented as a single color wash. (This may be substituted with a kalidoscope effect if the time for set up is more than one second.)
6. When the host processor gives control to the graphics processor, the first TV picture will be drawn using the following sequence of events. The first two lines before the active picture, up to 40 — 8 bit words will be fetched. This includes the following data:
   (a) the individual x and y coordinates of the top left hand corner of 8 moving objects, their location in graphics library, their color, visibility, and orientation (facing, left, right, up and down),
   (b) border color;
   (c) background color,
   (d) background offset in x, y from the top left hand corner of the active picture.
7. At the end of the last two lines before the active picture, the first 8 horizontal points of each of the eight moving objects will be fetched from the graphics ROM and loaded into the scratch pad in the graphics processor.
8. The graphics processor will then begin the active picture subroutine, "draw card" — move. At this time, beginning at address '000' in the 12 bit RAM area, each RAM address is fetched in sequence (20 per line). (Each address contains a secondary address for the graphics ROM plus an instruction on how to use the data contained in that address). Each 20 consective RAM location are re-addressed on 16 lines in each picture frame. This results in the picture requiring only 240 words to describe the entire screen (in RAM) while using the graphics ROM to detail the point by point detail in any one of the 240 "background card locations".
9. At the end of each active picture line the next (if required) picture dots of the moving objects are fetched from ROM and loaded to the graphics processor scratch pad.
10. Cards and moving objects are output simultaneously by the graphics processor. If, however, there is a conflict, moving objects have priority-write. This feature is the basis of interaction recording, i.e., object coincidence indicates an interaction to be decoded by the host processor.
11. By the end of the picture, all interaction possibilities would have been recorded. The graphics instructin detector can record all of the 67,108,869 possible moving object interactions. Additionally, there are 16,384 ways the moving objects can interact with the background objects. These are also recorded.

    The interaction structure is such that either shape, color, vertical position, horizontal position, or right angle position interaction can be detected and acted upon.
12. The host processor regains control at the end of the active picture and re-computes the outcome of the last action and what new action is required due to the picture interactions and change in the user controls.

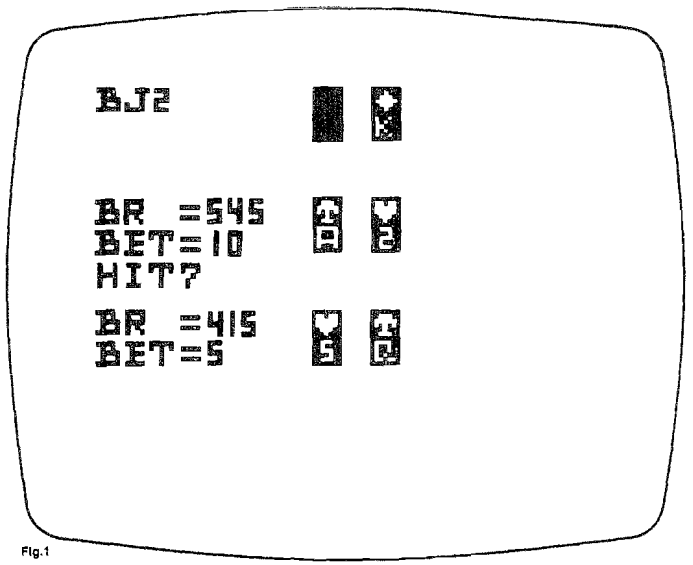


Fig.1

Black Jack (2 PLAYERS)

The Black Jack game is a one or two player game where the players are attempting to "beat the house" by drawing a higher card hand than the bank without exceeding a count of 21. The game determines the winning hands and increments or decrements the bankrolls of the players as a result of the outcome of the hand.

The game approximetes Las Vegas rules in that (a) the "house" will always draw a card if it has 16 or fewer points and will stand on 17 or more, (b) draws are standoffs and bets are not won or lost, (c) cards are dealt from a four deck "shoe" and (d) Black Jack pays 3 to 2.

Completion of bet entry by the players initiate the deal which consists of two cards being dealt face up to the players and one face up and one face down to the "house". The symbol H, asking if the player desires a hit, or the symbol D for double are shown on the screen in the position previously occupied by the S Symbol. D only appears if the player has a 10 or 11 showing. If the first player wishes to double, he depresses his yes button when D symbol appears. A single card is then dealt and the next player or bank completes his draw sequence. Depression of the no button causes the H symbol with a question mark to be displayed. One card will be dealt on each depression of the yes button until either: (1) Five cards have been drawn, (2) The player depresses the no button, or (3) More than 21 points have been drawn. At that time play is turned over to the second player, if any, who repeats the player one sequence.

When the players have drawn their final cards, the "house" competes its draw. Should the house have 16 or fewer points, it will always draw an additional card. A count of 17 or more by the "house" will complete the draw and cause an evaluation of the hands.

Those players with a card count greater than that of the house but not over 21, will have their bankrolls incremented by the amount of their bet or two times their bet should they have doubled. The bankroll count flashes indicating a winning hand. Players who exceed 21 or have less than the house have their bankrolls decremented by the amount of their bet or two times the bet in the event of a double. Players matching the house have no action taken on their bankrolls.

The game ends on depression of the game reset button.

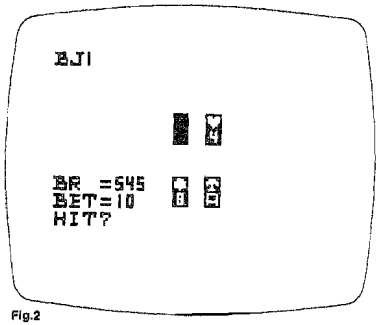


Fig.2

Black Jack (1 PLAYER)

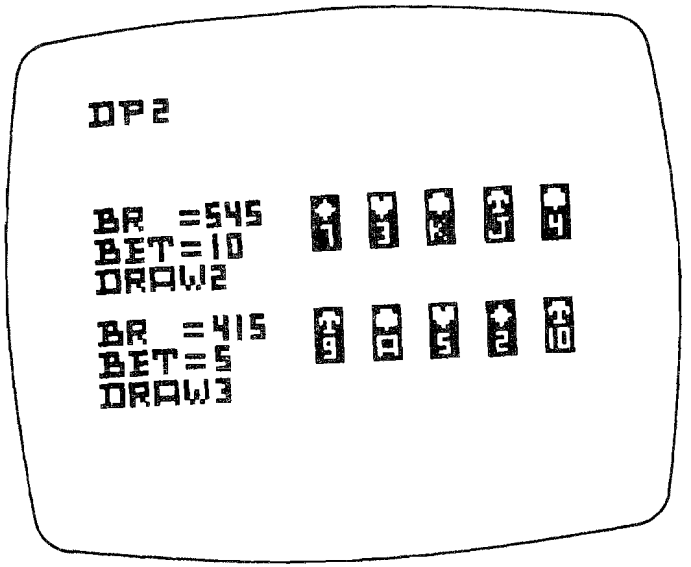


Fig.3

Draw Poker (2 PLAYERS)

The draw poker game is for one or two players who play against the house or against each other.

In two player operation, the players are dealt five cards face up after an automatic ante of $5 and a shuffle. The players may then evaluate their hands and raise the pot, if they desire. The raise is accomplished by the opening player, that is the one with the question mark next to his bet symbol, depressing his yes button. A raise of $5 is achieved each depression of the yes button. When the desired raise has been reached, the raiser depresses his no button and a question mark appears at the second player's bet line. If the second player desires to call or raise, he depresses his yes button once which causes his bet to equal the first player's bet. A $5 raise is made for each successive depression of the yes button. Depression of the no button after matching the original raiser is a call. If the second player does not match a raise and depresses his no button he concedes the hand and the raiser wins no further action.

The raise and betting continue until one of the players call. At that time, an indicator moves between the opposing player's cards, dwelling in each position for two seconds. The players wishing to discard one or more cards, secretly depress their yes buttons when the marker is in position. When the marker has moved past all the cards, the cards are discarded and new cards are dealt to replace the discards. The hands are then evaluated by the game, and the winning hand is awarded the loser's bet. The winner's bankroll count will then flash.

When a single player is playing the game, he is dealt five cards after the shuffle as in the two player game. The object of the game is to achieve the best poker hand, and odds are paid on the $5 bet in relation to the value of the hand as noted below. Discard is as previously described and the hand is evaluated after the new cards have been dealt.

Hand Value	Payout	Hand Value	Payout
Royal Flush	$500	Straight	$20
Straight Flush	$250	Three of a Kind	$15
Four of a Kind	$125	Two Pair	$10
Full House	$40	One Pair (Jacks or better)	Even
Flush	$25	All other hands	Lose

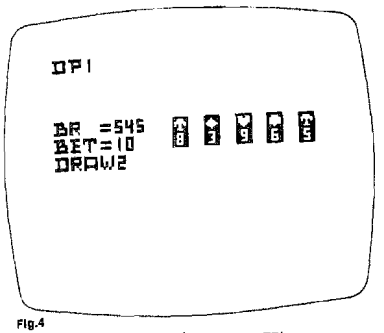


Fig.4

Draw Poker (1 PLAYER)

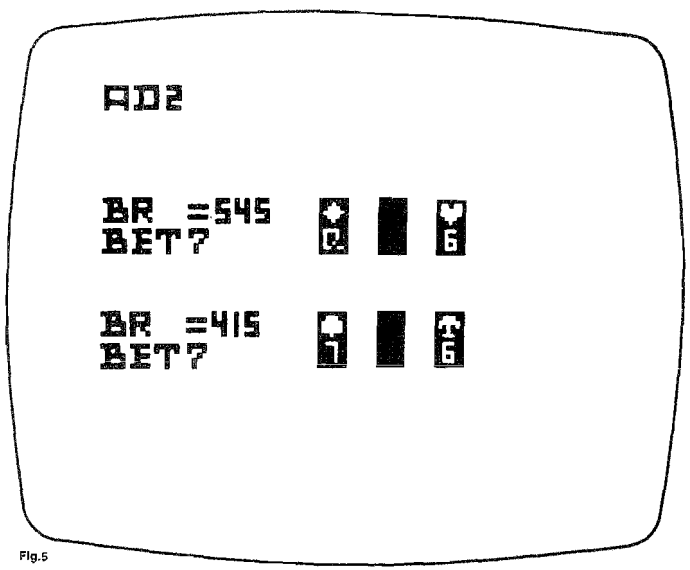


Fig.5

Acey/Deucy
(2 PLAYERS)

The Acey/Deucy game is for one or two players where the players use a combination of skill and luck to maximize their bankrolls. Shuffle and bankroll entry are accomplished in the same manner as for Black Jack.

The game is played with two cards dealt from a single deck face up to each player. The object of the game is to draw a card which is between but not equal to either of the two cards dealt.

Acey/Deucy
(1 PLAYER)

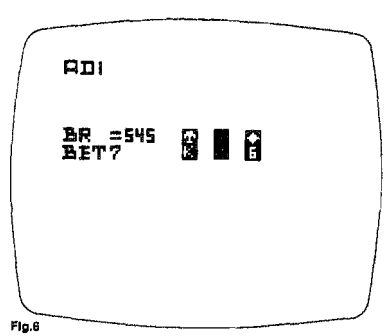


Fig.6

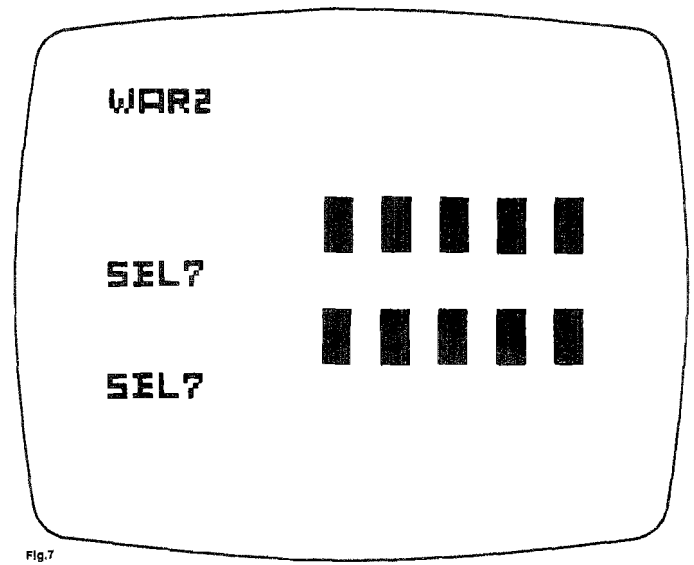


Fig.7

War
(2 PLAYERS)

The war game is a variation of the children's card game and is played with four decks. Each player is dealt five cards face down. After the deal, an indicator moves sequentially between the two rows of cards and the players choose the card to be turned over by depression of the yes button as the appropriate card is marked. When both players have selected their cards, the cards are shown face up. The player having the higher card wins two wins two points and the exposed cards are removed from the screen and replaced with two new face-down cards. In the event that both cards match, War, the players select two new cards in an attempt to win the trick. The winner in a War situation is awarded 12 points and the exposed cards play 8 additional cards are removed from the remaining deck. The game ends when all 208 cards are used. The winning score will then flash.

When only one person is playing against the game, card selection by the player causes both the player's card and the game's card in that position to be exposed.

War
(1 PLAYER)

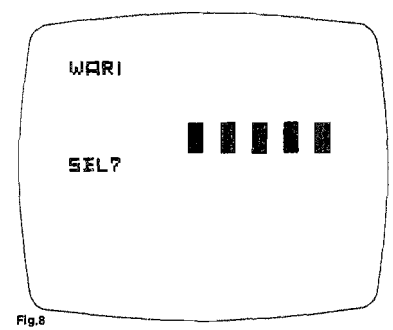


Fig.8

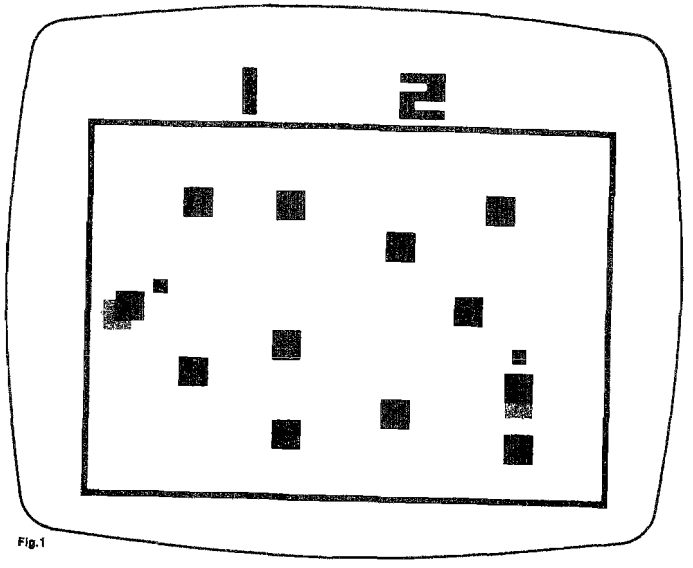


Fig.1

Combat Squares

The object of Combat Squares is to maneuver the square into such a position that a missile can be launched against the opponent's square. Each hit scores one point and 31 points ends the game. To further complicate the game, barriers are placed randomly over the playing area to provide protection from opponent's missiles and impede the maneuverability of the players. The missiles can be directed to follow curved paths, as they are directed by the turn controls.

Figures 1 shows a typical playing area

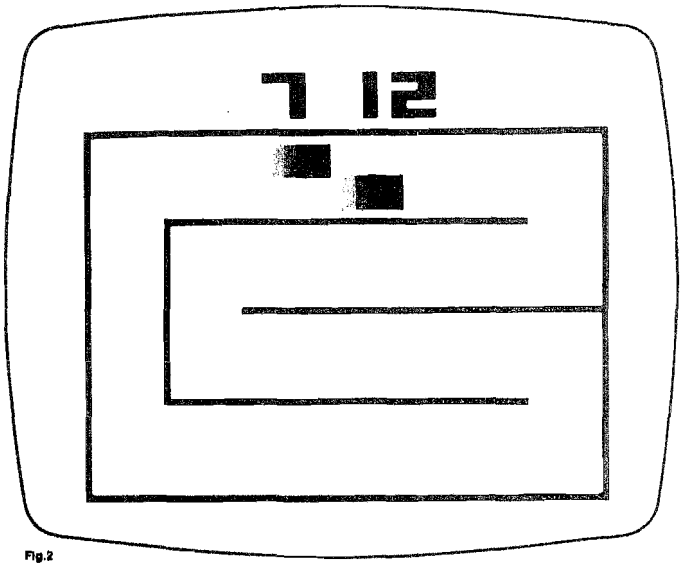


Fig.2

Racing Squares

This game requires both players to maneuver their squares around the course as shown in Figure 2. Each complete circuit of the course scores five points. However, if the player is not skillful in the driving of his square, his opponent scores one point each time the player hits the wall.

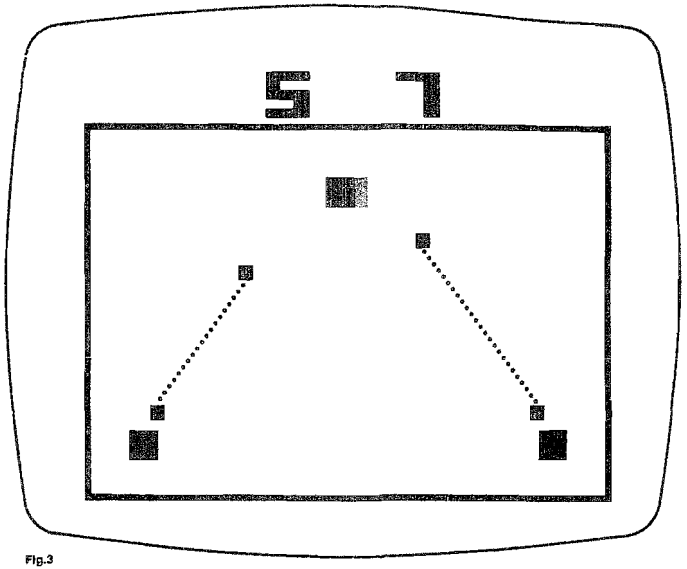


Fig.3

Shooting Squares

The Shooting Squares game is a target game where the players have their squares fixed as shown in Figure 3 and fire their missiles at the targets moving overhead. The targets move at various speeds and directions requiring constant adjustment of time and direction of fire. Thirty one hits by either player ends the game.

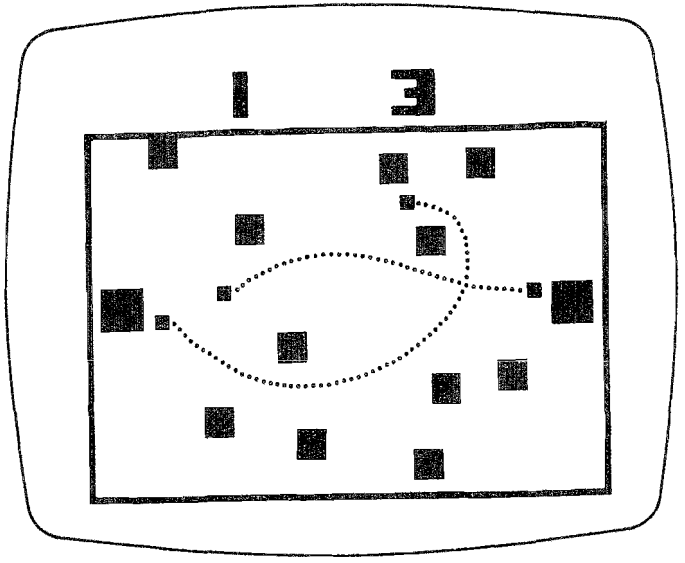


Fig.4

Juggle I

The game combines timing and judgment as the players launch missiles against each other in an attempt to have the missile hit a wall or obstacle while on the opponent's half of the playing area. The players have control of the missiles on their side of the playing area which they are able to steer in a right or left direction with their controllers

Play begins when both players have depressed their five buttons which launch simultaneous missiles from the player's squares The players then guide the missiles past the obstacles to the opponent's half of the playing area, where the opponent gains control of the incoming missile The player must then turn the missile to return it to his opponent. Each match ends when both missiles have collided with fixed objects and the players start a new match. The game ends when 31 points have been scored by either player

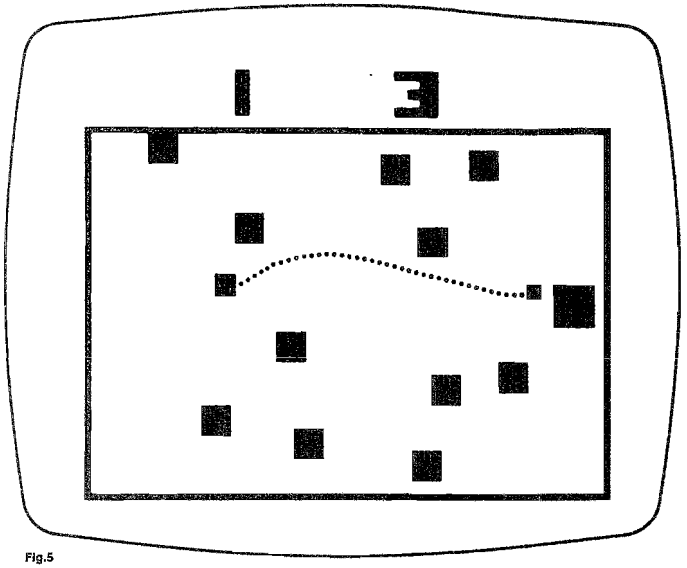


Fig.5

Juggle II

There is also a single missile version of the Juggle game where the player who was last scored against, launches the missile against his opponent

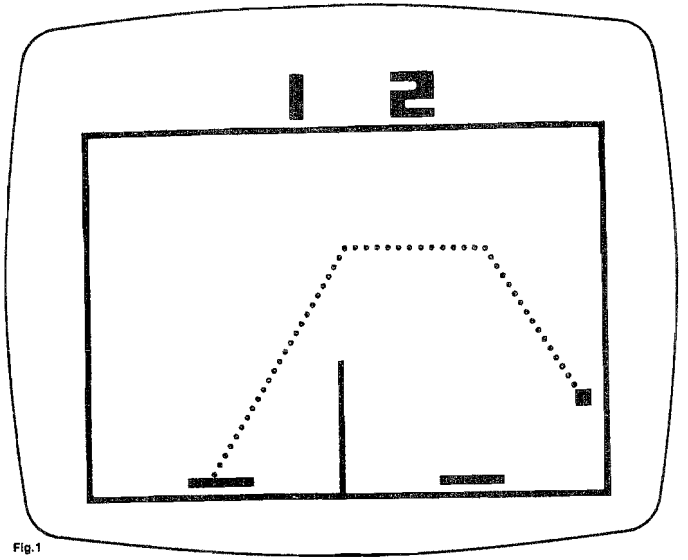


Fig.1

Volleyball

The Volleyball game uses the closed playing area shown above The players must hit the ball over the net to the opposing player. Failure to hit the ball, or hitting the ball against any wall is considered a foul

The game scoring is identical to the real game in that a foul by the server only results in loss of service and a foul made when not serving scores a point.

Ball travel approximates a parabolic path, and the distance of travel is directly related to the angle of the hit High angle hits result in shorter horizontal travel than the low angle hits

A score of 15 points by either player ends the game

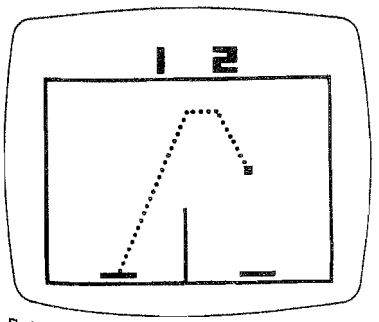


Fig.1a High Angle

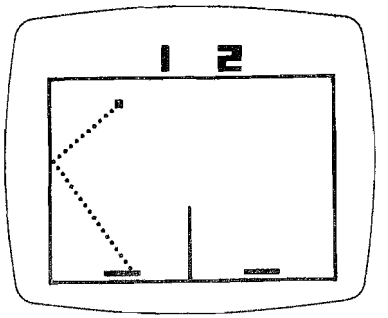


Fig.1b Foul

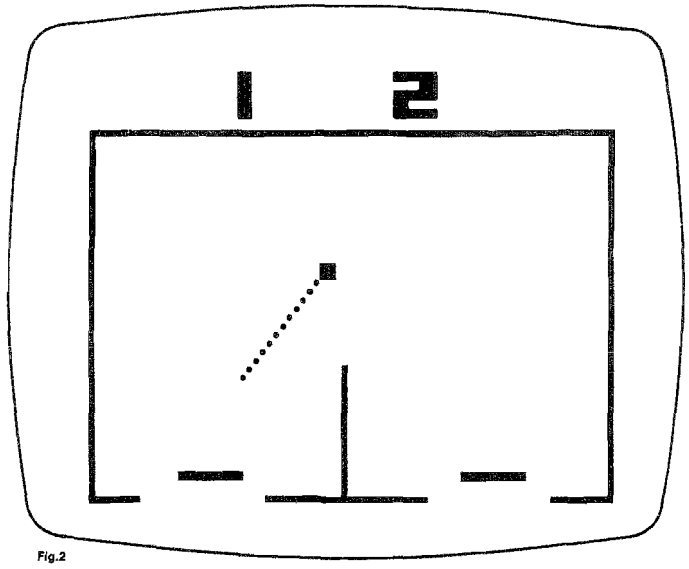


Fig.2

Protection

In this game, the player must protect the goal area of their sides of the net to prevent the ball from dropping through the goal opening. The ball may be played off of all surfaces and shots may rebound from the net or back wall. The game starts when the player who was last scored against depresses his serve button. The ball will then travel with a random angle to the opposing player who must return the ball before it falls through the goal area. Play continues until one of the players misses the ball and it goes through the goal.

The game ends at 15 points.

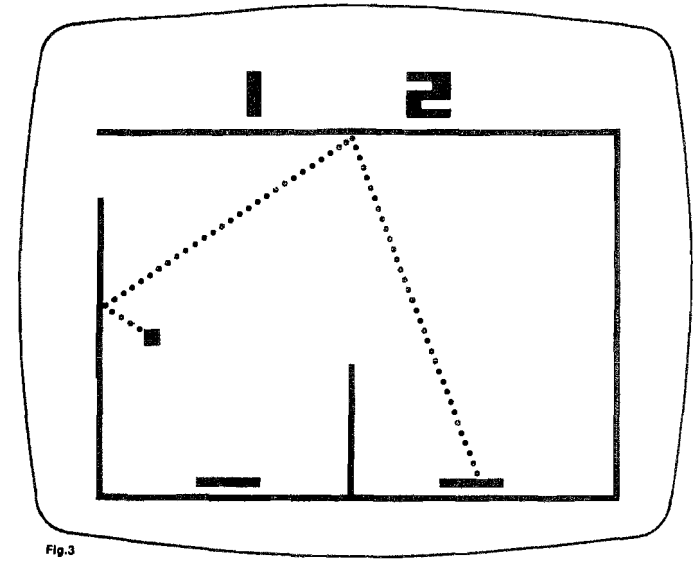


Fig.3

Hazard

The Hazard game is one of skill and luck where the object of the game is to keep from hitting the ball into the goal opening which is in constant and random motion around the boundary area. Should the ball go through the moving goal, the player having hit the ball is at fault and loses the point. It is therefore incumbent on the players to anticipate the location of the goal and hit the ball at the proper point on the bat to angle the ball so that it will hit a boundary. After a goal is made, the ball is next served by the player receiving the last point.

The game ends on a score of 15 points by either player.

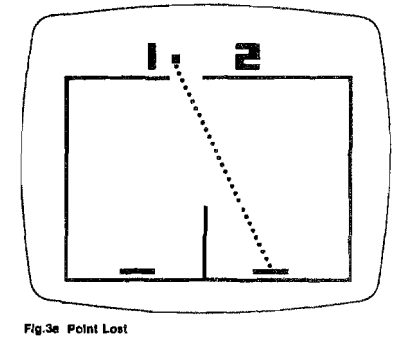


Fig.3a Point Lost

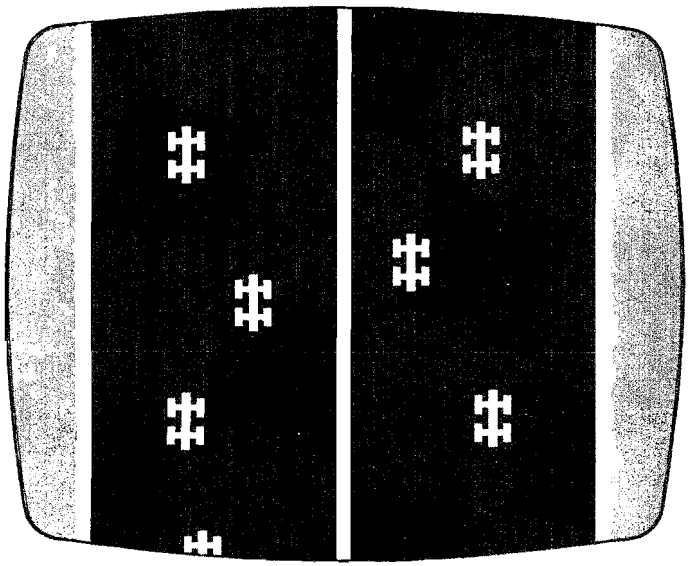


Fig.1

Roadrace

The Roadrace tests the skill and reaction time of one or two players who try to race down a "road" filled with traffic without colliding with any of the cars they are passing.

On game reset, the cars start accelerating and passing the slower traffic as they accelerate. Steering is controlled to the left or right by the corresponding motion of the joystick. Acceleration continues until one of the vehicles collides with a slower car at which time the game and the score is displayed. After five seconds, the score disappears and the race cars resule their acceleration.

The game ends when either player has nad 15 collisions.

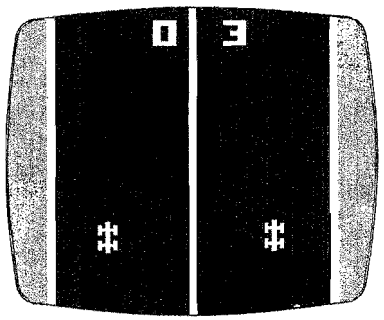


Fig.1a On Collision, game stops and number of collisions by each player is shown.

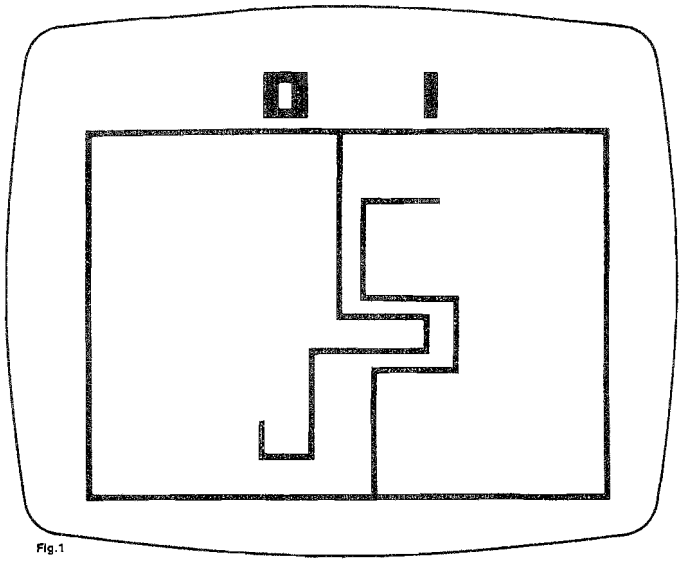


Fig.1

Barricade

The object of Barricade is to keep a constant velocity track, steerable in the vertical or horizontal direction, moving without crossing itself or a track made by the opponent. Skill and strategic playing are required for if either player intersects his own track or the track of his opponent, the track stops, a new track begins at the origin, and a point is scored for the opponent.

A score of three for either player terminates the game.

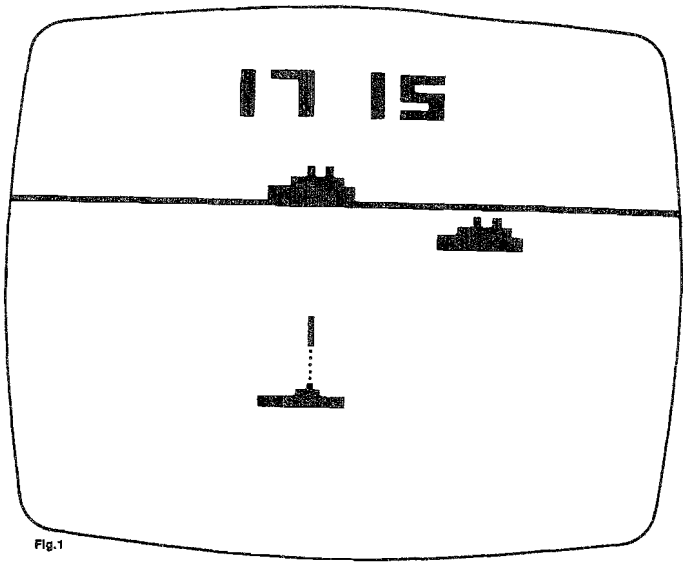


Fig.1

Submarine

Survival at saa is the objective of the submarine game with the surface fleet trying to depth charge the submarine and the submarine trying equally hard to torpedo the surface ships. The surface commander has a fleet of cargo and capital ships which he must protect with his destroyer. The destroyers are capable of dropping depth charges to stop and destroy the submarine and this ship can move left and right to fire. The other surface ships automatically move across the screen at various speeds to elude the sub. Each hit on the submarine counts for two points.

The submarine commander moves his submarine left and right at the bottom of the screen. His mission is to destroy cargo and capital ships as well as the destroyer. Each hit on a cargo ship counts for one point, a capital ship hit counts for two points and a destroyer hit, for five points.

Score are individually displayed and 31 points wins the game.

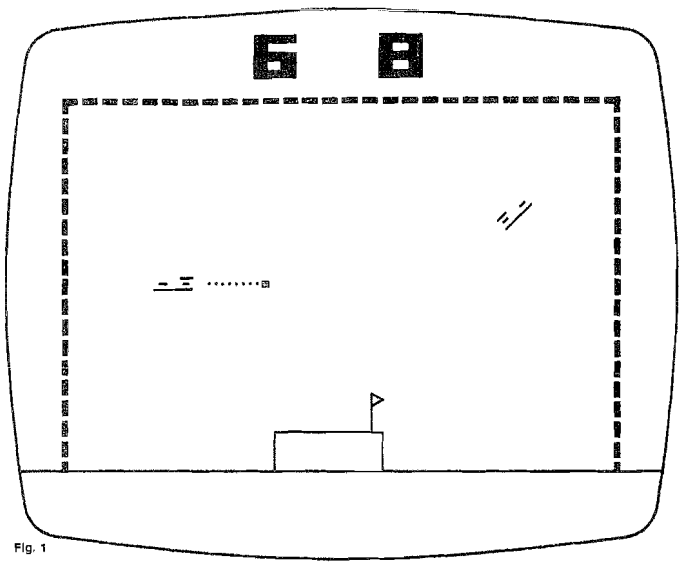
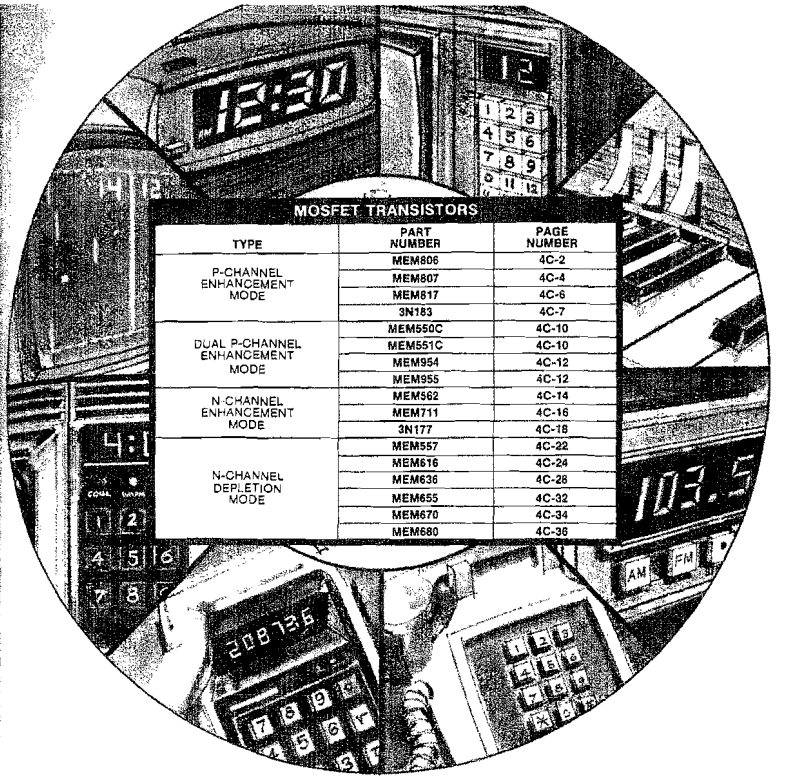


Fig. 1

Dogfight

The Dogfight Game locks two aircraft in aerial combat. The planes are controllable in both speed and direction by either one or two players whose objective is to destroy the other's aircraft with gun fire. Points for shooting down the other player are talliad by an on-screen counter and points are also scored when a player is hit by the ring of anticraft fire surrounding the playing area. The first player to score 31 is the victor and terminates play.

When only one player is using the game, the other aircraft flies continuously with it's gun firing. The player must carefully approach the aircraft and shoot it down without being hit himself.



MOSFET TRANSISTORS

MOSFET TRANSISTORS

MICRO ELECTRONICS

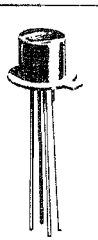
P-Channel Enhancement Mode MOSFETS

FEATURES

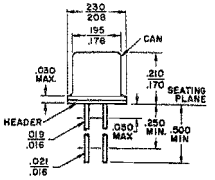
- High breakdown voltage
- Low input and drain to gate capacitance
- High "off" resistance
- Very high ratio of "off" to "on" resistance
- Normally off and zero offset voltage

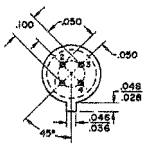
APPLICATIONS

- Low level chopper application
- Low level detector
- Sample and hold circuit
- Analog switching
- Multiplexers
- Operational amplifiers



TO-72





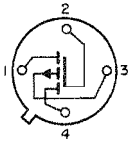
BOTTOM VIEW

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

	MEM 806/MEM 806A
Drain to Source Voltage	−40V
Drain to Gate Voltage	−40V
Gate to Source Voltage	−40V
Transient Gate to Source Voltage	±125V
Storage Temperature	−65°C to +150°C
Operating Temperature	−65°C to +150°C
Total Dissipation at 25°C Case Temperature	600mW
Total Dissipation at 25°C Ambient Temperature	300mW

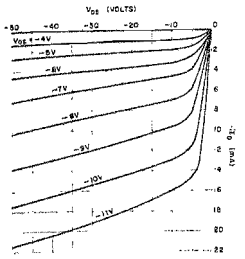
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

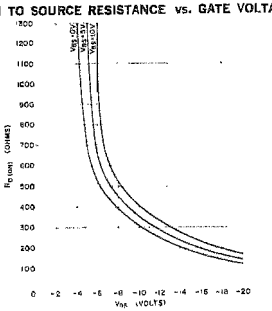
SYMBOL	CHARACTERISTIC	MEM806 MIN.	MEM806 MAX.	MEM806A MIN.	MEM806A MAX.	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−2.0	−5.5	−2.0	−5.5	Volts	$V_{DS} = V_D$, $I_D = 10\ \mu A$ $V_{BS} = 0V$
I_{DS1}	Drain Leakage Current		−1.0		−0.10	nA	$V_{DS} = -20V$, $V_{GS} = V_{BS} = 0V$
I_{GS1}	Source Leakage Current		−1.0		−0.10	nA	$V_{GS} = -20V$, $V_{DB} = V_{FD} = 0V$
I_{GSS}	Gate Leakage Current		−3.0		−1.0	pA	$V_{GS} = -20V$, $V_{DS} = V_{BS} = 0V$
$I_{D(on)}$	Drain Current	−5.0		−5.0		mA	$V_{GS} = V_{DS} = -15V$
BV_{GSS}	Drain-Source Breakdown	−40		−40		Volts	$I_D = -10\ \mu A$, $V_{GS} = V_{DS} = 0V$
BV_{DSS}	Source-Drain Breakdown	−40		−40		Volts	$I_S = -10\ \mu A$, $V_{GB} = V_{SB} = 0V$
$R_{DS(on)}$	Drain to Source on Resistance		300		300	ohms	$V_{GS} = -15V$, $I_D = 100\ \mu A$
Y_{fs}	Transadmittance	2000		2000		μmhos	$V_{DS} = -20V$, $f = 1KHz$, $I_{DS} = 10mA$
C_{gs}	Gate to Source Capacitance		2.0		2.0	pF	$V_{GS} = -10V$, $I_D = 10mA$
C_{ds}	Drain to Source Capacitance		0.3		0.3	pF	$V_{DS} = -10V$, $I_D = 10mA$
C_{gd}	Gate to Drain Capacitance		1.5		1.5	pF	$V_{DS} = -10V$, $I_D = 10mA$

TYPICAL CHARACTERISTIC CURVES

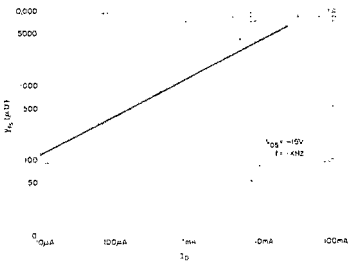
TRANSFER CHARACTERISTICS



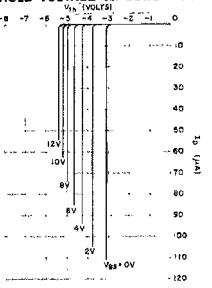
DRAIN TO SOURCE RESISTANCE vs. GATE VOLTAGE



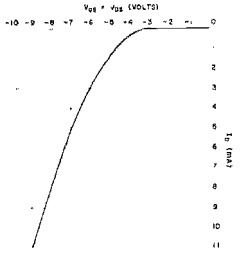
FORWARD TRANSCONDUCTANCE vs. DRAIN CURRENT



THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



TURN-ON CHARACTERISTICS



4C

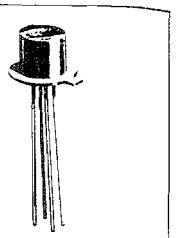
P-Channel Enchancement Mode MOSFETS

FEATURES

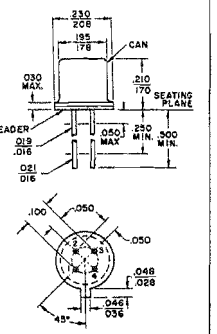
- High breakdown voltage
- Low input and gate to drain capacitance
- High drain to source off resistance
- Very high ratio of "off" to "on" resistance
- Normally off with zero gate voltage
- Zener protective diode

APPLICATIONS

- Low level chopper application
- Analog switching
- Sample and hold circuit
- Multiplexers
- Audio amplifier
- Operational amplifiers



TO-72



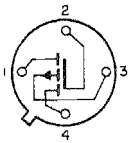
BOTTOM VIEW

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Gate
3. Substrate (Case)
4. Source



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

	MEM 807/MEM 807A
Drain to Source Voltage	−40V
Drain to Gate Voltage	−40V
Gate to Source Voltage	−40V
Transient Gate to Source Voltage	±125V
Storage Temperature	−65°C to +150°C
Operating Temperature	−65°C to +150°C
Total Dissipation at 25°C Case Temperature	600mW
Total Dissipation at 25°C Ambient Temperature	300mW

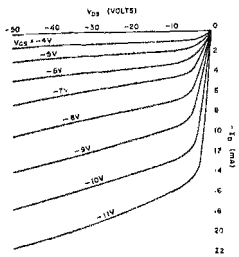
ELECTRICAL CHARACTERISTIC

(T_A = 25°C, unless otherwise specified — body grounded)

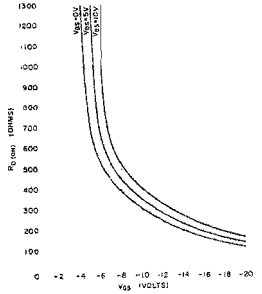
SYMBOL	CHARACTERISTIC	MEM807 MIN.	MEM807 MAX.	MEM807A MIN.	MEM807A MAX.	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−2.0	−5.5	−2.0	−5.5	Volts	$V_{DS} = V_{GS}$ $I_D = 10\ \mu A$ $V_{BS} = 0V$
I_{DSS}	Drain Leakage Current		−1.0		−0.10	nA	$V_{DS} = -20V$, $V_{GS} = V_{BS} = 0V$
I_{SSS}	Source Leakage Current		−1.0		−0.10	nA	$V_{SD} = -20V$, $V_{GD} = V_{BS} = 0V$
I_{GSS}	Gate Leakage Current		−0.20		−0.05	nA	$V_{GS} = -20V$, $V_{DS} = V_{BS} = 0v$
$I_{D(on)}$	Drain Current	−5.0		−5.0		mA	$V_{DS} = V_{GS} =$ $-15V$
BV_{DSS}	Drain-Source Breakdown	-40		−40		Volts	$I_D = -10\ \mu A$, $V_{GS} = V_{BS} = 0V$
BV_{DBS}	Source-Drain Breakdown	−40		−40		Volts	$I_S = -10\ \mu A$, $V_{DG} = V_{BG} = 0V$
BV_{GSS}	Gate to Source Breakdown	-40		−40		Volts	$I_G = -10\ \mu A$, $V_{SD} = V_{BD} = 0V$
$R_{DS(on)}$	Drain to Source on Resistance		300		300	ohms	$V_{GS} = -15V$, $I_D = 100\ \mu A$
Y_{fs}	Transadmittance	2000		2000		μmhos	$V_{DS} = -20V$ f = 1KHz, $I_{DS} = 10mA$
C_{gs}	Gate to Source Capacitance		2.0		2.0	pF	$V_{GS} = -10V$, $I_D = 10mA$
C_{ds}	Drain to Source Capacitance		0.3		0.3	pF	$V_{DS} = -10V$, $I_B = 10mA$
C_{gd}	Gate to Drain Capacitance		1.5		1.5	pF	$V_{DS} = -10V$, $I_G = 10mA$

TYPICAL CHARACTERISTIC CURVES

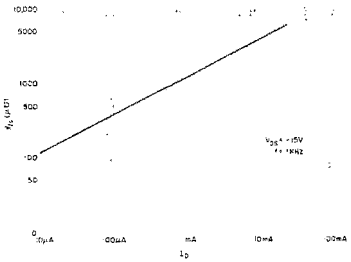
TRANSFER CHARACTERISTICS



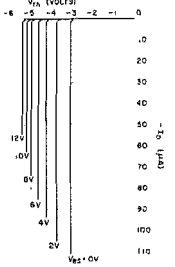
DRAIN TO SOURCE RESISTANCE vs. GATE VOLTAGE



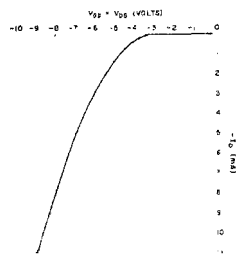
FORWARD TRANSCONDUCTANCE vs. DRAIN CURRENT



THRESHOLD VOLTAGE vs. SUBSTRATE BIAS



TURN-ON CHARACTERISTICS



P-Channel Enhancement Mode MOSFET

FEATURES

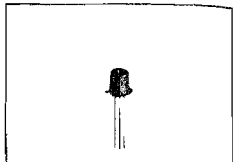
- High breakdown voltage
- Low input and drain to gate capacitance
- High "off" resistance
- Very high ratio of "off" to "on" resistance
- Normally off and zero offset voltage

APPLICATIONS

- Low level chopper application
- Low level detector
- Sample and hold circuit
- Analog switching
- Multiplexers
- Operational amplifiers
- Smoke Detector

MAXIMUM RATINGS

Drain to Source Voltage 45V
Drain to Gate Voltage 45V
Gate to Source Voltage ..... ±200V
Storage Temperature ..... -50°C to 150°C
Operating Temperature ..... -50°C to 125°C
Total Dissipation at 25°C Case Temperature 400mW
Total Dissipation at 25°C Ambient Temperature 225mW



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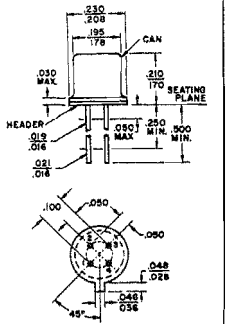
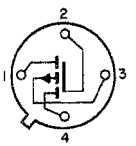


Bottom View

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Substrate (Case)
4. Source



ELECTRICAL CHARACTERISTICS Body Connected To Source.

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = -20V, I_{DS} = -10\mu A$	-2.5	–	-5.5	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -20V, V_{GS} = 0V$	–	–	-3	nA
I_{SDS}	Source Leakage Current	$V_{SD} = -20V, V_{GSD} = 0V$	–	–	-5	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = -25V, V_{DS} = 0V$	–	–	-1	pA
BV_{DSS}	Drain Breakdown Voltage	$I_{DS} = -10\mu A, V_{GS} = -0V$	-35	-45	–	V
BV_{GDX}	Gate, Oxide Breakdown Voltage	$V_{DS} = 0V$	±200	±225	–	V
$I_{D(on)}$	Drain Current	$V_{GS} = V_{DS} = -10V$	-3	-12	–	mA
$R_{D(on)}$	Drain-to-Source on resistance	$V_{GS} = -15V, I_{DS} = -1mA$	–	–	350	Ω
Y_{fs}	Forward Transadmittance	$V_{GS} = V_{DS} = -10V$	1000	2000	–	umhos
C_{iss}	Total Gate Input Capacitance	$V_{GS} = V_{DS} = -10V$ f = 1MHz	–	3.5	6	pF
C_{oss}	Total Drain Output Capacitance	$V_{GS} = V_{DS} = -10V$, f = 1MHz	–	2.5	5	pF
C_{rss}	Reverse Transfer Capacitance	$V_{GS} = V_{DS} = -10V$, f = 1MHz	–	1.2	2.5	pF
A_{GS}	Voltage Gain As Source Follower	$V_{DS} = -15V, R = 10K$ (Source) R(from gate to ground) = 10^9 ohms	–	0.8	–	–

p-Channel Enhancement Mode MOSFETS

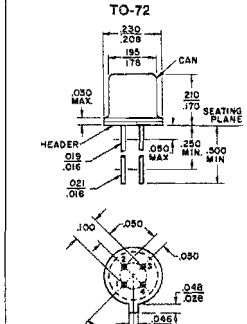
FEATURES

- One Watt Power Dissipation
- Low Drain-Source "ON" Resistance
- 10^{10} Ohms Input Resistance
- Integrated Zener Protects the Gate
- Normally "OFF" with Zero Gate Voltage
- Square Law Transfer Characteristics
- High Ratio of "OFF" to "ON" Resistance

APPLICATIONS

- Designed Primarily for Medium Power Switching and Chopper Applications
- Series and Shunt Choppers
- Analog Switch
- Multiplexers
- Low Impedance Device Driver

TO-72

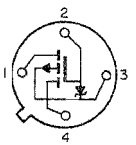


BOTTOM VIEW

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead
1. Drain
2. Gate
3. Substrate (Case)
4. Source



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

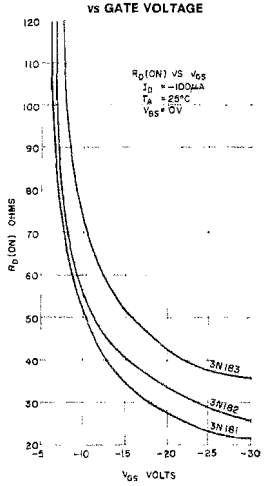
	3N181	3N182	3N183
Drain—Source Voltage	—30V	—30V	—25V
Drain—Gate Voltage	—30V	—30V	—25V
Gate Current (Forward Direction for Zener Clamp)	0.1mA	0.1mA	0.1mA
Gate Current (Reverse Direction for Zener Clamp)	1.0mA	1.0mA	1.0mA
Drain Current	100mA	100mA	100mA
Storage Temperature	—65°C to +200°C	—65°C to +200°C	—65°C to +200°C
Operating Temperature	—65°C to +150°C	—65°C to +150°C	—65°C to +150°C
Total Dissipation at 25°C Case Temp.	1.0 W	1.0 W	1.0 W
Total Dissipation at 25°C Ambient Temp.	300mW	300mW	300mW
Derating Factor	2.4mW/°C	2.4mW/°C	2.4mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

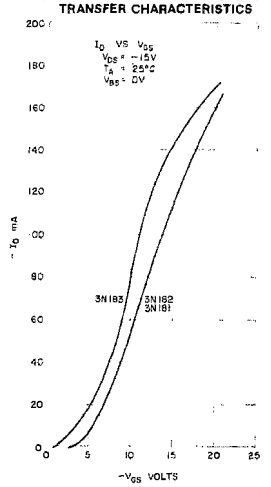
SYMBOL	DC CHARACTERISTICS	3N181 MIN	3N181 MAX	3N182 MIN	3N182 MAX	3N183 MIN	3N183 MAX	UNITS	CONDITIONS
$V_{GS(TH)}$	Threshold Voltage	3.0	4.0	2.5	5.0	2.0	6.0	Volts	$V_{DS} = -10V$, $I_D = -10\mu A$
I_{DSS}	Drain Leakage Current	—	0.5	—	2.5	—	10.0	nA	$V_{DS} = -20V$, $V_{GS} = 0V$
I_{DSS}	Drain Leakage Current	—	10.0	—	15.0	—	25.0	μA	$V_{DS} = -20V$, $V_{GS} = 0V$, $T_A = 150°C$
I_{GSS}	Source Leakage Current	—	1.0	—	5.0	—	10.0	nA	$V_{SD} = -20V$, $V_{GD} = 0V$
I_{GF}	Gate Forward Current	—	250	—	500	—	1000	pA	$V_{GS} = -20V$, $V_{DS} = 0V$
I_{GF}	Gate Forward Current	—	5.0	—	10.0	—	25.0	μA	$V_{GS} = -20V$, $V_{DS} = 0V$, $T_A = 150°C$
BV_{DSS}	Drain Breakdown Voltage	30	—	30	—	25	—	Volts	$I_D = -10\mu A$, $V_{GS} = 0V$
BV_{SDS}	Source Breakdown Voltage	30	—	30	—	25	—	Volts	$I_S = -10\mu A$, $V_{GD} = 0V$
V_{GSF}	Gate to Source Forward Voltage	30	—	30	—	25	—	Volts	$I_G = -10\mu A$, $V_{DS} = 0V$
$I_{D(ON)}$	Drain Current	40	—	40	—	25	—	mA	$V_{DS} = V_{GS} = -15V$
$R_{DS(ON)}$	Drain-Source on Resistance	—	45	—	60	—	75	Ohms	$V_{GS} = -15V$, $V_{DS} = 0V$, $I_D = 0.1mA$
$V_{DS(ON)}$	Drain-Source on Voltage	—	225	—	300	—	375	mV	$V_{GS} = -20V$, $I_D = 0.5mA$

SYMBOL	AC CHARACTERISTICS	3N181 MIN	3N181 MAX	3N182 MIN	3N182 MAX	3N183 MIN	3N183 MAX	UNITS	CONDITIONS
Y_{fs}	Forward Transadmittance	8000	—	8000	—	8000	—	μmhos	$V_{DS} = -15V$, $I_D = 25mA$, $f = 1kHz$
C_{iss}	Input Capacitance	—	25	—	25	—	30	pF	$V_{DS} = -15V$, $V_{GS} = 0V$, $f = 1MHz$
C_{os}	Drain to Source Capacitance	—	0.05	—	0.075	—	0.1	pF	$V_{DS} = -15V$, $V_{GS} = 0V$, $f = 1MHz$
C_{gd}	Gate to Drain Capacitance	—	8.0	—	10	—	12	pF	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$
$t_{d(on)}$	Turn-On Delay Time	—	30	—	35	—	40	ns	$R_1 = R_2 = 3.7K$ Ohms See Circuit Diagram Below
t_r	Rise Time	—	30	—	35	—	40	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	50	—	55	—	55	ns	
t_f	Fall Time	—	180	—	180	—	180	ns	

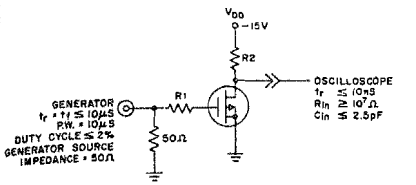
DRAIN TO SOURCE RESISTANCE vs GATE VOLTAGE

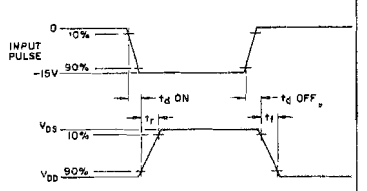


DRAIN CURRENT vs GATE VOLTAGE TRANSFER CHARACTERISTICS

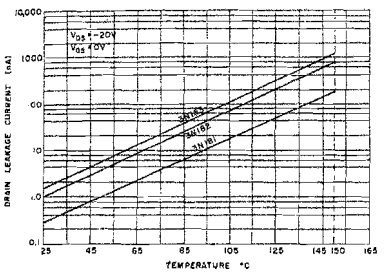


SWITCHING CIRCUIT FOR P-CHANNEL ENHANCEMENT

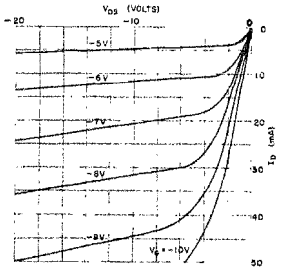




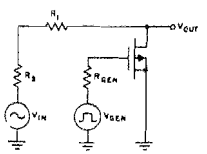
DRAIN (OR SOURCE) CURRENT vs TEMPERATURE



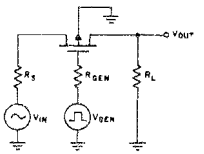
CHARACTERISTIC CURVE



SERIES CHOPPER (or MULTIPLEX CELL)

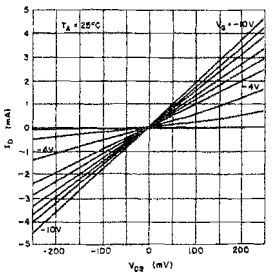


SHUNT CHOPPER



RANGE OF TYPICAL VALUES	
V_{GEN}	0 to −25V Square Wave 20Hz to 100kHz
V_{IN}	+0.5V (Max) / −20V (Max) A.C. or D.C. Signal
V_{OUT}	Chopped Output
R_S	1KΩ to 1MΩ
R_{GEN}	50Ω to 1MΩ
R_L	10KΩ to 10MΩ
R_1	1K to 1MΩ

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



MEM 550 MEM 550C
MEM 551 MEM 551C

Dual P-Channel Enhancement Mode MOSFETS

FEATURES

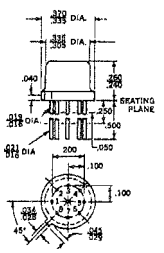
- 10^{10} ohms input resistance (MEM 550 Series)
- 10^{15} ohms input resistance (MEM 551 Series)
- Integrated zener clamp protects the gate (MEM 550 Series)
- Normally off with zero gate voltage
- Square Law transfer characteristics

APPLICATIONS

- Analog switches
- Series and shunt choppers
- Operational amplifiers
- Logic circuits
- Linear RF amplifiers
- Multiplexers
- Very high input impedance amplifiers (MEM 551 Series)

Actual Size

TO-77



Bottom View

Note: All dimensions in inches

MAXIMUM RATINGS

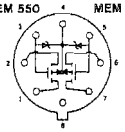
	MEM 550	MEM 551	MEM 550C	MEM 551C
Drain to Source Voltage	−30V	−30V	−25V	−25V
Source to Drain Voltage	−30V	−30V	−25V	−25V
Gate to Source Voltage	−30V	±30V	−25V	−25V
Gate to Drain Voltage	−30V	−30V	−25V	−25V
Gate Current (Forward Direction for Zener Clamp)	+0.1mA	—	±0.1mA	—
Drain Current	−25mA each side		−25mA each side	
Storage Temperature	−50 To 150°C		−50 To 125°C	
Operating Junction Temperature	−50 To 125°C		−50 To 100°C	
Total Dissipation at 25°C Case Temperature	325mW each side		250mW each side	
Total Dissipation at 25°C Ambient Temperature	112mW each side		85mW each side	

TERMINAL DIAGRAM

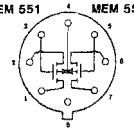
Lead

1 Drain 1	5. Gate 2
2 Source 1	6. Source 2
3 Gate 1	7 Drain 2
4. Substrate (Body)	8 Open

MEM 550 / MEM 550C



MEM 551 / MEM 551C



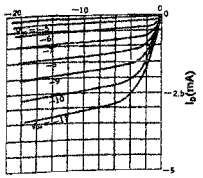
ELECTRICAL CHARACTERISTICS (for each side — body grounded)

SYMBOL	CHARACTERISTIC	CONDITIONS	MEM 550 MEM 551 MIN	MEM 550 MEM 551 TYP	MEM 550 MEM 551 MAX	MEM 550C MEM 551C MIN	MEM 550C MEM 551C TYP	MEM 550C MEM 551C MAX	UNITS
$V_{GS(T)}$	Gate Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -10\mu A$	−3	-	−6	−3	—	-6	V
I_{DSS}	Drain Leakage Current	$V_{DS} = -20V, V_{GS} = 0V$	—	−0.2	−10	—	—	−10	nA
I_{SOS}	Source Leakage Current	$V_{DS} = -20V, V_{GS} = 0V$	—	−0.2	−10	—	—	−10	nA
I_{GSS}	Gate Leakage Current	$V_{GS} = -15V$, $V_{DS} = 0V$ MEM 550	—	−0.1	−1	—	—	—	pA
		MEM 551	—	—	−1	—	—	—	
		MEM 550C	—	—	—	—	−0.03	−1	
		MEM 551C	-	—	—	—	-	−10	
$I_{D(on)}$	Drain Current	$V_{DS} = V_{DS} = -10V$	−1.5	−5	—	−1.5	−5	—	mA
BV_{DSS}	Drain-Source Breakdown	$I_D = -10\mu A, V_{GS} = 0V$	−30	−50	—	−25	−50	—	V
BV_{SDS}	Source-Drain Breakdown	$I_S = -10\mu A, V_{GS} = 0V$	−30	−50	-	−25	−50	—	V
BV_{GSS}	Gate to Source Breakdown	$I_{GS} = -10\mu A, V_{DS} = 0V$	−30	−50	—	−25	−50	—	V
Y_{fs}	Transadmittance	1kHz, $V_{GS} = V_{DS} = -10V$	500	—	—	500	—	—	μmho
C_{GS}	Gate to Source Capacitance	$V_{GS} = V_{DS} = -10V$	—	1.1	—	—	—	4	pF
C_{gd}	Gate to Drain Capacitance	$V_{GS} = V_{DS} = -10V$	—	1.1	—	—	—	4	pF
C_{ds}	Drain to Source Capacitance	$V_{GS} = V_{DS} = -10V$	-	0.15	—	—	—	0.2	pF
$r_{DS(on)}$	Drain to Source on Resistance	$V_{GS} = -15V, V_{DS} = 0V$	—	250	—	—	—	400	ohms
Y_{fs1}/Y_{fs2}	Transadmittance Ratio	$V_{DS} = -10V, I_{DS} = 250\mu A$	0.8	-	1.0	0.8	-	1.0	mV
$V_{GS1}-V_{GS2}$	Gate Voltage Differential	$V_{DS} = -10V, I_{DS} = 250\mu A$	—	70	200	-	70	200	mV

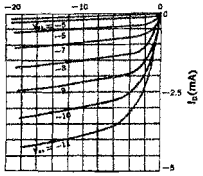
TYPICAL CHARACTERISTIC CURVES

MEM 550 / MEM 551

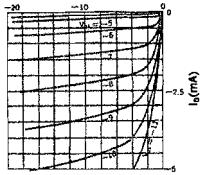
DRAIN CHARACTERISTICS AT 125°C
V_{DS} (VOLTS)



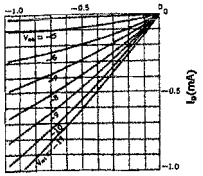
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



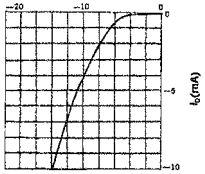
DRAIN CHARACTERISTICS AT −70°C
V_{DS} (VOLTS)



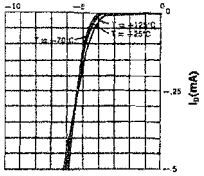
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

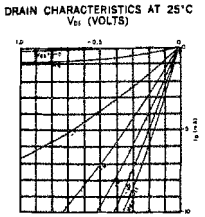


TURN-ON CHARACTERISTICS
$V_{GS} = V_{DS}$ (VOLTS)

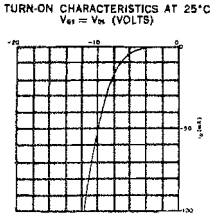


MEM 550C / MEM 551C

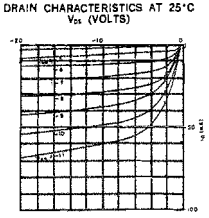
DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



TURN-ON CHARACTERISTICS AT 25°C
$V_{GS} = V_{DS}$ (VOLTS)

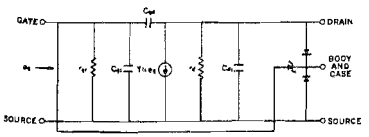


DRAIN CHARACTERISTICS AT 25°C
V_{DS} (VOLTS)



SMALL SIGNAL EQUIVALENT CIRCUIT FOR EACH SIDE

(Conditions: $V_{GS} = V_{DS} = 10V$)
$I_D \approx 3mA$



SYMBOL	CHARACTERISTIC	TYPICAL VALUE	UNITS
Diodes	All diodes are to be considered perfect diodes		
r_{ss}	Gate to source leakage resistance and diode leakage resistance	10^{14}	ohms
r_d	Dynamic drain resistance	18	Kohms
C_{gs}	Gate to source capacitance	1.1	pF
C_{gd}	Gate to drain capacitance	1.1	pF
C_{ds}	Drain to source capacitance	0.15	pF
Y_{fs}	Forward transadmittance	1400	μmho

MEM 954 Series
MEM 955 Series

Dual P-Channel Enhancement Mode MOSFETS

FEATURES

- Normally off with zero gate voltage
- Square law transfer characteristics
- Tight Vos match
- Low temperature coefficient of ΔV_{GS}
- Specified for audio noise
- Low leakage currents
- 10^{15} OHMS input resistance (MEM 955 Series)
- 10^{12} OHMS input resistance (MEM 954 Series)
- Integrated zener clamp protects the gate (MEM 954 Series)

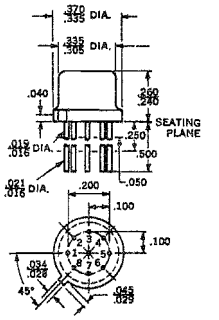
APPLICATIONS

Very high input impedance amplifiers
Series and shunt choppers
Operational amplifiers
Smoke detectors
Cryogenic amplifiers
Multiplexers
Analog switches

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain to source voltage ..... -35V
Source to drain voltage ..... -35V
Gate to source voltage ..... -40V
Gate to drain voltage ..... -40V
Gate current ..... +0.1 mA
(Fwd. direction for zener clamp) (MEM 954 Series)
Drain current ..... -50 mA each side
Storage temperature ..... -50°C to +150°C
Operating junction temperature ..... -50°C to +125°C
Total dissipation at 25°C case temperature ..... 300 mW each side
Total dissipation at 25°C ambient temperature ..... 112 mW each side

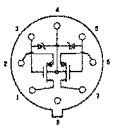
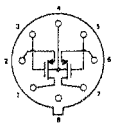
TO-77



Bottom view of 8 lead header
Note: All dimensions in inches

TERMINAL DIAGRAM

Lead
1. Drain 1
2. Source 1
3. Gate 1
4. Substrate (Body)
5. Gate 2
6. Source 2
7. Drain 2
8. Open

MEM 954 Series	MEM 955 Series
	

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

Symbol	Characteristics	MEM	Min.	Typ.	Max	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown	954 Series 955 Series	−35			V	V_{GS}=0V V_{BS}=0V I_D=−10μA
BV_{SDS}	Source-Drain Breakdown		−35			V	V_{SD}=0V V_{GD}=0V I_S=−10μA
BV_{GSS}	Gate-Source Breakdown		−40			V	V_{BS}=V_{BS}=0V I_G=−10μA
$V_{GS(TH)}$	Gate-Source Threshold Voltage		−2.0	−3.5	−5.0	V	V_{DS}=V_{GS}, I_D=−10μA
$R_{DS(ON)}$	Drain To Source On Resistance			100	150	Ω	V_{GS}=−15V V_{BS}=0V I_D=0.1 mA
Y_{fs}	Forward Transadmittance		700	1400		μmho	V_{DS}=−10V I_D=500μA V_{BS}=0V, f=1.0 kHz
Y_{fs1}/Y_{fs2}	Transadmittance Ratio		0.9		1.1	—	V_{DS}=−10V I_D=500μA V_{BS}=0V, f=1.0 kHz
E_{N1}	Equivalent Input Noise Voltage				700	$\frac{nV}{\sqrt{Hz}}$	V_{DS}=−10V I_D=500μA V_{BS}=0V f=100Hz, BW=1Hz
E_{N2}	Equivalent Input Noise Voltage				175	$\frac{nV}{\sqrt{Hz}}$	V_{DS}=−10V, I_D=500μA, V_{BS}=0V, f=1.0 kHz, BW=1 Hz
I_{DSS}	Drain Leakage Current	954, 954A, 955, 955A		08	1.0	nA	V_{DS}=−20V V_{GS}=V_{BS}=0V
		954B, 955B		.05	30		
I_{SDS}	Source Leakage Current	954, 954A, 955, 955A		08	1.0	nA	V_{SD}=−20V, V_{GD}=V_{BD}=0V
		954B, 955B		05	30		
I_{GSS}	Gate Leakage Current	954		03	30	nA	V_{GS}=−20V, V_{BS}=V_{DS}=0V
		954A, 954B		03	10		
		955, 955A		02	2.0	pA	V_{GS}=−40V, V_{BS}=V_{DS}=0V
		955B		02	1.0		
$\lvert V_{G1S}-V_{G2S} \rvert$	Gate Voltage Differential	954, 955			75	mV	V_{DS}=−10V I_D=500μA, V_{BS}=0V
		954A, 955A			25		
		954B, 955B			10		
$\frac{\Delta\lvert V_{G1S}-V_{G2S} \rvert}{\Delta T}$	Gate Voltage Differential Temp Coeff T_1=25°C, T_2=100°C	954, 955			150	μV/°C	V_{DS}=−10V I_D=500μA, V_{BS}=0V
		954A, 955A			50		
		954B, 955B			25		

4C

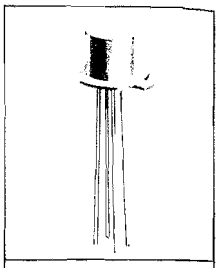
N-Channel Enhancement Mode MOSFETS

FEATURES
- 10^{12} ohms input resistance
- Normally off with zero gate voltage
- Square Law transfer characteristics
- Low insertion loss
- Low input and output capacitance

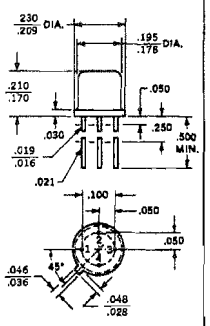
APPLICATIONS
- Logic circuits
- Switches
- Choppers
- Multiplexers
- Audio/RF Amplifier, Oscillators
- Operational Amplifiers

MAXIMUM RATINGS
(T_A = 25°C unless otherwise specified)

	MEM 562	MEM 562C
Drain to Source Voltage	±20 Volts	±20 Volts
Gate to Source Voltage	±10 Volts	±10 Volts
Gate to Drain Voltage	±30 Volts	±30 Volts
Drain Current I_D	Limited by Dissipation	Limited by Dissipation
Storage Temperature	−65 to 150°C	−50 to 125°C
Operating Junction Temperature	−65 to 125°C	−50 to 100°C
Total Dissipation		
@ 25°C Ambient Temperature	225mW	175 mW
@ 25°C Case Temperature	650mW	500 mW
Derate Linearly From	T_A = 25°C to 125°C @ 2.25mW/°C	
	T_C = 25°C to 125°C @ 6.5mW/°C	



TO-72

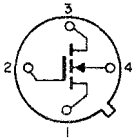


Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

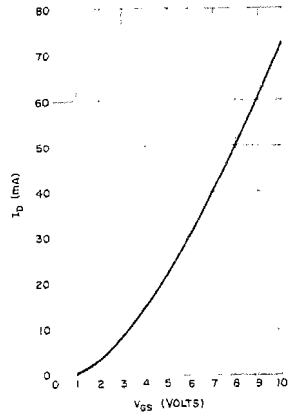
LEAD
1. Source
2. Gate
3. Drain
4. Substrate, case



ELECTRICAL CHARACTERISTICS
(T_A = 25°C. unless otherwise specified — body grounded)

Symbol	Characteristic	MEM 562 Min	MEM 562 Typ	MEM 562 Max	MEM 562C Min	MEM 562C Typ	MEM 562C Max	Units	Conditions
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	4.0	0.50	1.5	4.0	V	V_{DS} = V_{DS}, I_D = +10μA
I_{DSS}	Drain Leakage Current	—	—	10	—	—	10	nA	V_{DS} = +10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current	—	—	10	—	—	100	pA	V_{GS} = ±10V, V_{DS} = 0V
BV_{DSS}	Drain Breakdown Voltage	20	—	—	20	—	—	V	I_D ≤ +10μA, V_{GS} = 0V
$R_{DS(ON)}$	Drain to Source on Resistance	—	150	300	—	150	350	ohms	V_{GS} = +10V, I_D = 0.1mA
$I_{D(ON)}$	Drain Current	5	15	—	5.0	15	—	mA	V_{DS} = V_{DS}, = +10V
Y_{fs}	Forward Transadmittance	1000	—	—	1000	—	—	μmhos	V_{DS} = +10V, I_D = 2mA, f = 1kHz
C_{iss}	Total Gate Input Capacitance	—	3.0	4.0	—	3.0	5.0	pF	V_{DS} = 0V, V_{DS} = +10V, f = 1 MHz
C_{oss}	Total Drain Output Capacitance	—	3.0	4.0	—	3.0	5.0	pF	V_{DS} = 0V, V_{DS} = +10V, f = 1 MHz
C_{rss}	Gate to Drain Capacitance	—	0.3	0.5	—	0.3	0.6	pF	V_{DS} = 0V, V_{DS} = 0V, f = 1 MHz
t_d	Turn on Delay Time	—	—	45	—	—	55	nS	See Figure 1
t_r	Rise Time	—	—	65	—	—	75	nS	See Figure 1
$t_{(OFF)}$	Turnoff Time	—	—	160	—	—	170	nS	See Figure 1

DRAIN CURRENT vs GATE VOLTAGE
TRANSFER CHARACTERISTICS



DRAIN TO SOURCE RESISTANCE
vs GATE VOLTAGE

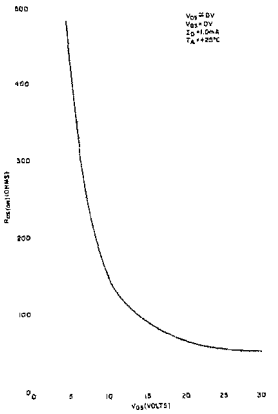
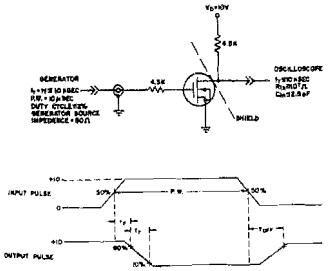
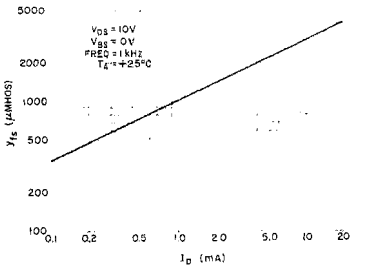


Fig. 1 SWITCHING TEST SET
MEM 562/MEM 562C



FORWARD TRANSADMITTANCE
vs DRAIN CURRENT



MEM 711

N-Channel Enhancement Mode MOSFET

FEATURES

- Monolithic Gate Protection Diode
- Low Feed-Through Capacitance
- Low ON Resistance
- Normally OFF with Zero Gate Drive

APPLICATIONS

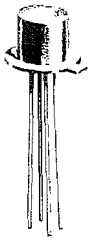
- High Speed Analog Switches
- Linear Amplifiers
- Series-Shunt Choppers
- Synchronous Detectors
- Level Shifters
- High Input Impedance Buffers

DESCRIPTION

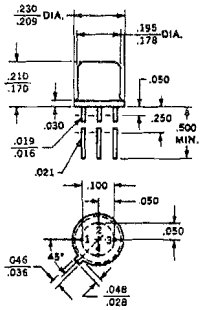
The MEM 711 is an N-channel, Enhancement Mode, Metal Oxide Semiconductor Field Effect Transistor, protected from excessive input voltages by a monolithic zener diode between gate and substrate. This MOSFET features a low threshold limit of 1.5 volts making possible direct drive from low voltage TTL logic levels. The low ON resistance and low feed-through capacitance make the MEM 711 ideally suited for high speed analog switching.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain to Source Voltage	V_{DS}	25 Volts
Gate to Source Voltage	V_{GS}	30 Volts
Gate to Drain Voltage	V_{GD}	30 Volts
Storage Temperature		−65 to 150°C
Operating Junction Temperature		−65 to 150°C
Total Dissipation @ 25°C Ambient Temperature		225 mW
@ 25°C Case Temperature		650 mW



TO-72



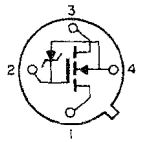
Bottom view

Note: All dimensions in inches.

TERMINAL DIAGRAM

LEAD

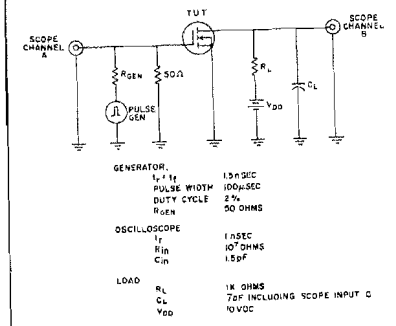
1. Source
2. Gate
3. Drain
4. Substrate, case

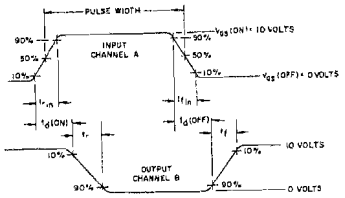


ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = +10V, I_D = +10μA, V_{BS} = 0V	0.50	–	1.5	V
I_{DSS}	Drain Leakage Current	V_{DS} = +10V, V_{GS} = 0V, V_{BS} = 0V	–	–	10	nA
I_{GSS}	Gate Leakage Current	V_{GS} = +10V, V_{DS} = 0V, V_{BS} = 0V	–	–	1.0	nA
BV_{DSS}	Drain Breakdown Voltage	I_D = +10μA, V_{GS} = 0V, V_{BS} = 0V	25	–	–	V
BV_{GSS}	Gate Breakdown Voltage	I_G = +10μA V_{DS} = V_{BS} = 0V	30	–	–	V
$R_{DS(ON)}$	Drain-to-Source on Resistance	V_{GS} = +10V, I_D = 0.1mA, V_{BS} = 0V	–	–	100	ohms
$I_{D(ON)}$	Drain Current	V_{DS} = V_{GS} = +10V, V_{BS} = 0V	10	–	–	mA
Y_{fs}	Forward Transadmittance	V_{DS} = +10V, I_D = 2mA, f = 1kHz, V_{BS} = 0V	1000	–	–	μmhos
C_{iss}	Total Gate Input Capacitance	V_{GS} = 0V, V_{DS} = +10V, f = 1 MHz, V_{BS} = 0V	–	–	6.0	pF
C_{oss}	Total Drain Output Capacitance	V_{GS} = 0V, V_{DS} = +10V, f = 1 MHz, V_{BS} = 0V	–	–	5.0	pF
C_{gd}	Gate-Drain Capacitance	V_{GS} = 0V, V_{DS} = 0V, f = 1 MHz, V_{BS} = 0V	–	–	1.0	pF
$t_{d(on)}$	Turn on Delay Time	V_{DD} = 10V	–	–	3	ns
t_r	Rise Time	$I_{D(on)}$ = 10mA, $V_{GS(on)}$ = 10V, $V_{GS(off)}$ = 0V — See Figure 1	–	–	5	ns
$t_{d(off)}$	Turnoff Delay Time		–	–	30	ns
t_f	Fall Time		–	–	60	ns

SWITCHING TEST CIRCUIT





N-Channel Enhancement Mode MOSFETS

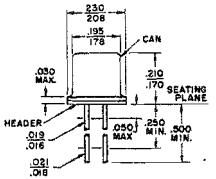
FEATURES

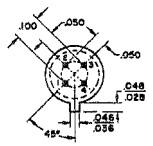
- Low Threshold Voltage
- Low Input and Gate to Drain Capacitance
- 10^{12} Ohms Input Resistance
- Normally "OFF" with Zero Gate Voltage
- Square Law Transfer Characteristics
- High Ratio of "OFF" to "ON" Resistance

APPLICATIONS

- Designed Primarily for Low Power Switching and Chopper Applications
- Complementary to P-Channel Enhancement MOS
- Series and Shunt Choppers
- Analog Switch
- Multiplexers
- Audio Amplifier
- Operational Amplifiers

TO-72





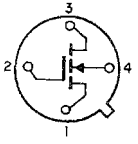
BOTTOM VIEW

Note: All dimensions in inches.

TERMINAL DIAGRAM

LEAD

1. Source
2. Gate
3. Drain
4. Bulk (Case)



MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

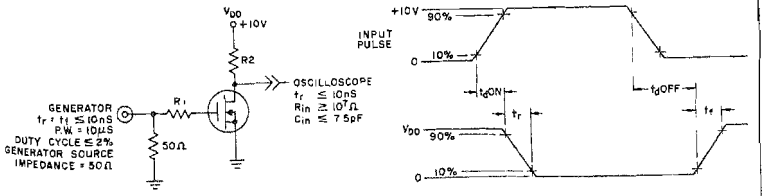
	3N175	3N176	3N177
Drain—Source Voltage	+30V	+25V	+20V
Drain—Gate Voltage	+30V	+25V	+20V
Forward Gate—Source Voltage	+35V	+30V	+20V
Reverse Gate—Source Voltage	−35V	−30V	−20V
Drain Current	50mA	50mA	50mA
Storage Temperature	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C
Operating Temperature	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Total Dissipation at 25°C Case Temp.	650mW	650mW	650mW
Total Dissipation at 25°C Ambient Temp.	225mW	225mW	225mW
Derating Factor	1.8mW/°C	1.8mW/°C	1.8mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

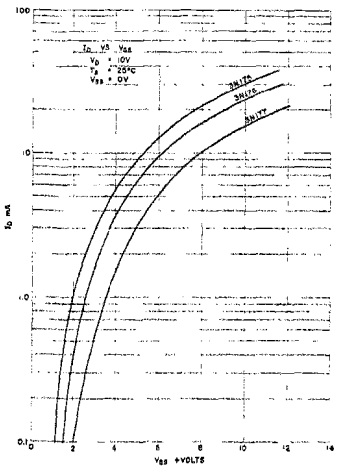
		3N175		3N176		3N177			
SYMBOL	DC CHARACTERISTICS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Threshold Voltage	1.0	2.0	1.0	2.5	1.0	3.5	Volts	V_{DS} = 10V, I_D = +10μA
I_{DSS}	Drain Leakage Current	—	5.0	—	10	—	25	nA	V_{DS} = +10V, V_{GS} = 0V
I_{GSS}	Drain Leakage Current	—	15	—	15	—	25	μA	V_{DS} = +10V, V_{GS} = 0V, T_A = 150°C
	Source Leakage Current	—	10	—	20	—	50	nA	V_{SD} = +10V, V_{GDS} = 0V
I_{GDS}	Gate Leakage Current	—	200	—	200	—	200	pA	3N175 V_G = +35V; 3N176 V_G = +30V; 3N177 V_G = +20V; V_{DS} = 0V
I_{GSS}	Gate Forward Current	—	100	—	500	—	1000	nA	3N175 V_G = +35V; 3N176 V_G = +30V; 3N177 V_G = +20V; V_{DS} = 0V, T_A = 150°C
$I_{D(ON)}$	Drain Current	20	—	15	—	10	—	mA	V_{DS} = V_{GS} = +10V
$R_{DS(ON)}$	Drain-Source on Resistance	—	200	—	300	—	500	Ohms	V_{GS} = +10V, V_{SS} = 0, I_D = 0.1mA
$V_{DS(ON)}$	Drain-Source on Voltage	—	440	—	660	—	1100	mV	V_{GS} = 10V, I_D = 2.2mA
BV_{DSS}	Drain Breakdown Voltage	35	—	30	—	20	—	Volts	I_D = +10μA, V_{GS} = 0V
BV_{SDS}	Source Breakdown Voltage	35	—	30	—	20	—	Volts	I_S = +10μA, V_{GSB} = 0V

		3N175		3N176		3N177			
SYMBOL	AC CHARACTERISTICS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
Y_{fs}	Forward Transadmittance	1200	—	1000	—	700	—	μmhos	V_{DS} = +15V, I_D = 2mA, f = 1kHz
C_{iss}	Input Capacitance	—	5.0	—	5.0	—	7.0	pF	V_{DS} = +15V, V_{GS} = 0V, f = 1MHz
C_{os}	Drain to Source	—	0.1	—	0.25	—	0.5	pF	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz
C_{rss} (C_{rss})	Gate to Drain Capacitance	—	0.5	—	0.5	—	0.75	pF	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
$t_{d(on)}$	Turn-On Delay Time	—	25	—	30	—	35	ns	R_L = R_S = 4.5K ohms See Circuit Diagram Below
t_r	Rise Time	—	30	—	35	—	40	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	50	—	55	—	60	ns	
t_f	Fall Time	—	150	—	150	—	150	ns	

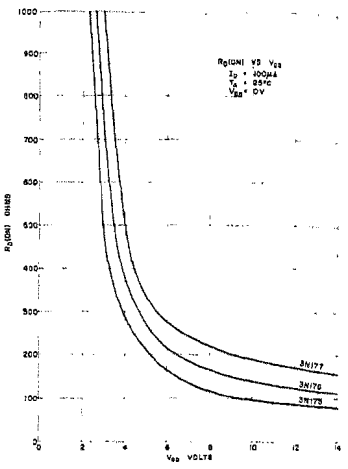
SWITCHING CIRCUIT FOR N-CHANNEL ENHANCEMENT



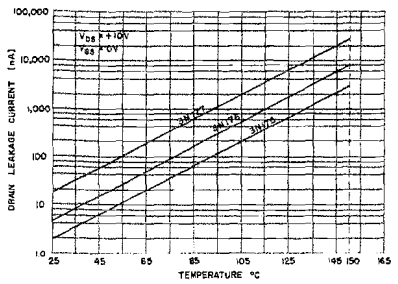
DRAIN CURRENT vs GATE VOLTAGE TRANSFER CHARACTERISTICS



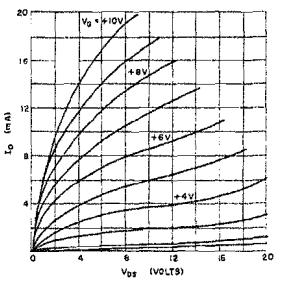
DRAIN TO SOURCE RESISTANCE vs GATE VOLTAGE



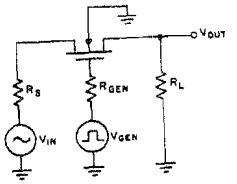
DRAIN (OR SOURCE) CURRENT vs TEMPERATURE



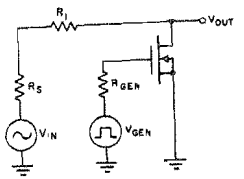
CHARACTERISTIC CURVE



SERIES CHOPPER (or MULTIPLEX CELL)

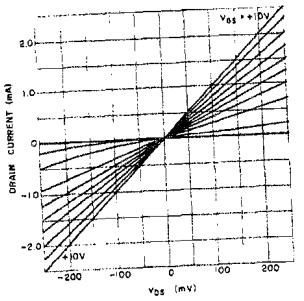


SHUNT CHOPPER



RANGE OF TYPICAL VALUES	
V_{GEN}	0 to −15V Square Wave 20Hz to 100kHz
V_{IN}	−0.5V (Max) + 10V (Max) A.C. or D.C. Signal
V_{OUT}	Chopped Outout
R_S	1KΩ to 1MΩ
R_{GEN}	50Ω to 1MΩ
R_L	10KΩ to 10MΩ
R	1K to 1MΩ

DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



4C

N-Channel Depletion Mode MOSFET

FEATURES

- 10^{13} ohms input resistance
- Low 3rd order distortion
- High gain — low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching

MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Drain-to-Source voltage, V_{DS}	+20V
Gate-to-Source voltage, V_{GS}	±30V
Gate-to-Drain voltage, V_{DG}	±30V
Drain Current, I_D	Limited by Dissipation
Storage Temperature	−65 to +150°C
Operating Junction Temperature	−65 to +150°C
Total Dissipation at 25°C Case Temperature	300 mW
Total Dissipation at 25°C Ambient Temperature	150 mW
at 100°C Ambient Temperature	150 mW

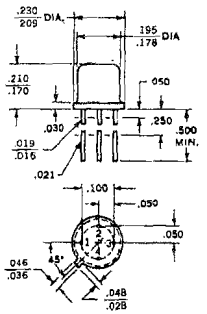
Derate Linearly from 100°C to 150°C at 3 mW/°C

ELECTRICAL CHARACTERISTICS
(T_A = 25°C, unless otherwise specified — body grounded)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BV_{DSX}	Breakdown voltage drain to source	20	—	—	V	V_{GS} = −4V, I_D = 100µA
I_{GSS}	Gate Leakage Current	—	—	0.10	nA	V_{GS} = ±10V
I_D (off)	Drain to Source Leakage Current	—	—	100	µA	V_{DS} = +15V, V_{GS} = −4.0V
I_{DSS}	Zero signal Gate voltage drain current	3.0	—	30	mA	V_{DS} = +15V, V_{GS} = 0V
V_G (off)	Gate-Source Cutoff Voltage	−0.3	−2.0	−4.0	V	V_{DS} = +15V, I_D = 100µA
C_{iss}	Small-signal, short circuit gate No. 1-to-source capacitance	—	3.0	5.0	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{oss}	Small-signal, short circuit drain-to-source	—	2.0	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz
C_{rss}	Small-signal, short circuit reverse transfer capacitance	—	0.32	—	pF	V_{DS} = +15V, I_D = 10mA*, f = 1 MHz
G_{fs}	Forward trans-conductance	8000	10000	—	µmhos	V_{DS} = +15V, I_D = 10mA* f = 1 kHz
G_{ps}	Power gain for measurements circuits	16	18	—	dB	V_{DS} = +15V, V_{GS} = 1.7V, f = 200 MHz, R_S = 270Ω
NF	Noise Figure**	—	2.5	4.0	dB	V_{DS} = +15V, V_{GS} = 1.7V, f = 200 MHz, R_S = 270Ω
$rd_{(on)}$	Drain to Source on resistance	—	200	300	Ω	V_{GS} = 0V I_D = 0.1mA

*V_{GS} is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72 PACKAGE



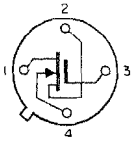
Bottom view

Note: All dimensions in inches.

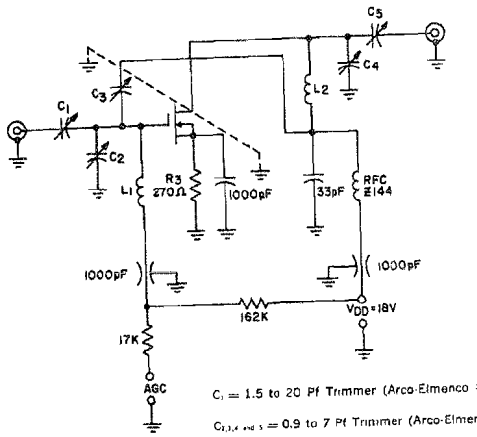
TERMINAL DIAGRAM

LEAD

1. Drain
2. Source
3. Gate
4. Substrate and case



POWER GAIN TEST JIG @ 200MHz FOR MEM 557 WITH NEUTRALIZING



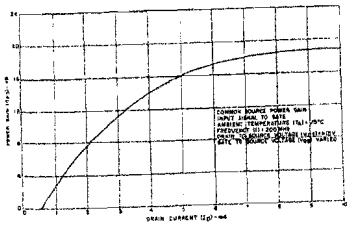
C_1 = 1.5 to 20 Pf Trimmer (Arco-Elmenco #400)

$C_{2,3,4 \text{ and } 5}$ = 0.9 to 7 Pf Trimmer (Arco-Elmenco #402)

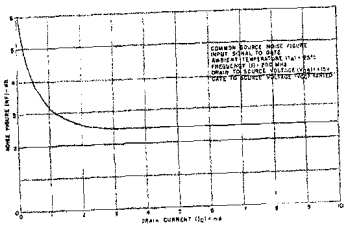
L_1 = 5 Turns #22 Wire 1/8" Dia. & 1/8" Spacing

L_2 = 4 Turns #22 Wire 1/4" Dia. & 1/8" Spacing

POWER GAIN vs DRAIN CURRENT



NOISE FIGURE vs DRAIN CURRENT



MEM 616 MEM 617 MEM 618

N-Channel Depletion Mode Dual-Gate MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain–Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers–Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

DESCRIPTION

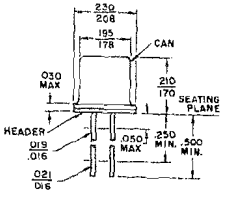
The MEM 616 / MEM 617 / MEM 618 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

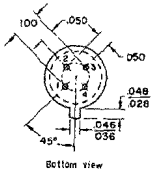
The MEM 616 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

The MEM 617 is intended for use in VHF mixers in television tuners where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

The MEM 618 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.

TO-72

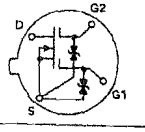




Bottom view

TERMINAL DIAGRAM

1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE/SUBSTRATE



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

DRAIN-SOURCE VOLTAGE, V_{DS}	25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1}	25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2}	25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S}	±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S}	±6V
DRAIN CURRENT I_D	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	360mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

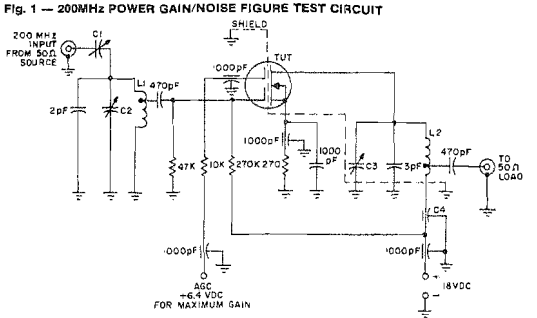
ELECTRICAL CHARACTERISTICS: (T_A = 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 616 MIN	MEM 616 TYP	MEM 616 MAX	MEM 617 MIN	MEM 617 TYP	MEM 617 MAX	MEM 618 MIN	MEM 618 TYP	MEM 618 MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100µA, V_{G1S}=V_{G2S}=−4V	25	–	–	20	–	–	20	–	–	volts
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10µA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	volts
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10µA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	volts
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50µA V_{DS}=15V, V_{G2S}=4V	–	−1.5	–	–	−1.0	–	–	−1.5	–	volts
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50µA, V_{DS}=15V, V_{G1S}=0V	–	–	−4.0	–	–	−4.0	–	–	−4.0	volts
I_{DSS}	Gate 2– Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	5.0[7]	–	30	2.0[7]	–	15	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	.005	.02	.03	–	–	–	.005	.02	.03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	780	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	1.25	–	–	17	–	–	18	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see	–	−55	–	–	–	–	–	−13.6	–	degree
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, notes	–	30	–	–	–	–	–	5.5	–	µmho
θ_{rs}	Angle of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, 4,5,6	–	−30	–	–	–	–	–	90	–	degree
MAG	Maximum Available Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	–	21	–	–	17.3[2]	–	–	39	–	dB
G_{ps}	Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	16	18[1]	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain	V_{DS}=+15V, V_{G2S}=+4V,	–	–	–	–	–	–	–	30[3]	–	dB
N.F.	Noise Figure	V_{DS}=+15V, V_{G2S}=+4V,	–	3.5	4.5	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 616 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 617 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 618 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of I_{DSS}, the following I_{DSS} ranges are available

Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (ohms)	Suggested Biasing (volts)
MEM616 R.F. Amplifier	5-13	Black Dot	150	V_{G1} = +1.5, V_{G2S}= +4.0
	11-22	Blue Dot	180	
	20-30	Red Dot	200	
MEM617 Mixer	2-9	Black Dot	100	V_{G1} = +0.5, V_{G2} = +1.5
	7-15	Blue Dot	100	
MEM618 I.F. Amplifier	3-9	Black Dot	270	V_{G1} = +1.0, V_{G2S}= +4.0
	7-14	Blue Dot	270	
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END

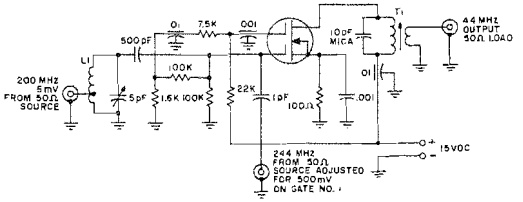
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END

C1 0.4 TO 7pF (ARCO 400)

C2,C3 1.3 TO 5pF VARIABLE.

C4 1000pF BUTTON TYPE CAPACITOR

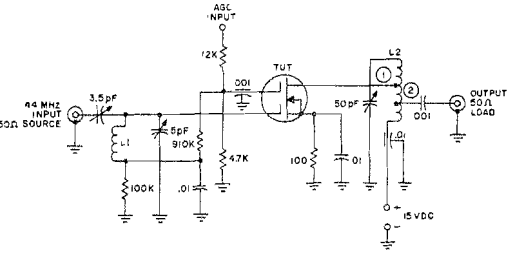
Fig. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END

T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO

Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



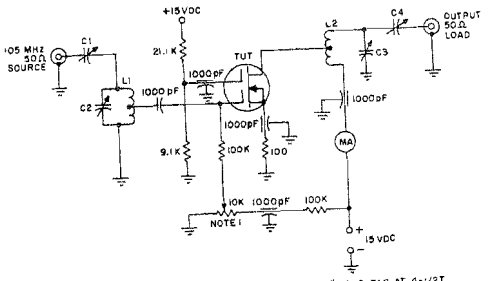
L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM

L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG

(1) DRAIN TAP 2-1/2T FROM COLD END

(2) LOAD TAP 0.4T FROM COLD END

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 4-1/2T C_t =17.8pF R_t =15K AT 100MHz, MOUNTED.

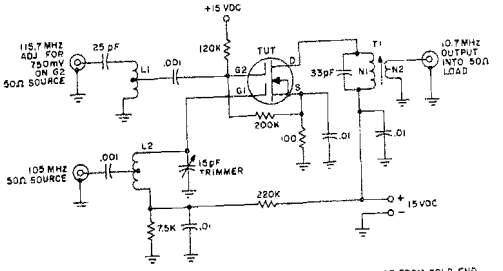
L2 SAME AS L1, BUT R_t =30K MOUNTED

C1,C4 0.9 TO 7.0pF TRIMMER

C2,C3 AIR VARIABLE CAPACITOR 20pF MAX

NOTE1 ADJUST 10K POT FOR 6mA I_D

Fig. 5 — 105MHz to 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END

L2 9T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END

T1 Q_0=67 AT 10.7MHz, N1/N2=17

4C

MEM 636 MEM 637 MEM 638

N-Channel Depletion Mode Dual-Gate MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain–Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers–Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

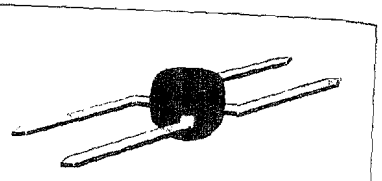
DESCRIPTION

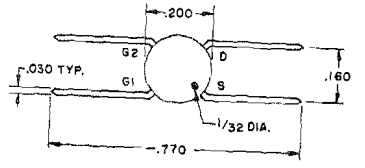
The MEM 636/MEM 637/MEM 638 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor field-effect transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

The MEM 636 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

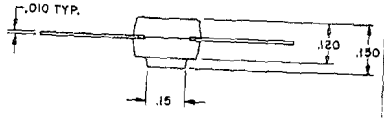
The MEM 637 is intended for use in VHF mixers where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

The MEM 638 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.





TOP VIEW

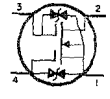


SIDE VIEW

LEADS CAN BE PREFORMED TO CUSTOMER SPECIFICATION

TERMINAL DIAGRAM

1. SOURCE
2. DRAIN
3. GATE 2
4. GATE 1



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

DRAIN-SOURCE VOLTAGE, V_{DS}	25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1}	25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2}	25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S}	±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S}	±6V
DRAIN CURRENT, I_D	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	350mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

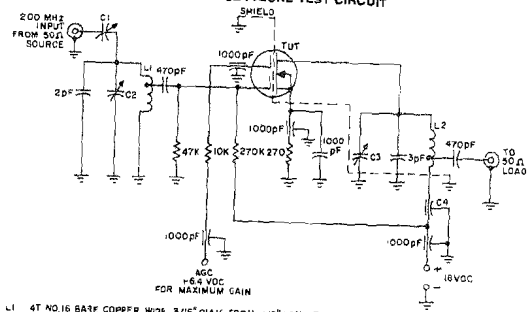
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 636 MIN	MEM 636 TYP	MEM 636 MAX	MEM 637 MIN	MEM 637 TYP	MEM 637 MAX	MEM 638 MIN	MEM 638 TYP	MEM 638 MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100µA, V_{G1S}=V_{G2S}=−4V	20	–	–	20	–	–	20	–	–	V
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10µA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10µA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50µA, V_{DS}=15V, V_{G2S}=4V	–	−1.5	–	–	−1.0	–	–	−1.5	–	V
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50µA, V_{DS}=15V, V_{G1S}=0V	–	–	−4.0	–	–	−4.0	–	–	−4.0	V
I_{DSS}	Gate 2–Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	4.0[7]	–	30	2.0[7]	–	20	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	005	.02	.03	–	–	–	005	.02	03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	780	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=−15V, V_{G2S}=+4V,	–	2.00	–	–	17	–	–	19	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4[8]	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see	–	−95	–	–	–	–	–	−13.6	–	deg
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, notes	–	30	–	–	–	–	–	5.5	–	µmho
θ_{rs}	Angle of Rev Transadmittance	V_{DS}=+15V V_{G2S}=+4V, 4,5,6	–	−30	–	–	–	–	–	90	–	deg
Gc	Conversion Power Gain Fig. 2 200MHz, Fig. 5 105MHz	V_{DS}=+15V, V_{G2S}=+4V,					18					dB
Gps	Power Gain – 200MHz	Fig. 1	19	21	–	–	–	–	–	–	–	dB
Gps	Power Gain – 105MHz	Fig. 4	–	27	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain – 44MHz	Fig. 3		–	–	–	–	–	–	30[3]	–	dB
N.F	Noise Figure – 200MHz	Fig. 1	–	2.5	3.0	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 636 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 637 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 638 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of I_{DSS}, the following I_{DSS} ranges are available
8. Forward conversion transconductance

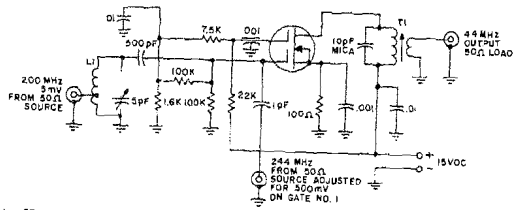
Device	I_{DSS} Range (mA)	Color Code	Suggested Source Resistor (Ω)	Suggested Biasing (V)
MEM 636 R.F. Amplifier	4-13	Yellow Dot	150	V_{G1} = +1.5
	11-22	Blue Dot	180	V_{G2S} = +4.0
	20-30	Red Dot	200	
MEM 637 Mixer	2-8	Yellow Dot	100	V_{G1} = +0.5
	6-12	Blue Dot	100	V_{G2} = +1.5
	10-20	Red Dot		
MEM 638 I.F. Amplifier	3-9	Yellow Dot	270	V_{G1} = −1.0
	7-14	Blue Dot	270	V_{G2S} = +4.0
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



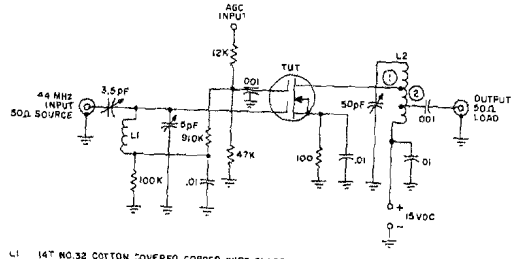
L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END
L2 4T NO.16 1/4" DIAM. FORM, 1/2" LONG TAP AT 3/4T FROM COLD END.
C1 0.4 TO 7pF [ARCO 400]
C2,C3 1.3 TO 5pF VARIABLE
C4 1000pF BUTTON TYPE CAPACITOR

FIG. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



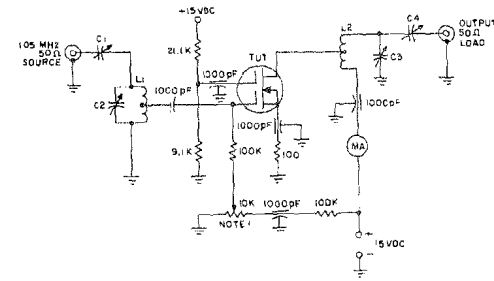
L1 3T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG, TAP AT 3/4T FROM COLD END
T1 PRIMARY 4T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM
SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO

Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



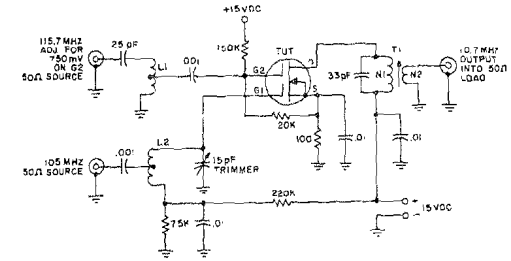
L1 14T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM FORM
L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG
① DRAIN TAP 2-1/2T FROM COLD END
② LOAD TAP 0.4T FROM COLD END.

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 8T NO.18 BARE COPPER WIRE ON 5/16" DIAM CORE, 1/2" LONG TAP AT 4-1/2T
C_t =17.8pF R_t =15K AT 100MHz, MOUNTED
L2 SAME AS L1, BUT R_t =30K MOUNTED
C1,C4 0.9 TO 7.0pF TRIMMER.
C2,C3 AIR VARIABLE CAPACITOR 20pF MAX
NOTE 1. ADJUST 10K POT. FOR 6mA I_D

Fig. 5 — 105MHz TO 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM CORE, 1/2" LONG TAP AT 2T FROM COLD END.
L2 4T NO.18 BARE COPPER WIRE ON 5/16" DIAM CORE, 3/8" LONG TAP AT 1T FROM COLD END.
T1 Q_0=67 AT 10.7MHz, N1/N2=17

4C

N-Channel Depletion Mode MOSFET

FEATURES

- Back-to-Back Zener Clamp to protect gate
- Low 3rd order distortion
- High gain–low noise through VHF range
- Low feedback capacitance 0.32 pF typ.
- Square law response

APPLICATIONS

- TV Tuners
- FM Tuners
- IF Amplifiers
- SSB Amplifiers
- Wideband Amplifiers
- High Frequency Analog Switching

MAXIMUM RATINGS:

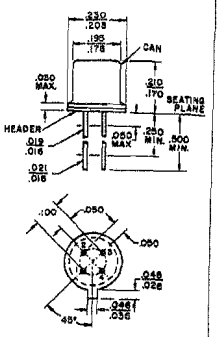
Drain-to-Source voltage ..... +20V
Gate-to-Source voltage ..... ±8.0V
Drain-to-Gate voltage ..... +30 to −6.0V
Drain Current ..... Limited by Dissipation
Storage Temperature ..... −65 to +150°C
Operating Junction Temperature ..... −65 to +150°C
Total Dissipation at 25°C Case Temperature 300mW
Total Dissipation at 25°C Ambient Temperature 225mW
at 100°C Ambient Temperature 150mW
Derate Linearly from 100°C to 150°C at 3 mW/°C

ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Conditions	Min	Typ	Max	Units
BV_{DSX}	Breakdown voltage drain to source	V_{GS} = −4.0V I_D = 100μA	20	–	–	V
BV_{gss}	Breakdown voltage gate to source	V_{DS} = 0V, I_G = 100μA	±6.0	–	–	V
I_{GSS}	Gate Leakage Current	V_{GS} = ±4.0V	–	–	±100	nA
$I_{D(off)}$	Drain to Source Leakage Current	V_{GS} = +15V, V_{GS} = −4.0V	–	–	100	μA
I_{DSS}	Zero signal Gate voltage drain current	V_{DS} = +15V, V_{GS} = 0V	1.0	4.0	20.0	mA
$V_{G(off)}$	Gate-Source Cutoff Voltage	V_{DS} = +15V, I_D = 100μA	–	−1.0	−4.0	V
C_{iss}	Small-signal, short circuit input capacitance	V_{DS} = +15V, I_D = 10mA*, f = 44 MHz	–	4.0	7.0	pF
C_{oss}	Small-signal, short circuit output capacitance	V_{DS} = +15V, I_D = 5mA*, f = 44 MHz	–	2.0	–	pF
C_{rss}	Small-signal, short circuit reverse transfer capacitance	V_{DS} = +15V, I_D = 5mA*, f = 1.0 MHz	–	0.32	–	pF
G_{fs}	Forward transconductance	V_{DS} = +15V, I_D = 5mA*, f = 1.0 kHz	6000	10000	–	μmhos
G_{ps}	Power gain (See Fig. 1 for measurement circuit)	V_{DD} = +18V, f = 100 MHz, R_g = 270Ω	18	22	–	dB
NF	Noise Figure ** (See Fig. 1 for measurement circuit)	V_{DD} = +18V, f = 100 MHz, R_g = 270Ω	–	2.5	4.5	dB
$rd_{s\,(on)}$	Drain to Source on resistance	V_{GS} = +5.0, I_D 0.1mA	–	30	100	Ω

*V_{GS} bias is adjusted for the required current.
**Input circuit adjusted for minimum noise figure.

TO-72



Bottom View

Note: All dimensions in inches.

TERMINAL DIAGRAM

Lead

1. Drain
2. Source
3. Gate
4. Substrate and case

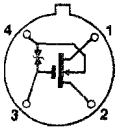
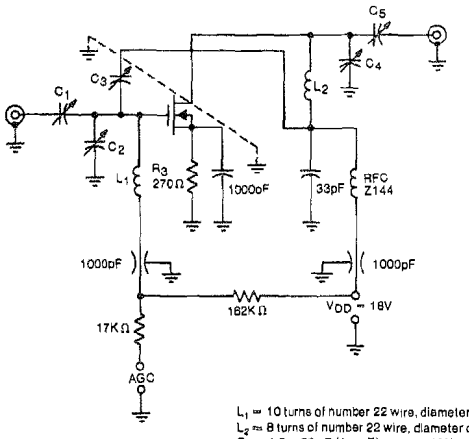


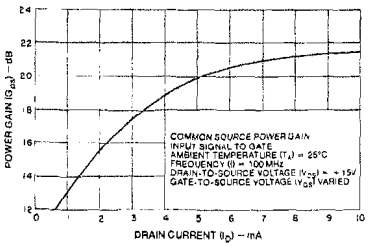
Fig. 1 — POWER GAIN TEST JIG @ 100MHz WITH NEUTRALIZING



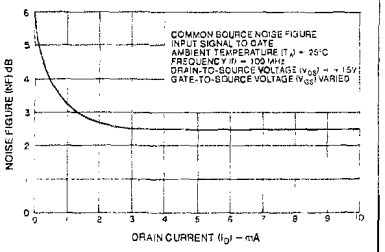
L_1 = 10 turns of number 22 wire, diameter of coil = .125 inch
L_2 = 8 turns of number 22 wire, diameter of coil = .25 inch
C_1 = 1.5 – 20 pF (Arco Elmenco # 400)
C_2 & C_3 = 9 to 7 pF (Arco Elmenco # 402)
C_4 & C_5 = .9 to 7 pF (Arco Elmenco # 402)

TYPICAL CHARACTERISTIC CURVES

POWER GAIN vs. DRAIN CURRENT



NOISE FIGURE vs. DRAIN CURRENT



4C

MEM 670

N-Channel Depletion Mode Silicon MOSFET

FEATURES

- Femtoamp Gate Leakage
- 10^{15} Ohms Input Resistance
- High Transient Gate Voltage Capability
- Narrow I_{DSS} Range
- Low Input Capacitance
- Excellent Stability

APPLICATIONS

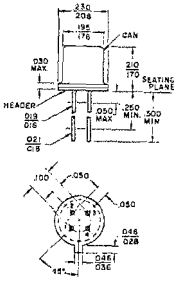
Smoke Detectors
Memory Modules
Electrometers
Alarm Systems

DESCRIPTION

The MEM 670 is an N-channel, Depletion Mode, Metal Oxide Semiconductor Field Effect Transistor. This MOSFET exhibits very low gate leakage, extremely high input resistence, and is capable of handling very high gate to source voltage transients.

These features, combined with an excellent stability, make the MEM 670 ideally suited for smoke detector applications

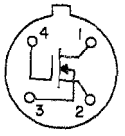
TO-72



BOTTOM VIEW
Note: All dimensions in inches

LEAD CONFIGURATION

1 – DRAIN
2 – SOURCE
3 – SUBSTRATE AND CASE
4 – GATE



MAXIMUM RATINGS (T_A = 25°C)

DRAIN-SOURCE VOLTAGE, V_{DS} 20V
DRAIN-GATE VOLTAGE, V_{GD} 20V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±100V
DRAIN CURRENT, I_D ..... Limited by Dissipation
STORAGE TEMPERATURE RANGE ..... −65°C to +150°C
OPERATING TEMPERATURE RANGE ..... −65°C to +125°C
POWER DISSIPATION (T_C=25°C) ..... 300 mW
POWER DISSIPATION (T_A=25°C) ..... 150 mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(BR)SDX}$	DRAIN-SOURCE BREAKDOWN	V_{GS}=−4V, I_D=10µA, V_{US}=0	20	45	–	volts
$V_{GS(off)}$	GATE-SOURCE CUTOFF VOLTAGE	V_{DS}=+15V, I_D=10µA	−0.3	−2.5	−4.0	volts
$I_{D(off)}$	DRAIN CUTOFF CURRENT	V_{DS}=+15V, V_{GS}=−4V, V_{US}=0	–	0.5	10	nA
I_{GSS}	GATE LEAKAGE CURRENT	V_{GS}=±10V, V_{DS}=V_{US}=0	–	.01	1.0	pA
$\|Y_{fs}\|$	FORWARD TRANSFER ADMITTANCE	V_{DS}=+15V, I_D=2mA, V_{US}=0	–	2000	–	umho
C_{iss}*	INPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	–	2.0	5.0	pF
C_{oss}*	OUTPUT CAPACITANCE	V_{DS}=+15V, I_D=10mA f=1MHz	–	2.0	5.0	pF
C_{rss}*	REVERSE TRANSFER CAPACITANCE	V_{DS}=+15V, I_D=10mA, f=1MHz	–	0.3	–	pF
I_{DSS}	ZERO GATE VOLTAGE DRAIN CURRENT	V_{DS}=+15V, V_{GS}=V_{US}=0				
		COLOR CODE – NONE	0.5	–	2.2	mA
		COLOR CODE – BLACK DOT	1.8	–	5.0	mA

NOTES * V_{GS} ADJUSTED FOR I_D = 10mA

N-Channel Depletion Mode Dual-Gate MOSFETS

FEATURES

- Monolithic Gate-Protection Diodes
- Low Feedback Capacitance
- High Gain—Low Noise at VHF
- Reverse AGC Capability
- Linear Mixers—Low Cross-Modulation Distortion
- Dual-Gate Cascode Operation

APPLICATIONS

TV Tuner RF Amplifiers and Mixers
FM Tuner RF Amplifiers and Mixers
IF Amplifiers
Synchronous Detectors
Wide Band RF Amplifiers

DESCRIPTION

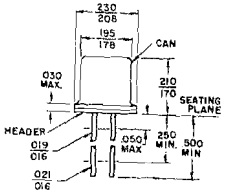
The MEM 680/MEM 681/MEM 682 are N-channel, Depletion-Mode, Dual-Gate Metal Oxide Semiconductor field-effect transistors. They are protected from excessive input voltages by monolithic back-to-back diodes between gates and source.

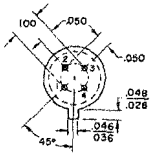
The MEM 680 is intended for use in VHF amplifiers. The low feedback capacitance permits stable high gain without the use of neutralization.

The MEM 681 is intended for use in VHF mixers where minimized cross-modulation, and inter-modulation distortion and low noise operation are required.

The MEM 682 is intended for use in tuned high frequency amplifiers such as TV IF. The low feedback capacitance permits high single stage gain and stability without neutralization.

TO-72

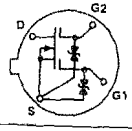




Bottom view

TERMINAL DIAGRAM

1. DRAIN
2. GATE 2
3. GATE 1
4. SOURCE/SUBSTRATE



MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

@T_A=25°C UNLESS OTHERWISE SPECIFIED

DRAIN-SOURCE VOLTAGE, V_{DS}	25V
DRAIN-GATE NO. 1 VOLTAGE, V_{DG1}	25V
DRAIN-GATE NO. 2 VOLTAGE, V_{DG2}	25V
GATE NO. 1–SOURCE VOLTAGE, V_{G1S}	±6V
GATE NO. 2–SOURCE VOLTAGE, V_{G2S}	±6V
DRAIN CURRENT I_D	50mA
TRANSISTOR DISSIPATION, P_T AT 25°C	350mW
ABOVE 25°C, DERATE LINEARLY	2.4mW/°C
LEAD TEMPERATURE DISTANCE 1/32 FROM THE SEATED SURFACE FOR 10 SECONDS	265°C
STORAGE TEMPERATURE RANGE	−65°C to +175°C

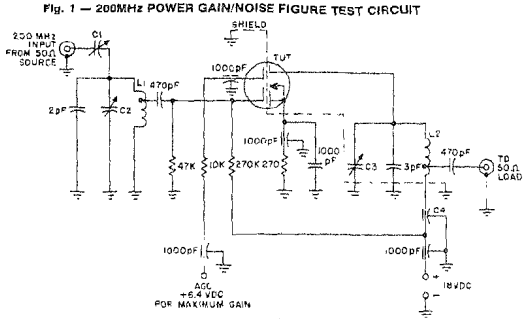
ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTICS	TEST CONDITIONS	MEM 680 MIN	MEM 680 TYP	MEM 680 MAX	MEM 681 MIN	MEM 681 TYP	MEM 681 MAX	MEM 682 MIN	MEM 682 TYP	MEM 682 MAX	UNITS
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=100µA, V_{G1S}=V_{G2S}=−4V	20	–	–	20	–	–	20	–	–	V
BV_{G1SS}	Gate 1–Source Breakdown Voltage	I_{G1S}=10µA, V_{DS}=V_{G2S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
BV_{G2SS}	Gate 2–Source Breakdown Voltage	I_{G2S}=10µA, V_{DS}=V_{G1S}=0V	±6.0	–	–	±6.0	–	–	±6.0	–	–	V
$V_{G1S(off)}$	Gate 1–Source Cutoff Voltage	I_D=50µA, V_{DS}=15V, V_{G2S}=4V	–	−1.5	–	–	−1.0	–	–	−1.5	–	V
$V_{G2S(off)}$	Gate 2–Source Cutoff Voltage	I_D=50µA, V_{DS}=15V, V_{G1S}=0V	–	–	−4.0	–	–	−4.0	–	–	−4.0	V
I_{DSS}	Gate 2–Voltage Drain Current	V_{DS}=15V, V_{G1S}=0V, V_{G2S}=4V	4.0[7]	–	30	2.0[7]	–	20	3.0[7]	–	20	mA
I_{G1SS}	Gate 1–Leakage Current	V_{G1S}=±4V, V_{G2S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
I_{G2SS}	Gate 2–Leakage Current	V_{G2S}=±4V, V_{G1S}=V_{DS}=0V	–	–	50	–	–	50	–	–	50	nA
C_{rss}	Reverse Transfer Capacitance	V_{DS}=+15V, V_{G2S}=+4V, I_D=10mA, f=1.0MHz	.005	.02	.03	–	–		.005	.02	.03	pF
C_{iss}	Input Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	4.0	5.4	6.0	–	6.0	–	–	5.1	–	pF
C_{oss}	Output Capacitance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.2	–	–	2.5	–	–	2.5	–	pF
r_{iss}	Input Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	790	–	–	670	–	–	15k	–	Ω
r_{oss}	Output Resistance	V_{DS}=+15V, V_{G2S}=+4V,	–	2.00	–	–	17	–	–	18	–	kΩ
$\|Y_{fs}\|$	Magnitude of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	12	18	–	–	4.4[8]	–	10	14	–	mmho
θ	Angle of Fwd Transadmittance	V_{DS}=+15V, V_{G2S}=+4V, see notes 4,5,6	–	−55	–	–	–	–	–	−13.6	–	deg
$\|Y_{rs}\|$	Magnitude of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	–	30	–	–	–	–	–	5.5	–	µmho
θ_{rs}	Angle of Rev Transadmittance	V_{DS}=+15V, V_{G2S}=+4V,	–	−30	–	–	–	–	–	90	–	deg
G_c	Conversion Power Gain Fig. 2 200MHz Fig. 5 105MHz	V_{DS}=+15V, V_{G2S}=+4V,	–	–	–	–	18	–	–	–	–	dB
G_{ps}	Power Gain – 200MHz	Fig. 1	19	21	–	–	–	–	–	–	–	dB
G_{ps}	Power Gain – 105MHz	Fig. 4	–	27	–	–	–	–	–	–	–	dB
MUG	Maximum Usable Power Gain – 44MHz	Fig. 3	–	–	–	–	–	–	–	30[3]	–	dB
N.F.	Noise Figure – 200MHz	Fig. 1	–	2.5	3.3	–	–	–	–	–	–	dB

NOTES:
1. See Figure 1.
2. Signal and local oscillator voltages, both are applied on Gate 1 with injection level equal to 500MV RMS (see Figure 2).
3. Unneutralized maximum usable gain for one stage (see Figure 3).
4. MEM 680 (RF AMP) I_D=10mA, f=200MHz.
5. MEM 681 (MIXER) V_{G1S}=0.1V, f=200MHz/44MHz.
6. MEM 682 (IF AMP) I_D=5mA, f=44MHz.
7. In addition to the standard range of IDSS, the following IDSS ranges are available:
8. Forward conversion transconductance.

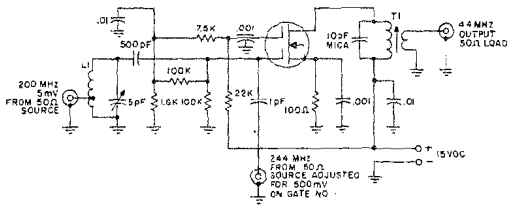
Device	IDSS Range (mA)	Color Code	Suggested Source Resistor (Ω)	Suggested Biasing (V)
MEM 680 R.F. Amplifier	4-13	Yellow Dot	150	V_{G1} = +1.5
	11-22	Blue Dot	180	V_{G2S}= +4.0
	20-30	Red Dot	200	
MEM 681 Mixer	2-8	Yellow Dot	100	V_{G1} = +0.5
	8-12	Blue Dot	100	V_{G2} = +1.5
	10-20	Red Dot		
MEM 682 I.F. Amplifier	3-9	Yellow Dot	270	V_{G1} = +1.0
	7-14	Blue Dot	270	V_{G2S}= +4.0
	12-20	Red Dot	270	

Fig. 1 — 200MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



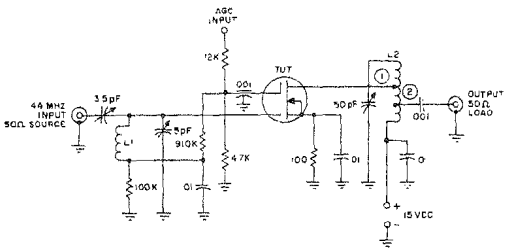
L1 4T NO.16 BARE COPPER WIRE 3/16" DIAM. FORM, 1/2" LONG TAP AT 3T FROM COLD END
L2 4T NO.16 1/4" DIAM FORM, 1/2" LONG TAP AT 3/4T FROM COLD END
C1 0.4 TO 7pF (ARCO 402)
C2,C3 3 TO 5pF VARIABLE
C4 1000pF BUTTON TYPE CAPACITOR

Fig. 2 — 200MHz TO 44MHz MIXER TEST CIRCUIT



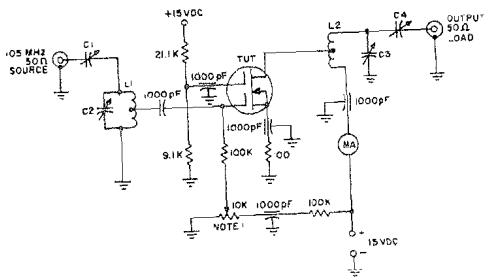
L1 5T NO.16 BARE COPPER WIRE ON 5/16" CORE, 1/2" LONG TAP AT 3/4T FROM COLD END
T1 PRIMARY 10T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" FORM SECONDARY 1T NO.32 ENAMELED COPPER WIRE ADJUSTED FOR 16 TO 1 TURNS RATIO

Fig. 3 — 44MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



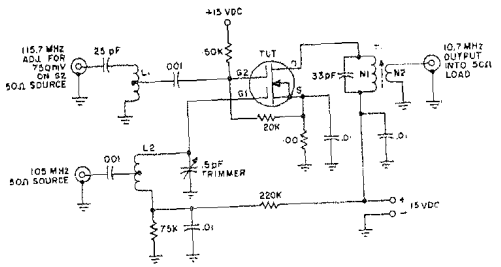
L1 4T NO.32 COTTON COVERED COPPER WIRE CLOSE WOUND ON 1/4" DIAM. FORM
L2 7T NO.16 BARE COPPER WIRE ON 1/2" FORM, 1/2" LONG
(1) DRAIN TAP 2-1/2T FROM COLD END
(2) LOAD TAP 0.4T FROM COLD END

Fig. 4 — 105MHz POWER GAIN/NOISE FIGURE TEST CIRCUIT



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM CORE, 1/2" LONG TAP AT 3-1/2T C_T =17.8pF R_L =15K AT 100MHz, MOUNTED
L2 SAME AS L1, BUT R_L =30K MOUNTED
C1,C4 0.9 TO 7.0pF TRIMMER
C2,C3 AIR VARIABLE CAPACITOR 20pF MAX
NOTE 1. ADJUST 10K POT. FOR 6mA I_D

Fig. 5 — 105MHz TO 10.7MHz CONVERSION GAIN TEST CIRCUIT (PRODUCT MIXER)



L1 6T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 1/2" LONG TAP AT 2T FROM COLD END
L2 4T NO.18 BARE COPPER WIRE ON 5/16" DIAM. CORE, 3/8" LONG TAP AT 1T FROM COLD END
T1 Q_0 =67 AT 10.7MHz, N1/N2=1

MUSIC

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
MASTER FREQUENCY GENERATOR/ TOP OCTAVE GENERATOR	Generates a complete octave of musical frequencies	AY-1-0212	5-3
		AY-1-0212A	5-3
		AY-3-0214	5-6
		AY-3-0215	5-6
		AY-3-0216	5-6
LATCHING NETWORK	Establishes priority level of 13 latch inputs/outputs	AY-1-1313	5-8
RHYTHM GENERATOR	Generates 6 rhythms, drives 8 instruments	AY-5-1315	5-10
CHORD GENERATOR	Produces major, minor, 7th chords, walking bass	AY-5-1317A	5-12
PIANO KEYBOARD	Electronically simulates piano operation and sound	AY-1-1320	5-16
FREQUENCY DIVIDERS	4 stage	AY-1-5051	5-20
	5 stage	AY-1-6721/5	5-20
	6 stage	AY-1-6721/6	5-20
		AY-1-1006	5-22
		AY-1-2006	5-22
	7 stage	AY-1-5050	5-20
		AY-1-1007B	5-24
	2^{16} FL Counter/Divider	AY-9-1000	5-26

5

MUSIC

MICRO ELECTRONICS

Master Frequency Generator/Top Octave Generator

FEATURES

- Wide Input Frequency Range
  1) AY-1-0212—250KHz to 1.5MHz
  2) AY-1-0212A—250KHz to 2.5MHz
- Low Impedance Push-Pull Outputs
- Full Musical Scale in One Chip
- Zener Protected Input

DESCRIPTION

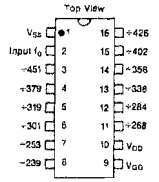
The Master Frequency Generator/Top Octave Generator is a digital tone generator which produces, from a single input frequency, a full octave of twelve frequencies on twelve separate output terminals.

The M.F.G./T.O.G. consists of twelve divider circuits which divide the input by an exact integer to produce a chromatic scale of twelve notes. When used in conjunction with an oscillator and frequency dividers, a system may be configured which generates all the frequencies required by an electronic music synthesizer.

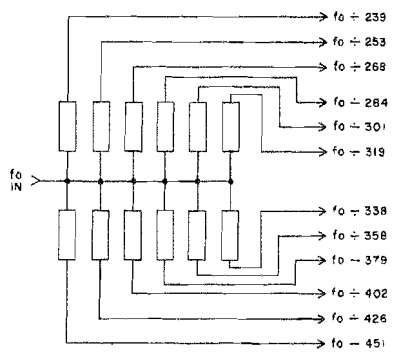
The AY-1-0212 operates with input frequencies of up to 1.5MHz. A premium device designated AY-1-0212A operates up to 2.5MHz

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} .....-30V to +0.3V
Storage Temperature ....-55°C to +150°C
Operating Temperature (T_A) ....0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)
V_{SS} = GND
See Fig.1 for V_{DD} and V_{GG} Operating Voltages

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	10	μA	at 27V
Input Positive Level	+0.3	—	−2.0	Volts	
Input Negative Level	−10.0	—	V_{DD}	Volts	
Output on Impedance to V_{DD}	—	—	3500	Ohms	
Output on Impedance to V_{SS}	—	—	3500	Ohms	See Note 1
I_{GG} Supply Current	—	—	16	mA	
I_{DD} Supply Current	—	—	20	mA	
AC CHARACTERISTICS					
AY-1-0212 Input Frequency f_o	.25	—	1.5	MHz	See Fig.3
AY-1-0212A Input Frequency f_o	.25	—	2.5	MHz	
Input Capacitance	—	5	10	pF	1 MHz
Input Positive Level Width t_p	33	—	—	μs	AY-1-0212
Input Negative Level Width t_n	33	—	—	μs	AY-1-0212
Input Positive Level Width t_p	.2	—	—	μs	AY-1-0212A
Input Negative Level Width t_n	.2	—	—	μs	AY-1-0212A
Output Rise Time t_r	—	1	—	μs	no load
Output Fall Time t_f	—	1	—	μs	no load

** Typical values are at +25°C and nominal voltages

NOTE:
1 Output impedance measurements are made with 1.0V across the device to be measured with 17K Ohm load to −6V.

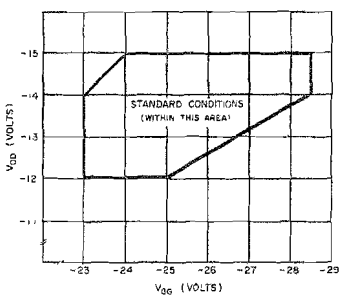


Fig.1 OPERATING VOLTAGES

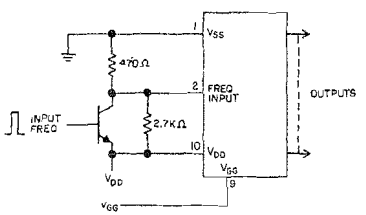


Fig.2 TYPICAL INPUT BUFFER (IF REQUIRED)

TYPICAL CHARACTERISTIC CURVE

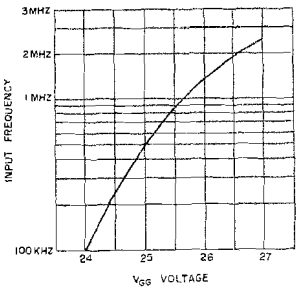
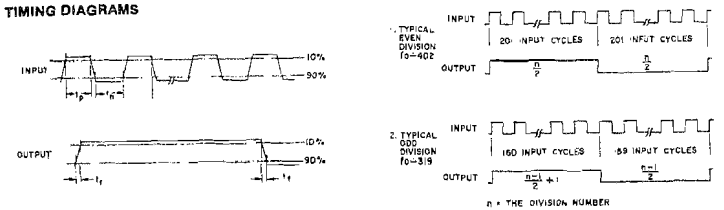
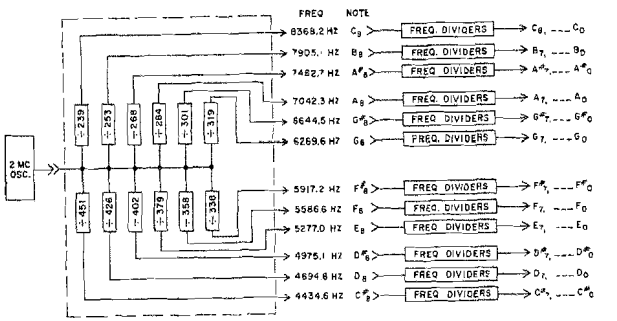


Fig.3 · TYPICAL FREQUENCY VS. V_{GG} VOLTAGE OPERATION

TIMING DIAGRAMS



TYPICAL APPLICATION



AY-3-0214
AY-3-0215
AY-3-0216

Master Frequency Generator/Top Octave Generator

FEATURES

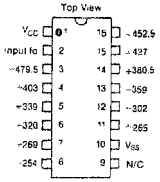
- Wide input frequency range 100 KHz to 4.5 MHz
- Single power supply
- Full musical scale on one chip
- Low impedance push-pull outputs
- Zener protected input.
- AY-3-0214 12 outputs — 50% Duty Cycle (Highest accuracy)
- AY-3-0215 13 outputs — 50% Duty Cycle
- AY-3-0216 13 outputs — 30% Duty Cycle

DESCRIPTION

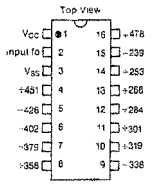
The General Instrument M.F.G./T.O.G. is a digital tone generator which produces, from a single input frequency, 12 or 13 semitone outputs fully spanning the equal tempered scale. When used in conjunction with an oscillator and frequency dividers such as the G.I. AY-1-1007B, a system maybe configured which generates all the frequencies required by an electronic music synthesizer.

PIN CONFIGURATION

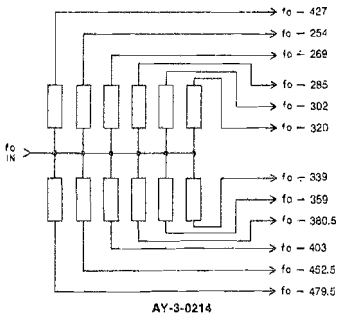
16 LEAD DUAL IN LINE
AY-3-0214



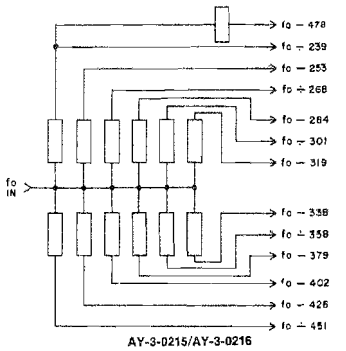
16 LEAD DUAL IN LINE
AY-3-0215/AY-3-0216



BLOCK DIAGRAMS



AY-3-0214



AY-3-0215/AY-3-0216

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3
Storage Temperature ..... -55°C to -150°C
Operating Temperature (T_A) ..... 0°C to +50°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$0°C \leq TA \leq 50°C$
$V_{SS} = 0.0V$
$V_{CC} = +10V$ to $+16V$

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Low	0.0	—	0.8	V	
High	V_{CC} -3.0	V_{CC}	V_{CC}	V	
Frequency	100	—	4500	KHz	
Rise Time	—	—	30	ns	4.5 MHz
Fall Time	—	—	30	ns	4.5 MHz
Duty Cycle	40	50	60	%	
Capacitance	—	—	10	pF	
Outputs					
High	V_{CC} -1.5	—	V_{CC}	V	0.25 mA
Low	0.0	—	0.5	V	0.7 mA
Fall Time	—	—	2.5	µs	20K & 500 pF to 16V
Rise Time	—	—	2.5	µs	20K & 500 pF to V_{SS} when V_{CC} =16V
Duty Cycle	—	50	—	%	AY-3-0214/5
	—	30	—	%	AY-3-0216
Supply current	—	—	120	mA	16V, 4.5 MHz. 25° C

**Typical values are at +25° C and nominal voltages

TIMING DIAGRAMS

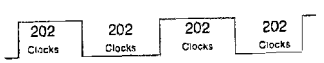


Fig.1 TYPICAL EVEN DIVISOR N = 404

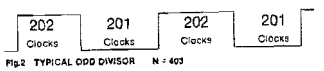


Fig.2 TYPICAL ODD DIVISOR N = 403

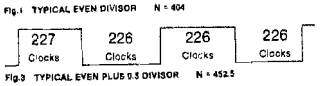


Fig.3 TYPICAL EVEN PLUS 0.5 DIVISOR N = 452.5

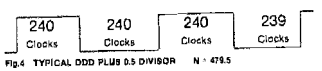
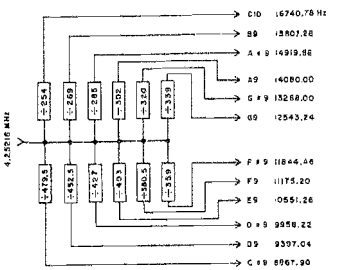
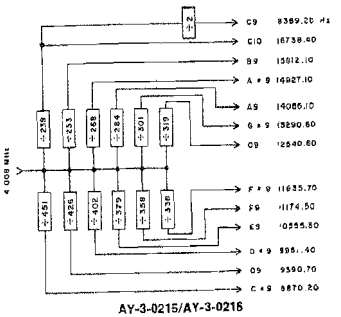


Fig.4 TYPICAL ODD PLUS 0.5 DIVISOR N = 479.5

TYPICAL APPLICATIONS



AY-3-0214



AY-3-0215/AY-3-0216

5

Priority Latching Network

FEATURES

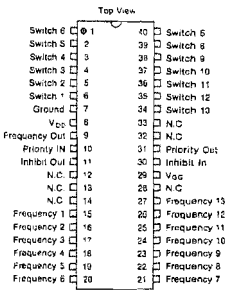
- Low Power Consumption
- Two or more units may be connected in tandem

DESCRIPTION

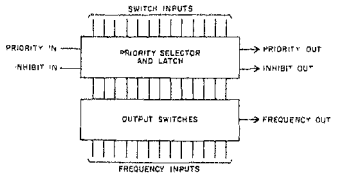
The AY-1-1313 Priority Latching Network is a LSI subsystem designed for use in electronic organ keyboard and pedal latching circuits. When any combination of one or more "switch" inputs is connected to logic "1" the output switch corresponding to the highest priority, or lowest number, input will close, connecting the selected frequency to the output frequency bus. The output switch will remain closed even if the input switch is released, and will remain closed until a new input switch closure occurs.

PIN CONFIGURATION

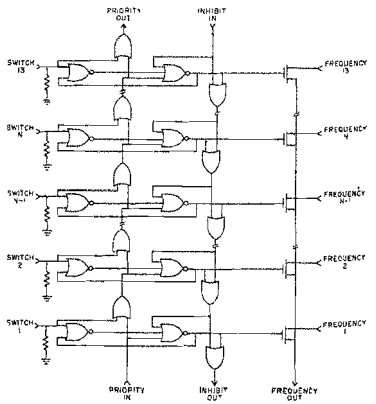
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} ..... -30V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature (T_A) ..... -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

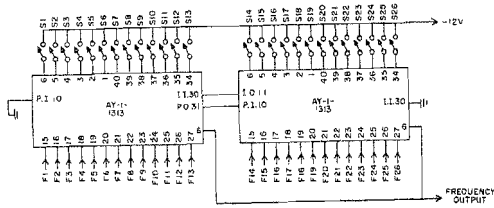
Standard Conditions (unless otherwise noted)

V_{DD} = -12±1V
V_{GG} = -27±1.5V
V_{SS} = GND

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Switch Inputs Impedance	15	—	80	KΩ	Measured to Ground
Priority and Inhibit Inputs Impedance	1	—	—	MΩ	Measured to Ground
Input Logic "0"	—	—	-2	Volts	
Input Logic "1"	-9	—	—	Volts	
Output Logic "0"	—	—	-2	Volts	R_L = 47K to V_{DD}
Output Logic "1"	-9	—	—	Volts	R_L = 47K to V_{DD}
Frequency Output Switch					
Impedance — "ON"	—	—	20	KΩ	
"OFF"	5	—	—	MΩ	
I_{DD} Supply Current	—	—	8	mA	
I_{GG} Supply Current	—	—	1	mA	

**Typical values are at +25°C and nominal voltages.

TYPICAL APPLICATION



For multiple unit operation, the Priority Output of the higher priority unit is connected to the Priority Input of the lower, and the Inhibit Input of the higher priority unit is connected to the Inhibit Output of the lower. The Priority and Inhibit Inputs must be grounded when not in use.

5

Rhythm Generator

FEATURES

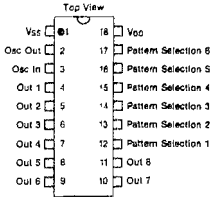
- Drives 8 instruments
- 32 beat long pattern
- 6 rhythm selections
- Internal oscillator
- Mask programmable rhythm pattern and pattern length
- Automatic reset for easy chord coupling

DESCRIPTION

The AY-5-1315 is a P-Channel MOS IC specifically designed for the Rhythm and Percussion section of an Electronic Organ and for Automatic Rhythmers. It contains all the logic circuits necessary to generate six sets of rhythm patterns driving eight instruments. The automatic reset feature allows it, when coupled with the chord section of the organ, to start on the downbeat every time a new chord is played. Selecting multiple patterns will result in a combination of the patterns selected. Tempo is externally adjustable from slower than largo to faster than presto. For added stability of the internal tempo oscillator a ÷ 32 circuit is provided. If an external tempo oscillator is used this circuit could be mask programmed out of the counter decoder chain. For added flexibility the output buffers could be mask programmed for either 100% or 50% duty cycle. The AY-5-1315 may be operated alone or in conjunction with the AY-5-1317A chord generator

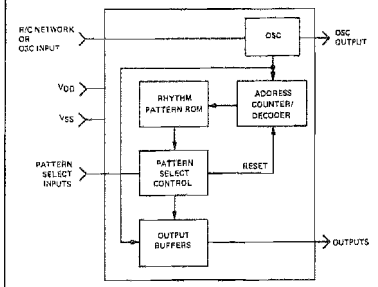
PIN CONFIGURATION

18 LEAD DUAL IN LINE

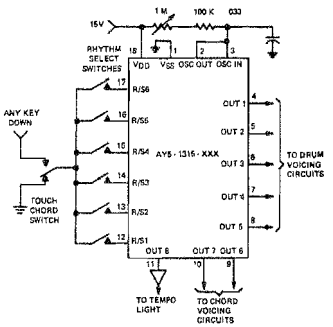


A separate publication, "AY-5-1315 Custom Coding Information", available from GI Sales Offices, describes the punched card and truth table format for custom programming of the AY-5-1315 memory.

BLOCK DIAGRAM



TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} . . . . . -20V to -0.3V
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature (T_A) . . . . . -25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)
V_{SS} = 0 Volts V_{DD} = -12 to -18 V

Characteristic	Min	Typ**	Max	Units	Conditions
Clock input					
Freq.	DC	100/1000	100K	Hz	with ÷32 circuit in
	DC	3/300	100K	Hz	with no ÷32 circuit
Logic '0'	V_{DD}-4.0	—	V_{DD}	V	
Logic '1'	-0.3	—	-1.0	V	
Internal osc. freq.	—	100/1000	—	Hz	Set by external resistor & capacitor
Rhythm select inputs Logic '0'	V_{DD}-.4	—	V_{DD}	V	
Rhythm select inputs Logic '1'	-0.3	—	-1.0	V	
Rhythm select input Impedance	10	—	—	KOhm	Pulled to V_{DD}
Instrument & osc. output Logic '0' (Note 1)	V_{DD}-6.0	—	V_{DD}-4.0	V	with internal pull ups to V_{DD} (instrument outputs only) supplying 0.1 mA
Instrument & osc. output Logic '1'	—	—	-1.0	V	Sinking 1.0 mA
Power	—	—	300	mW	V_{DD} = 15 volts

**Typical values are at +25°C and nominal voltages.

NOTE 1. Open ended devices have a minimum impedance of 500K ohm to GND when in the off condition.

OPERATION

The AY-5-1315 Rhythm Generator contains an internal oscillator, a clock generator circuit, a 5-bit synchronous resetable counter/decoder, and a ROM that drives 8 instruments and the reset circuit. By selecting one of the 6 available rhythm patterns the appropriate section of the ROM is enabled.

If no pattern is selected the reset circuit is activated which stops the internal oscillator, inhibits the output drivers and resets the counter to count 1. When a selection is made, the outputs are enabled which brings out the program as stored in count 1- the down beat program.

The oscillator frequency determines the tempo of the rhythm pattern generated. The clock generator generates a 2 phase clock $\phi 1$ and $\phi 2$. If the internal divide by 32 option is selected $\phi 1$ is on for the first 16 count and $\phi 2$ is on between count 17 and 32, thus producing two non overlaping clocks. If the divide by 32 circuit is programmed out, the circuit $\phi 1$ and $\phi 2$ will be directly related to the ON (logic 1) and OFF (logic 0) time at the clock generator input as provided by an external oscillator. The $\phi 2$ clock drives the 5 bit counter/decoder which sequentially turns on one of the 32 lines of the ROM.

On the $\phi 1$ clock, the program out of the ROM is transferred to the output thus eliminating decoding spikes at the output. If the output of the ROM is a '1' the proper instrument will be turned on. The output drivers are programmed either for 100% duty cycle or 50% duty cycle. When programmed for 100% duty cycle the output turned on will remain on for an entire $\phi 1/\phi 2$ cycle. If the next bit in the program is a '1' again, the output will remain on for the next cycle without going to zero between cycles. When programmed for 50% duty cycle the output will be on during $\phi 1$ only and return to zero during $\phi 2$.

5

Chord Generator

FEATURES

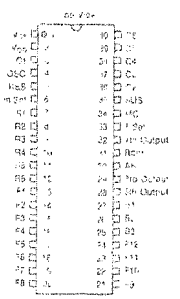
- ROOT, 3rd, 5th, 7th Chord Elements
- Additional output for special effects
- Sustain capability
- Top key priority
- Self-contained oscillator circuit
- Operated with single pole, single throw switch matrix

DESCRIPTION

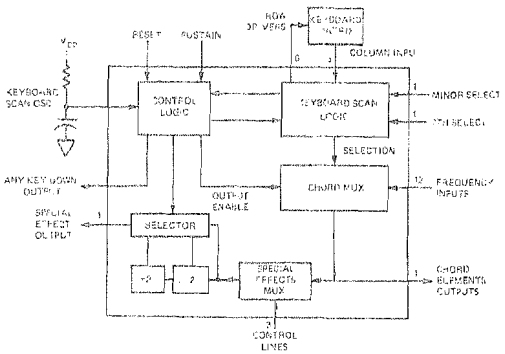
The AY-5-1317A is a P-Channel MOS IC which accepts twelve basic frequencies (one full octave) and outputs the notes necessary to form Major, Minor and Seventh chords. This is the only known standard chord generator IC that performs these functions. The chord elements (ROOT, 3rd, 4th, 5th, 6th, and 7th) can be multiplexed internally to perform special effects such as walking bass, rhythm arpegio alternating bass etc. The AY-5-1317A will operate in conjunction with and, through the KEY DOWN output, synchronize a rhythm generator such as the General Instrument AY-5-1315. The AY-5-1317A has a keyboard priority system with the C Major chord having the highest priority.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	Ground (Vss)	Ground
2	Power Supply (V_{GG})	Negative Supply
3, 36-40	Column Inputs (C1-C6)	Column inputs from Keyboard Matrix
4	Oscillator Input (OSC)	R/C network connection for keyboard scan oscillator
5	Reset (RES)	A logic 1 (+ ground) will reset the keyboard scanner, and the memorized key
6	Minor Select (m Sel)	A Ground on this line changes the 3rd output from Major to Minor
7-12	Row Outputs (R1-R6)	Row outputs to Keyboard Matrix
13-24	Frequency Inputs (F1-F12)	These are the input lines for the 12 frequencies (one full octave B thru C) used to generate the chords
25-27	Control Inputs (B3-B1)	These 3 lines will be internally latched and decoded to select either the ROOT, 3rd, 4th, 5th, 6th, or 7th frequency as the special effect output B1 B2 B3 Selection F 0 0 No change from last selection 0 0 1 ROOT 0 1 0 5th 0 1 1 3rd 1 0 1 7th 1 1 0 4th 1 0 0 6th
28	5th Output (5th)	This line will output the 5th frequency element of the selected chord
29	3rd Output (3rd)	This line will output the 3rd frequency element of the selected chord. Minor 3rd will be provided if a Minor chord is selected. Major 3rd will be provided if a Major or 7th chord are selected.
30	Any Key Down (AK)	This line goes to a logic "1" whenever a chord selection key is depressed
31	Root Output (Root)	This line will output the ROOT frequency element of the selected chord
32	7th Output (7th)	This line will output the 7th frequency element of the selected chord if a 7th chord is selected otherwise the output is logic "0" (Voltage)
33	7th Select (7 Sel)	A ground on this line turns the 7th output on
34	Special Effect Output (MO)	This line will output one of the six frequency elements as programmed by the control lines B1-B3. The 7th chord element frequency will be provided independently of the chord selection
35	Sustain (SUS)	A logic 1 on this line will activate the memory circuit which memorizes the last key played

TRUTH TABLE FOR SPECIAL EFFECT OUTPUT

Chord Selection	Root	3rd Minor	3rd Major	4th	5th	6th	7th
C	C (÷2)	D# (÷2)	E (÷2)	F (÷2)	G (÷2)	A (÷2)	A# (÷2)
C#	C# (÷2)	E (÷2)	F (÷2)	F# (÷2)	G# (÷2)	A# (÷2)	B (÷2)
D	D (÷2)	F (÷2)	F# (÷2)	G (÷2)	A (÷2)	B (÷2)	C (÷1)
D#	D# (÷2)	F# (÷2)	G (÷2)	G# (÷2)	A# (÷2)	C (÷1)	C# (÷1)
E	F (÷2)	G (÷2)	G# (÷2)	A (÷2)	B (÷2)	C# (÷1)	D (÷1)
F	F (÷2)	G# (÷2)	A (÷2)	A# (÷2)	C (÷1)	D (÷1)	D# (÷1)
F#	F# (÷4)	A (÷4)	A# (÷4)	B (÷4)	C# (÷2)	D# (÷2)	E (÷2)
G	G (÷4)	A# (÷4)	B (÷4)	C (÷2)	D (÷2)	E (÷2)	F (÷2)
G#	G# (÷4)	B (÷4)	C (÷2)	C# (÷2)	D# (÷2)	F (÷2)	F# (÷2)
A	A (÷4)	C (÷2)	C# (÷2)	D (÷2)	E (÷2)	F# (÷2)	G (÷2)
A#	A# (÷4)	C# (÷2)	D (÷2)	D# (÷2)	F (÷2)	G (÷2)	G# (÷2)
B	B (÷4)	D (÷2)	D# (÷2)	E (÷2)	F# (÷2)	G# (÷2)	A (÷2)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} with respect to V_{SS}	−20V to +0.3V
Logic Input Voltages with respect to V_{SS}	−20V to +0.3V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

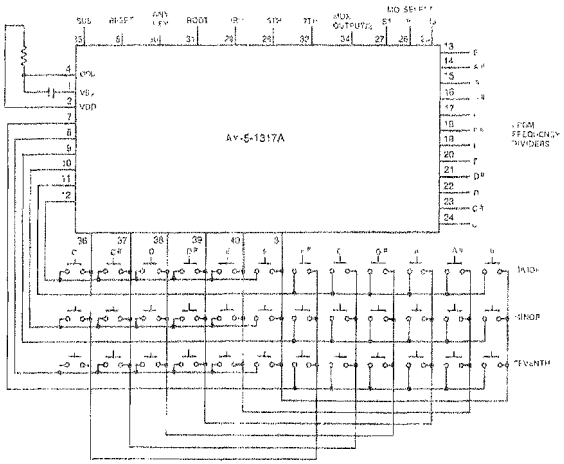
Standard Conditions (unless otherwise noted)

V_{DD} = −15V ±3V
V_{SS} = 0V (substrate voltage)
Operating Temperature (T_A) = +25°C

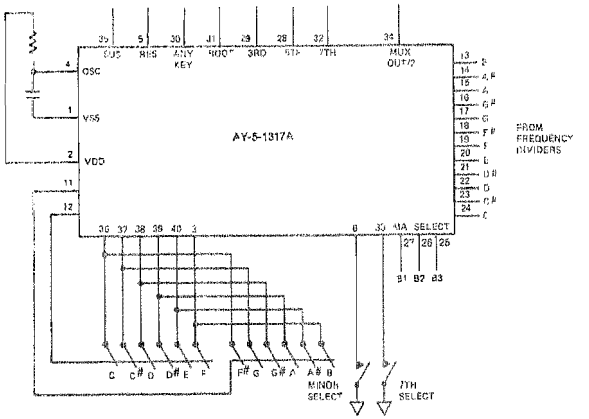
Characteristic	Sym	Min	Typ**	Max	Conditions
Input Logic Levels					
Logic 0	VIL	V_{DD}	—	−8.5	
Logic 1	VIH	1.0V	—	−0.3V	
Input Capacitance	CIN	—	—	10 pF	
Note Outputs					
Logic 0	R_{OL}	160KΩ	—	—	
Logic 1	R_{OH}	—	—	500Ω	
Row Drivers Output Impedance		—	750Ω	—	V_{DD} = −15V
Control Input		10KΩ	—	1000K Ω	
Keyboard Row Input Impedance		24KΩ	—	00KΩ	
Keyboard Scan Frequency		—	25KHz	—	500 pF 750K, V_{DD} = −15V

**Typical values are at +25°C and nominal voltages

STANDARD INTERCONNECTION FOR A 3×12 KEY MATRIX



STANDARD INTERCONNECTION FOR A SINGLE ROW KEYBOARD WITH SEPARATE KEY FOR MINOR AND SEVENTH



Piano Keyboard Circuit

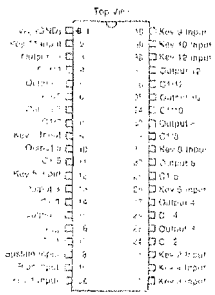
FEATURES

- 12 keys per package
- Loudness proportional to key press velocity
- Sustain input to give loud pedal operation

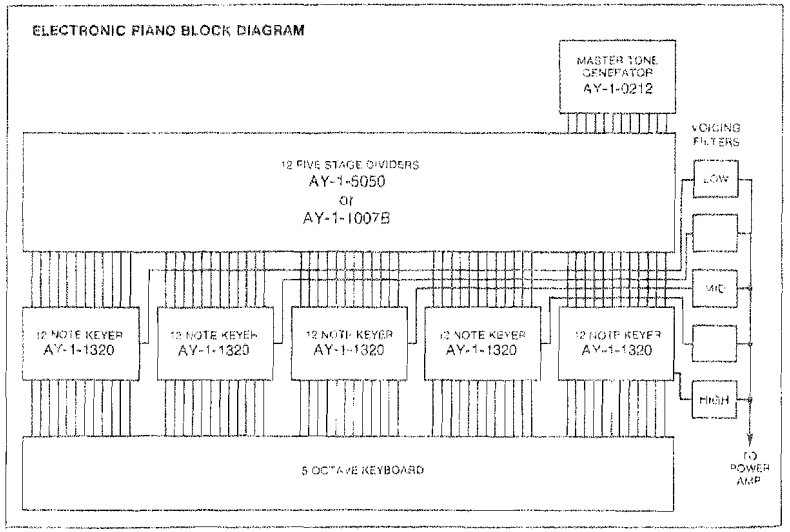
DESCRIPTION

The electronic piano chip when used in conjunction with standard divider circuits will make an instrument closely resembling a piano in operation and sound. The chip is arranged so that the loudness of the notes is proportional to the velocity of the keys as in an acoustical instrument. Additionally the notes are arranged to die away at a realistic rate. A sustain input is provided so that the operation of the loud pedal can be emulated

PIN CONFIGURATION
40 LEAD DUAL IN LINE



ELECTRONIC PIANO BLOCK DIAGRAM



PIN FUNCTIONS

Name	Function
V_{SS}	Positive supply
V_{GG}	Negative supply (-25 to -29V)
$V_{BIAS\ 1}$	Bias supply to keying circuit (-27V nominal)
Sustain	When a logic '1' the outputs are damped with a time constant of 180msec when the key is released. This input simulates the action of the loud pedal in a piano
Key inputs (1-12)	These inputs are switched from logic '0' to logic '1' by a break before make change over switch. During the transit the input is held at an intermediate logic level. The transit time determines the initial output level
C1 (1-12)	The capacitor C1 connected to this pin establishes the key velocity time constant. 0.5μF gives a time constant of 18msec
Output (1-12)	This output provides an exponentially decaying DC level proportional to the amplitude of the desired note. The capacitor C2 determines the damper time constant. The resistor R1 together with C2 determines the undamped decay time constant. The DC level is chopped by external frequency dividers to generate the note

OPERATION

In the rest condition with the key up capacitor C1 is charged to -12 volts. When the key is depressed C1 is first disconnected and it starts to discharge through the 39KOhm resistor with a time constant of 18msec. At the end of the key travel the final voltage on C1 is transferred to the gate of T3 via T2. This causes C2 to be charged to V_{CC} + 4 Volts. The faster the key depression the larger the initial voltage on C2 and the louder the note.

The DC voltage on C2 is chopped via R1 and the divider circuit and the resulting square wave is fed to the voicing circuits and amplifiers. C2 slowly discharges through R1 to give the required exponential decay of note amplitude. When the key is released the 50K damping resistor is optionally connected across C2 to damp the notes with a 110msec time constant.

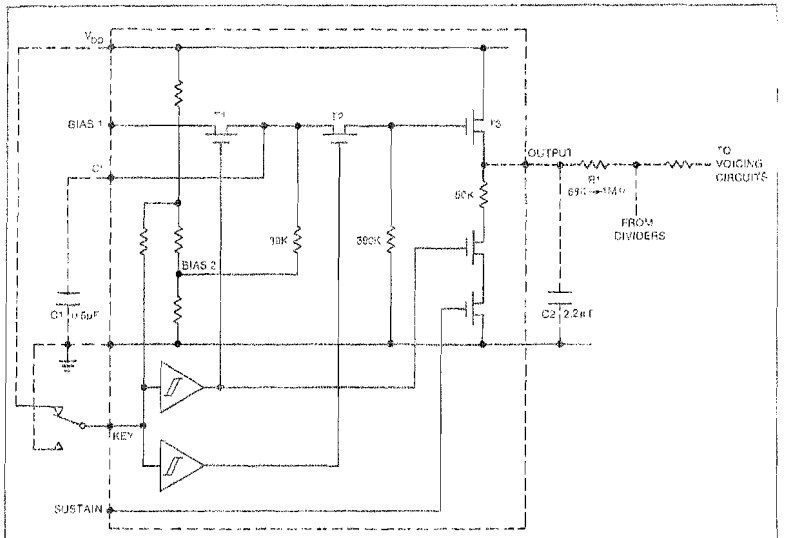


Fig.1 KEY CIRCUIT SCHEMATIC

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin ..... +0.3 to -30 Volts
Storage Temperature Range ..... -65°C to +150°C
Ambient Operating Temperature Range ..... 0°C to +70°C

*Exceeding these ranges could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{GG} = -25 to -29 Volts
V_{SS} = 0V
$V_{BIAS\ 1}$ = V_{GG}
Operating Temperature (T_A) = 0°C to +70°C

Characteristics		Min.	Typ**	Max	Units	Conditions
Key Input Logic '1'		+24	---	-28	Volts	Key up
Key Input Logic '0'		+0.3	---	+1	Volts	Key down
Key velocity time constant		---	18	---	ms	C1 = 0.5μF (Note 1)
Output peak amplitude		---	8	---	Volts p-p	(Note 2)
Output decay time constant		---	286-2486	---	ms	See Table 1
Damper time constant		---	110	---	ms	C2 = 2.2μF
Dynamic range		---	30	---	dB	
Power Supply Current	I_{GG}	---	4	---	mA	
	I_{BIAS}	---	3	---	mA	

**Typical values are at +25°C and nominal voltages

Note 1. The key transit time determines the initial amplitude of the note. The longer the time the softer the note. If the transit time is 18ms the amplitude will be approximately 37% of maximum. Capacitor C1 determines the time constant.

Note 2. This is the amplitude that would be obtained if the key transit time was zero.

Table 1 — TYPICAL COMPONENT VALUES/DECAY TIME
C2 = 2.2 μF Square wave chopper

Octave	R1 KOhm	R2 KOhm	Decay Time msec.
C7-C6# 2093-1108Hz	68	470	286
C6-C5# 1046.4-554.2Hz	120	470	484
C5-C4# 523.2-277.1Hz	220	470	825
C4-C3# 261.6-138.6Hz	330	470	1155
C3-C2# 130.8-69.3Hz	680	470	1960
C2-C1# 65.4-43.6Hz	1000	470	2486

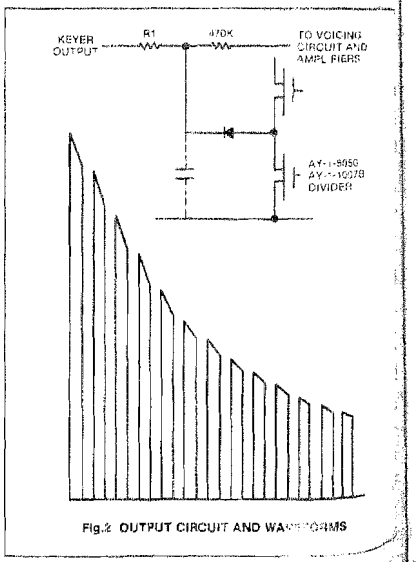


Fig.2 OUTPUT CIRCUIT AND WAVEFORMS

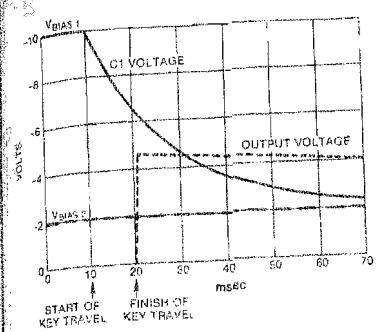


Fig.3 KEY VELOCITY WAVEFORMS

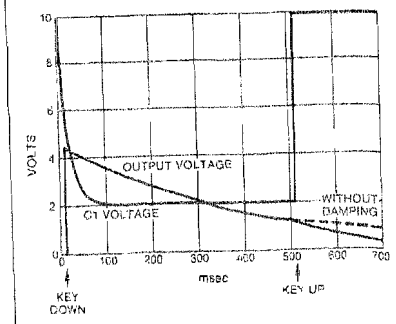


Fig.4 OUTPUT ENVELOPE DECAY WAVEFORM

4-5-6-7 Stage Frequency Dividers

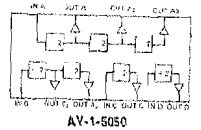
FEATURES

- DC to 1 MHz operating frequency range.
- Diode protection on all inputs
- Low output impedance in both states.
- Choice of configurations:
  1) AY-1-5050 7-Stage Frequency Divider, 3+2+1+1
  2) AY-1-5051 4-Stage Frequency Divider, 2+1+1
  3) AY-1-6721/5. 5-Stage Frequency Divider, 3+2
  4) AY-1-6721/6. 6-Stage Frequency Divider, 3+2+1

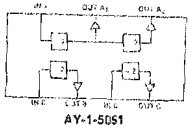
DESCRIPTION

The AY-1-5050, AY-1-5051, AY-1-6721/5 and the AY-1-6721/6 are constructed on monolithic silicon chips using MTOS (Metal-Thick-Oxide-Silicon) P-Channel Enhancement Mode Field Effect Transistors. All circuits can be driven from a sine or square wave input. The different types all have the same specifications and are fully compatible with one another.

BLOCK DIAGRAMS



AY-1-5050



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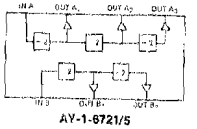

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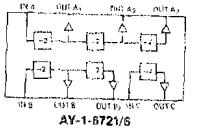
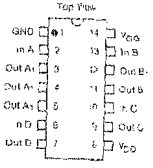


AY-1-6721/6

PIN CONFIGURATIONS

14 LEAD DUAL IN LINE
AY-1-5050



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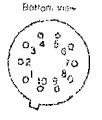
AY-1-5051



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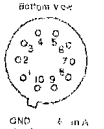
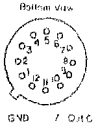
AY-1-6721/5



12 LEAD
AY-1-6721/6



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Drain Voltage	−30V to +0.3V
Gate Voltage	−30V to +0.3V
Data Input Voltage	30V to +0.3V
Storage Temperature	−55° C to +150° C
Operating Temperature (T_A)	0° C to +70° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

Standard Conditions (unless otherwise noted)

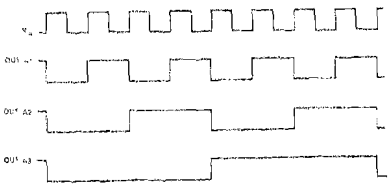
V_{DD} = −13V ±1V
V_{GG} = −27V ±1V
R_L = 1M Ohm
C_L = 10 pF
Operating Temperature (T_A) = +25° C

Characteristics	Min.	Typ**	Max	Units	Conditions
Data Input					
Logic "0" level	—	—	−2	V	
Logic "1" level	−10	—	—	V	
Data input operating freq	DC	—	1	MHz	Sine or square wave
Data input Pulse width					
— "0" level	300	—	—	ns	
— "1" level	300	—	—	ns	
Input Leakage	—	—	5	µA	V_{in} = −20VDC
Output Parameters					
Logic "0" level	—	—	−1	V	
Logic "1" level	−11	—	—	V	
Drive Capability					
— "0" level	—	−1	−1.5	V	Sinking current = 0.5 mA
— "1" level	−11	—	—	V	R_L = 100 KΩ
— "1" level	−8	—	—	V	R_L = 10 KΩ
Data output Rise and Fall time	—	0.6	—	µs	
Current Drain					
I_{GG}	—	3	—	mA	V_{GG} = −27 V
I_{DD}	—	***	—		

**Typical values are at +25° C and nominal voltages

*** V_{DD} is only used for the push-pull outputs therefore I_{DD} is equal to the sum of load currents. This separate V_{DD} enables tremulant to be introduced in the electronic organ application.

TIMING DIAGRAM



Six Stage Frequency Dividers

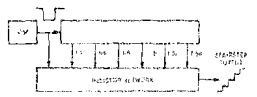
FEATURES

- Sine or Square Wave Input
- Low Impedance Push-Pull Outputs
- Six Divider Stages
  3-2-1 (AY-1-1006)
  2-2-1-1 (AY-1-2006)

DESCRIPTION

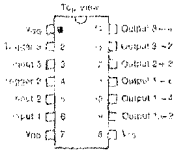
The AY-1-1006 and AY-1-2006 are monolithic frequency divider circuits which utilize MOS technology. Each consists of six flip-flops arranged either 3-2-1 (AY-1-1006) or 2-2-1-1 (AY-1-2006) and diffused into a single silicon substrate. Each circuit can be driven from a sine or square wave input. Each output is a low impedance push-pull output which is capable of driving external circuitry as well as other flip-flops.

APPLICATION



PIN CONFIGURATIONS

14 LEAD DUAL IN LINE
AY-1-1006



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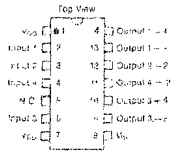
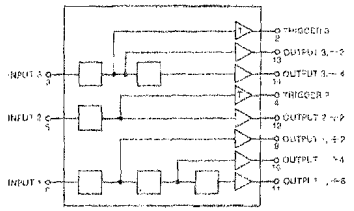
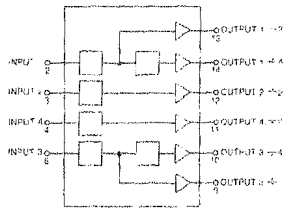
AY-1-2006



BLOCK DIAGRAMS



AY-1-1006



AY-1-2006

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} ..... -30V to +0.3V
Storage Temperature ..... -65°C to +150°C
Operating Temperature (T_A) ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$-14 < V_{DD} < +0.3V$ $V_{GG} = -27 \pm 2V$ $V_{SS} = GND$

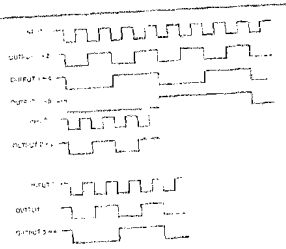
Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	1	μA	$V_{IN} = -20V$
Input Positive Level	—	—	-2.0	Volts	
Input Negative Level	8.0	—	—	Volts	
Output Positive Level	—	—	-1.0	Volts	$V_{GG} = -27V$, $V_{DD} = +12V$
Output Negative Level	-10.0	—	—	Volts	$V_{GG} = -27V$, $V_{DD} = +12V$
I_{GG} Supply Current	—	—	10.0	mA	$V_{GG} = -28V$
D.C. Noise Immunity (Note 2)	±1.0	—	—	Volts	
AC CHARACTERISTICS					
Input Repetition Rate	D.C.	—	50	KHz	
Input Capacitance	—	—	5	pF	$V_{IN} = 0V$

**Typical values are at +25°C and nominal voltages

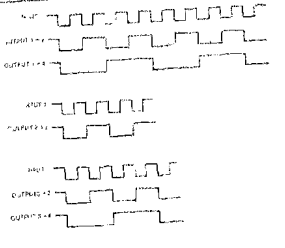
NOTES

1. Outputs may be momentarily grounded (individually) without damage to the device.
2. D.C. noise immunity is defined as follows:
   "1" state N.I. = V_{OH} "1" — V_{IN} "1" = [-10] - [-8] = 2V
   "0" state N.I. = V_{IN} "0" — V_{OUT} "0" = [-2] - [-1] = 1V
3. V_{DD} not used internally. Used for output negative supply only.
4. Outputs change on the negative transition of the respective inputs.

TIMING DIAGRAMS

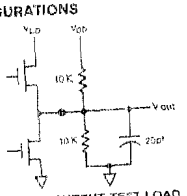


AY-1-1006

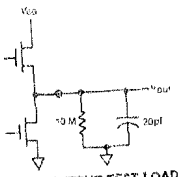


AY-1-2006

CIRCUIT TEST CONFIGURATIONS



BUFFER OUTPUT TEST LOAD



TRIGGER OUTPUT TEST LOAD

7-Stage Frequency Divider

FEATURES

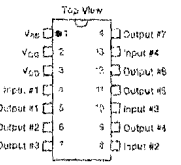
- Sine or Square Wave Input
- Low Impedance Push-Pull Outputs
- Seven Divider Stages
- Power-On-Reset

DESCRIPTION

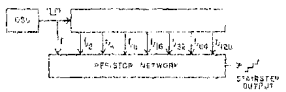
The AY-1-1007B is a monolithic frequency divider circuit which utilizes MOS technology. The divider circuit consists of seven flip-flops arranged in a 3-2-1-1 configuration and diffused into a single silicon substrate. The circuit can be driven from a sine or square wave input. Each flip-flop has a low impedance push-pull output which is capable of driving external circuitry as well as other flip-flops.

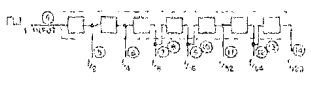
PIN CONFIGURATION

14 LEAD DUAL IN LINE

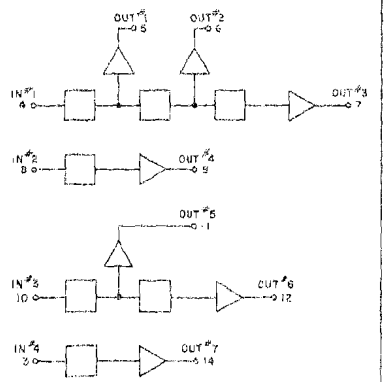


TYPICAL APPLICATIONS

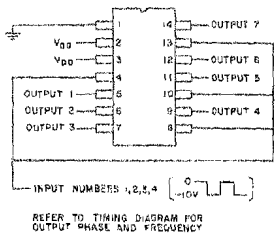




BLOCK DIAGRAM



CIRCUIT TEST CONFIGURATION



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} ..... -30V to +0.3V
Storage Temperature ..... -55°C to +150°C
Operating Temperature (T_A) ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

$-14 \leq V_{DD} \leq +0.3V$ $V_{CC} = -27V \pm 2V$ $V_{SS} = GND$

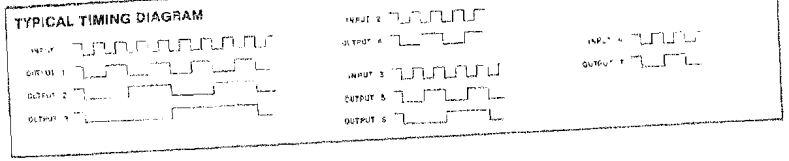
Characteristics	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Leakage	—	—	1	μA	$V_{IN} = -20V$
Input Positive Level	—	—	-2.0	Volts	
Input Negative Level	-9.0	—	—	Volts	
Output Positive Level	—	—	-1.6	Volts	$V_{OUT} = -27V$, $V_{DD} = -12V$,
Output Negative Level	-11.0	—	—	Volts	$V_{CC} = -27V$, $V_{DD} = -12V$,
I_{GG} Supply Current	—	—	14.0	mA	$V_{GG} = -25V$,
D.C. Noise Immunity (Note 2)	-1.0	—	—	Volts	
AC CHARACTERISTICS					
Input Repetition Rate	D.C	—	50	KHz	
Input Capacitance	—	—	5	pF	$V_{IN} = 0V$

**Typical values are at +25°C and nominal voltages.

Notes

1. Outputs may be momentarily grounded (individually) without damage to the device.
2. D.C. noise immunity is defined as follows:
   "1" state N.I. = V_{OUT} "1" — V_{IN} "1" = [-10] -[-9] = 1V
   "0" state N.I. = V_{IN} "0" —V_{OUT} "0" = [-2] -[-1] = 1V
3. V_{DD} not used internally. Used for output negative supply only.
4. Typical output impedance to V_{SS} or V_{DD} is 1.2KOhms

TYPICAL TIMING DIAGRAM



2^{16} I^2L Frequency Divider

FEATURES

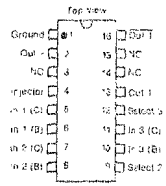
- Crystal oscillator input
- RC oscillator input
- Sine or square wave input
- Divide by 2^{16}, 2^{15}, 2^{12}, 2^{11}, 2^{10}, or 2^7
- TTL interface capability

DESCRIPTION

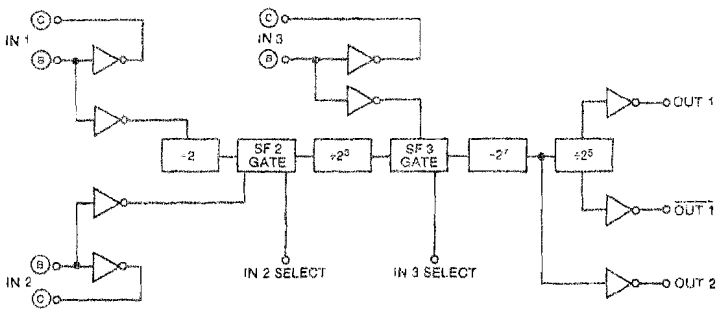
The AY-9-1000 is a monolithic frequency divider that uses General Instrument's bipolar logic. This logic uses an ion-implanted integrated injection technique, which allows operation in environments normally too hostile for average MOS technology. High speed low power operation and TTL interface capability are also provided using this technique.

The AY-9-1000 inverter inputs are intended for use as a crystal oscillator/amplifier; however, they may be used as a normal logic inverter if desired.

PIN CONFIGURATION
16 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Open Collector Voltage (V_{oh})	7.0 Volts
Supply Current (I_{cc})	200mA
Input Current	20mA
Storage Temperature	-55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

STANDARD CONDITIONS (unless otherwise noted)

V_{CC} = 5V (Note 1) R_i = 1600Ω (Resistor from V_{CC} to Injection Input Pin)
T_A = 25°C Open Collector Outputs tied to V_{CC} via 2400 ohm Resistors

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
Supply Current (Note 2)	I_{cc}	---	15.0	---	mA	
High Level Output Voltage	V_{oh}	4.8	---	5.0	V	
Low Level Output Voltage (I_{ol} = 2.0mA)	V_{ol}	---	0.2	0.4	V	
High Level Input Voltage	V_{ih}	---	0.7	---	V	
Low Level Input Voltage	V	---	0.4	---	V	
High Level Input Current (V_{ih} = 750mV)	I_{ih}	-	50	100	µA	

**Typical values are at +25°C and nominal voltages

1. Normal device voltage is about 750mV. Operation is a function of the current through a resistor from V_{CC} to injection pin. The outputs are open collector devices.

2. I_{CC} is a function of the programming resistor R_i.

5

INPUT CHARACTERISTICS (at -25°C)

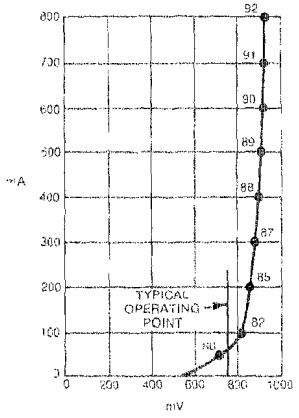


Fig.1 INPUT CURRENT vs INPUT VOLTAGE

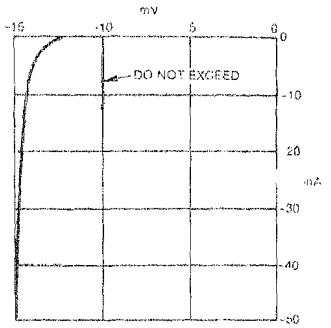


Fig.2 REVERSE BREAKDOWN

INJECTOR CHARACTERISTICS (at +25°C)

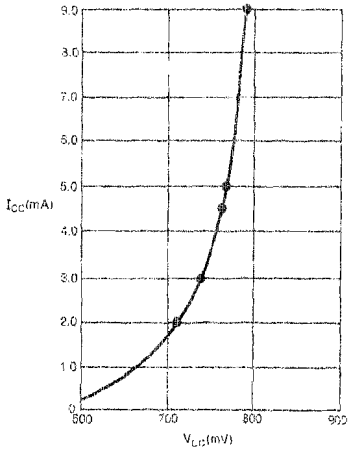


Fig.3 INJECTOR CURRENT vs. INJECTOR VOLTAGE

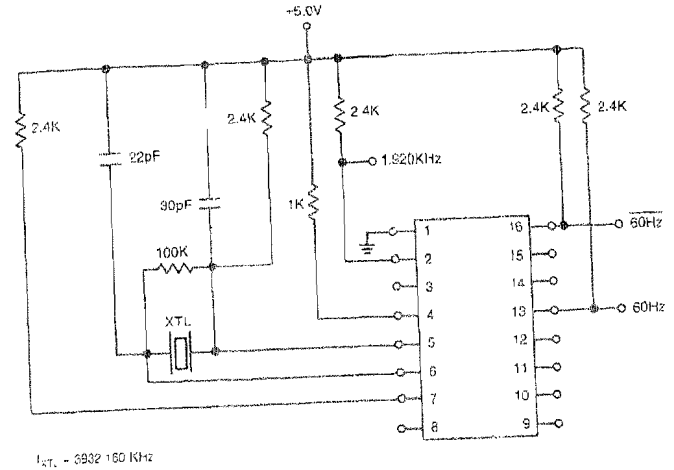


Fig. 4 — TYPICAL APPLICATION (60Hz CLOCK)

5

APPLIANCES / SECURITY

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
CLOCK TIMER	24 hour programmable repeatable on/off time switch with 4 digit clock	AY-5-1230	6-2
		AY-5-1231	6-2
		AY-5-1232	6-2
		AY-5-1233	6-2
COOKER TIMER	Appliance timer with clock Full control of "start" time "stop" time, or "duration."	AY-5-1250	6-6
		AY-5-1251	6-6
COINBOX CIRCUIT	A coin memory/credit accumulator for use in coin-operated equipment	AY-1-8622	6-10
IONIZATION SMOKE DETECTOR	Complete ionization smoke detector circuitry in a single CMOS LSI	MEM4962	6-15

6

APPLIANCES/SECURITY

MICRO ELECTRONICS

Clock / Appliance Timers

FEATURES

- 4 Digit Clock
- Drives 7 segment Fluorescent Displays
- Programmable switch on and switch off times.
- Repeating or non-repeating operation.
- Dimming control.
- Power on reset, remains reset until time is set
- Foolproof switch on/off setting, if switch off time not programmed output stays on for 10 minutes only
- Non multiplexed set inputs for low radiated noise
- Indication of set alarm state
- AY-5-1230/1232/1233:50Hz input, 24 hour operation
- AY-5-1231: 50/60Hz input, 12/24 hour operation.

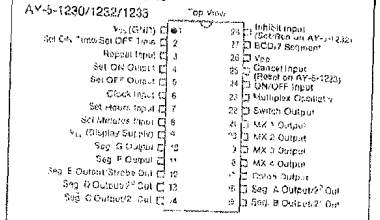
DESCRIPTION

The AY-5-1230 Series Clock/Appliance Timers are circuits designed to provide a four digit clock display and automatic on/off switching of a TV or other appliance at any desired time. A typical application would be the use of an AY-5-1230 Series circuit with GI's AY-5-8320 TV Time/Channel Display circuit to provide a clock display and automatic on and off switching of the TV at any desired time.

PIN CONFIGURATION

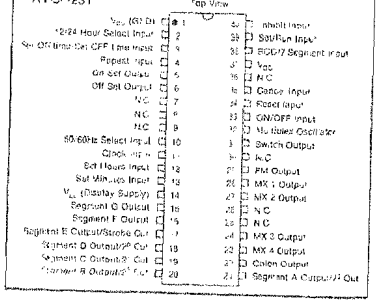
28 LEAD DUAL IN LINE

AY-5-1230/1232/1233

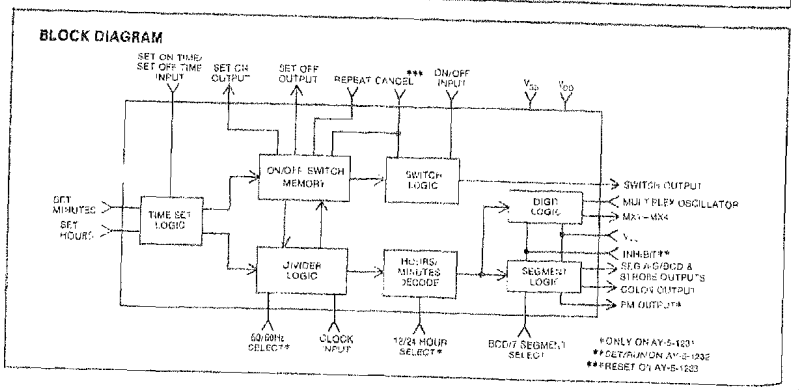


40 LEAD DUAL IN LINE

AY-5-1231



BLOCK DIAGRAM



PIN FUNCTIONS

AY-5-1230 Pin. No.	AY-5-1231 Pin No.	AY-5-1232 Pin No.	AY-5-1233 Pin No.	Name	Function
1.	1.	1.	1.	V_{SS}	Positive Supply
2.	3.	2.	2	Set ON time/ Set OFF time Input	When taken to logic '0' the ON time is displayed and the Set hours and Set minutes inputs operate the ON time counter. When taken to logic '1' the OFF time is displayed and the Set hours and Set minutes inputs operate the OFF time counter. When left open circuit the time is displayed. When either Set ON or Set OFF is activated the Switch logic is set and the switch output will operate at the set times.
3.	4	3	3	Repeat Input	When connected to logic '0' the Switch output comes on every 24 hours. When left open circuit the Switch output comes on only once after which the Switch logic is reset. The switch logic can be set again by pressing Set ON and Set OFF.
4	5	4	4.	Set ON Output	This output goes to logic '0' when an ON time has been set. It returns to '1' when the switch logic has timed out or has been cancelled
5.	6.	5.	5	Set OFF Output	This output goes to logic '0' when an OFF time has been set. It returns to '1' when the switch logic has timed out or has been cancelled.
6	11.	6.	6.	Clock Input	The timing clock is input to this pin. Hysteresis is provided so that the input waveform is not critical.
7	12.	7	7.	Set Hours Input	When this input is taken to logic '0' the hours counter is advanced twice per second.
8.	13	8.	8.	Set Minutes Input	When this input is taken to logic '0' the minutes counter is advanced twice per second. During setting the minutes counter does not overflow into the hours counter.
9	14	9	9	V_{LL} (Display Supply)	The on chip pull down resistors provided for each high voltage output are connected to this pin. When driving fluorescent display this pin is connected to -32 Volts.
10-16	15-21	10-16	10-16	7 Segment Outputs	High voltage outputs capable of driving fluorescent displays directly. At logic '0' to display. They have on-chip pull down resistors to V_{LL}
13-16	16-21	13-16	13-16	BCD Outputs	In the BCD mode the time data is output on these pins
17	22	17.	17.	Colon Output	This high voltage output is enabled on MX3 time and flashes once per second.
18-21	23,24 27,28	18-21	18-21	MX4-MX1 Outputs	These outputs are switched to logic '0' successively to select the digits, MX4 is 10s hours, MX1 is units mins. There are 5 time slots the fifth being blank. These outputs are high voltage and have on-chip pull down resistors to V_{LL}
22.	31.	22	22.	Switch Output	This output goes to logic '0' when the ON time is reached and returns to logic '1' when the OFF time is reached. If an OFF time has not been programmed the output will return to logic '1' ten minutes after the ON time has been reached. The output will sink 30mA
23.	32	23.	23.	Multiplex Oscillator	Not used normally. An external capacitor can be connected to reduce the mux frequency, or an external clock can be applied if required.
24	33.	24.	24.	ON/OFF Input	When this input is taken to logic '0' the switch output is alternately turned ON and OFF. This input has antibounce logic to prevent maloperation.
25	35	25	—	Cancel Input	When this input is taken to logic '0' the Switch logic is reset and the Switch output turned off
26.	37	26.	26.	V_{DD}	Negative supply 15V nom. (11-19V)
27.	38.	27.	27.	BCD/7 Segment Select	When this input is wired to logic '0' BCD operation results
28.	40	—	—	Inhibit Input	When this input is taken to logic '0' display outputs are switched off. This input can be used for display dimming
—	2	—	—	12/24 Hour Select	When connected to V_{SS} selects 12 hour operation.
—	10	—	—	50/60Hz Select	When connected to V_{SS} selects 60Hz operation
—	29.	—	—	PM Output	This output is on during the PM period. It is a high voltage output enabled at MX4 time slot
—	39	28.	—	Set/Run Input	When taken to logic '1', the clock is stopped and the seconds counter is reset to zero
—	34	—	25	Reset Input	When taken to logic '0', this input resets either the clock, the "on" time, or the "off" time, depending on the state of the Set ON and Set OFF inputs

NOTE:
1. All inputs have a pull down resistor to V_{DD}
2. At power-on the chip is reset but the clock does not start to count until either the set hours or set minutes button has been pressed.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin (except display pins) with respect to V_{ss} pin	+0.3 to −20V
Voltage on display pins with respect to V_{ss} pin	+0.3 to −35V
Operating temperature range	0°C to +70°C
Storage temperature range	−55°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at those conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{ss} = 0V
V_{DD} = −11 to −9V
V_{LL} = −31 to −33V
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	50/60	—	Hz	50Hz only on AY-5-1230/1232/1233.
Logic '0'	+0.5	—	−2	Volts	Note 1
Logic '1'	+10	—	−19	Volts	
Multiplex Clock Frequency	—	100	—	KHz	Note 2
Control Inputs					
Logic '0'	+0.3	—	−1.5	Volts	
Logic '1'	6	—	−19	Volts	
Pull Up Resistance	—	200	—	Kohm	to V_{DD}
Segment Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 2mA
Logic '1'	—	—	10	uA	V_{OUT} = −35V
Mx Outputs					
Logic '0'	—	—	2	Volts	I_{OUT} = 5mA
Logic '1'	—	—	10	µA	V_{OUT} = 35V
Pull Up Resistance	—	200	—	Kohm	to V_{LL}
Switch Output					
Logic '0'	—	—	−2	Volts	I_{OUT} = 30mA
Logic '1'	—	—	10	µA	V_{OUT} = −19V
Set ON, OFF Outputs:					
Logic '0'	—	—	−2	Volts	I_{OUT} = −2mA
Logic '1'	—	—	10	µA	V_{OUT} = −19V
Power	—	350	—	mW	

**Typical values are at −25°C and nominal voltages

NOTE
1. The clock input may be taken positive provided that the current is limited to 100µA
2. This results in a multiplex rate of 5KHz.

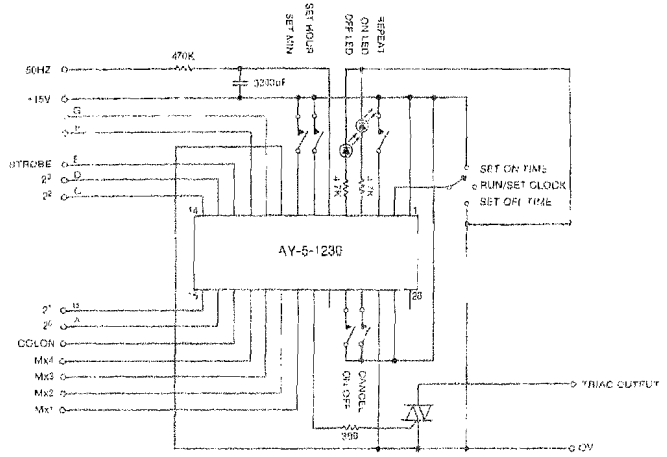


Fig.1 AY-5-1230 CONNECTION DIAGRAM

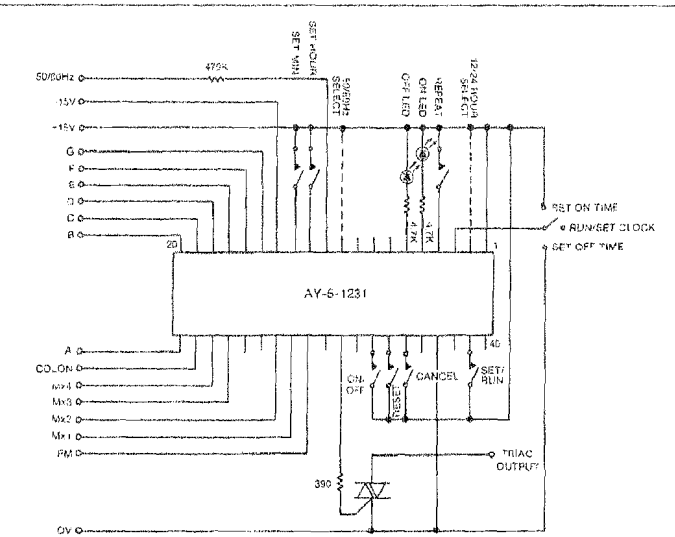


Fig.2 AY-5-1231 CONNECTION DIAGRAM

Cooker Timers

FEATURES

- 12/24 Hour Clock
- 3 Timing Functions Start, Stop, Duration
- Separate 'minute minder' function
- AY-5-1250 Daily repeat mode for central heating control
- AY-5-1251 Temperature programming capability
- Three high current timed outputs

DESCRIPTION

The AY-5-1250/1251 are designed to be incorporated in domestic cookers/stoves. In addition to the three timing functions for automatic cooking the circuit includes a count-down timer (Minute Minder). Control of an oven temperature for 2 of the outputs is also provided.

Both clocks and automatic timer controls can use 12 or 24 hour systems, but when the 12 hour mode a P.M. key is provided to enable the controls to be set more than 12 hours ahead.

PIN CONFIGURATION

28 LEAD DUAL IN LINE

AY-5-1250 KEYBOARD FUNCTIONS

(a) 12/24 hour — Wiring selectable option. PM indicator when in 12 hours.

(b) 50/60Hz — Wiring selectable option.

(c) Separate Minute Minder Display — (i) 4 digit display - when minute minder selected then required period is shown in the time window. (ii) Minute minder display is continuously shown on a separate 3 digit display.

(d) Time Switch 1 — A wiring selectable function. (i) When time buttons depressed their digits advanced at 2Hz. (ii) Digits advance at 2Hz for 4 counts and then at 8Hz.

(e) Time Switch 2 — A wiring selectable function. (i) On selecting an automatic timed function that function remains displayed for 5 secs following release of the select key or increment time keys. (ii) Function remains displayed until another time function is selected.

(f) Repeat Mode — Wiring selectable function. (i) Cooker application - all automatic register memories revert to zero after time period complete. (ii) Central Heating application. Outputs activated each 24 hour period.

(g) Auto/Manual Switch — A wiring selectable function. (i) When automatic time controls are set then automatic cooking is set immediately the AUTO lamp lights. (ii) In this mode the automatic time controls are set but the AUTO lights are not illuminated (except to flash to indicate error conditions in time setting) until the Auto/Manual Switch is depressed.

AY-5-1251 KEYBOARD FUNCTIONS

(a) 12/24 hour — A key position to be permanently wired to select 24 hour operation and left open circuit for 12 hour operation.

(b) 50/60Hz — A wiring selectable option.

(c) Separate Minute Minder Display — A wiring selectable function. (i) 4 digit display - when minute minder selected then required period is shown in the time window, for 5 seconds. (ii) When minute minder selected the required period is entered into an additional 3 digit display and remains illuminated.

(d) Number Keyboard — A push button keyboard with the numbers 0-9, a PM key for 12 hour system, and a clear key. (If oven temperature control is possible then the temperature setting could be either linear on a potentiometer or digital through the keyboard, having first depressed a temperature key).

OPERATION

On initial switch-on all registers are set to zero and any display selected reads a single '0' in the R.H. position. No output is in the AUTO mode.

Following any AC line failure the initial condition is re-established. Provision of a capacitor in the power supply circuit will enable the chip to remain active during AC line transients.

If the external standby oscillator is connected then true time is maintained from battery operation (though not displayed) during power failure. Time memories are also stored. On resumption of the main power a lamp is lit to indicate that a failure has occured.

The standby oscillator is of acceptable accuracy from passive components (2 minutes per day).

Time Display

A 4 digit display of time in either 12 or 24 hour mode as selected. An LED is provided to indicate PM times when in the 12 hour mode (this could be incorporated in the display).

When the 'Set Time' key is depressed the display is blanked, and the colon commences to flash at 1Hz. The time is entered through the keyboard commencing with the hours. Digits are displayed from the RHS; in this manner leading zeros remain suppressed.

A second depression of the 'Set Time' key causes the colon to be illuminated constantly and the clock to operate from the mains supply. The internal 'seconds' register starts to operate from the '0' state.

In the event of a false time being entered (more than 23 hours or 59 minutes) the colon continues to flash and buzzer sounds at 1Hz. modulation. The clock fails to start. False entries can be deleted by depression of the 'clear key'.

Automatic Output Control

Two outputs (3 on the AY-5-1251) are under the control of the automatic timer. The controls are "Set Start Time", "Set Stop Time" and "Set Cook Duration", although on any manufacturers model only 2 of the 3 are necessary.

Two keys can be used for each controlled output, or alternatively one pair of keys with a 2 (or 3) position switch to direct the information to the relevant chip input can be used.

(a) SETTING

Set Start Time When depressed this key immediately lights up and the time display colon commences to flash. The display shows the previously set Start Time if a cooking period is incomplete, or a single '0' on the RHS if no period is underway. A 'Start Time' is fixed with the same Set Keys. To set a time commencing with 0 hours it is necessary to give a single depression to the Set Hours key (counting commences with 0) to illuminate the hours digit.

If Time Switch 2 is in the static position then the display reads the "Start Time" until another function is selected, otherwise it reverts to Real Time and a constant colon 5 secs after releasing the Set Time, Set Hours or Set Minutes key.

The relevant AUTO lamp lights after the 5 seconds if a Cook Duration or Stop Time has been previously set. Automatic Cooking is set (See note Paragraph 2g).

Set Cook Duration Functions as the 'Set Start Time' switch, except the Cook Duration switch is illuminated. The relevant AUTO lamp lights if a Stop Time or Start Time has been previously set, although the AUTO lamp flashes and automatic cooking is not set if the cook duration is greater than the period between the real time and selected Stop Time.

To enter a Cook Duration of less than one hour it is only necessary to use the 'Set Minutes' button.

Set Stop Time Functions as the 'Set Start Time' switch, except Stop Time' Switch is illuminated.

The relevant AUTO lamp lights.

If a cook duration has been selected which is greater than the period between the real time and the selected stop time then the AUTO lamp flashes and automatic cooking is not set.

(b) USE

Fully Automatic: The time controls are set and the oven temperature selected. When the real time reaches the Start Time selected (or the Stop Time less the Cook Duration) the relevant output is activated and lights the ON lamp. At the conclusion of cooking both the AUTO and the ON lamps are extinguished and the relevant timing registers revert to 0. The audio output gives a 1Hz cycle for 10 secs.

Where the Auto/Manual button is included then cooking can be terminated at any time by the momentary depression of this switch, which will also cancel the AUTO lamp.

Semi-Automatic: The 'Stop Time' is set and oven temperature selected. Cooking continues until the Stop Time is reached, when the AUTO and ON lamps are extinguished and the Stop Time register reverts to zero. The audio output gives a 1Hz cycle for 10 secs.

Manual: Operation is simply through the oven temperature select switch.

INFORMATION RECALL

Times selected for automatic operation can be displayed for 5 seconds by depression of the appropriate key.

If the Cook Duration is interrogated during cooking then the time remaining before completion is displayed.

MINUTE MINDER (Short Term Alarm)

Depression of the 'Minute Minder' key illuminates that key and displays the contents of the MM register. The display colon flashes.

Time is entered from the keyboard - any increment of 1 minute is accepted from 1 minute to 9 hours 59 minutes.

5 secs. following the last entry key the colon ceases to flash and the countdown commences (providing no false time has been entered - greater than 9 hours or 59 minutes. Use of the clear key will delete a false entry). It is important that the countdown starts immediately following this 5 secs. period rather than to couple the MM register to that for true time for in this latter case an error of up to 59 secs. can occur and seriously distort short periods.

For models with a separate MM display the time remaining to the end of the selected period is continuously shown. For single display models this time can be displayed by depressing the MM key and remains for 5 secs. following release of this key.

On completion of the selected period the audio output gives a continuous tone for 1 minute. This tone can be cancelled by depressing the MM key.

The minute minder setting can be cancelled at any time by depressing the MM key followed by the clear key.

CENTRAL HEATING OPERATION with the AY-5-1250:

For this application an additional output is provided which is the composite signal of the two timed outputs in order to minimize external peripheral circuitry

The Repeat mode is selected to enable the two timed periods to remain stored and operate every 24 hours.

Setting Start and Stop times is achieved in precisely the same manner as previously described

Cancel

Cancel buttons are provided for each output which, when depressed, extinguish the relevant AUTO lamp and inhibit the output signal even though the Start and Stop times remain in memory. The output can be restored by depressing the Start and Stop time keys, whereupon the AUTO lamp lights up

On/Off Control

This is a bistable action switch which changes the state of the composite signal output switch. If the output were OFF then this switch turns it ON until the next Stop Time; if it were ON then it becomes switched OFF until the next Start Time

Further depression again changes the state

ELECTRICAL CHARACTERISTICS

V_{DD}	9V
Operating temperature range	0°C to 70°C
Clock Input	50Hz or 60Hz
Internal Multiplex Clock frequency	100KHz
Display outputs	Suitable to drive LED displays up to 0.5" high. Segments are driven directly Fluorescent compatibility
Timed outputs	3 timed outputs are provided with 30mA drive capability to operate a triac or relay
Audio output	Continuous tone for 30 secs. on completion of minute minder period. 1Hz cycle for 10 secs. on completion of automatic cooking period. Tone 1KHz — nominal
Keyboard	Keybounce protection and two key lockout provided.

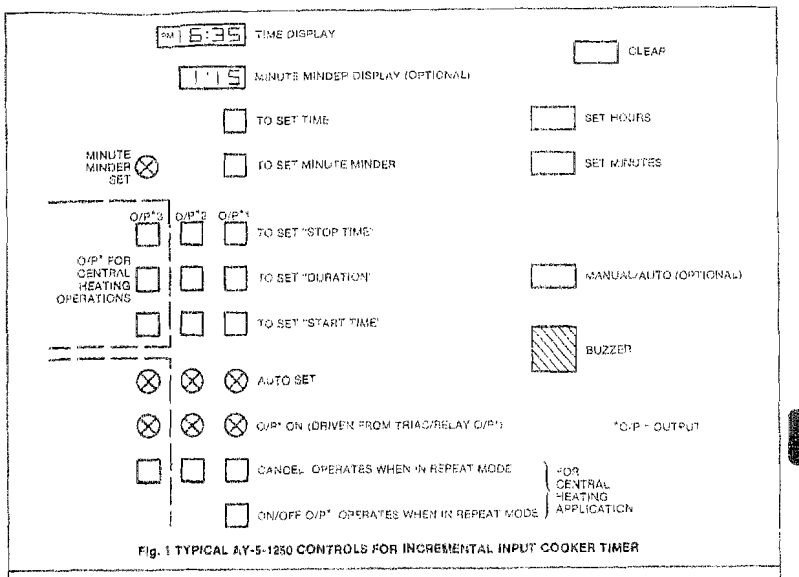


Fig. 1 TYPICAL AY-5-1250 CONTROLS FOR INCREMENTAL INPUT COOKER TIMER

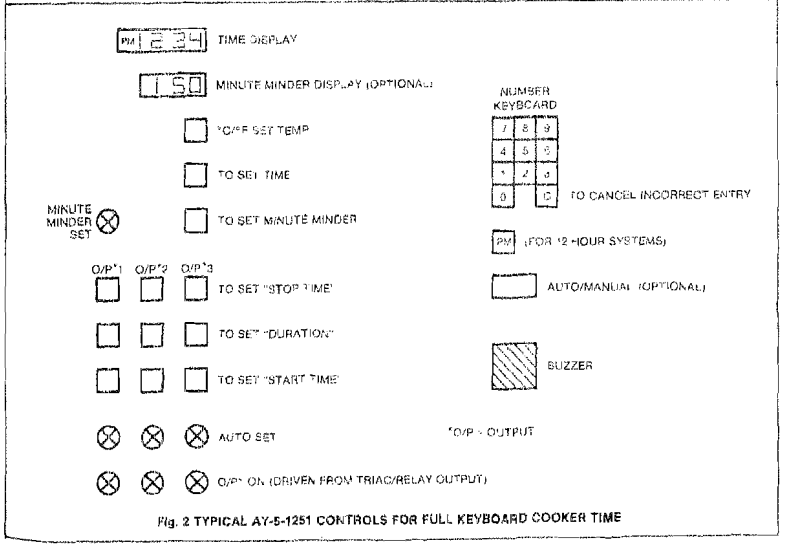


Fig. 2 TYPICAL AY-5-1251 CONTROLS FOR FULL KEYBOARD COOKER TIME

Coinbox Circuit

FEATURES

- 63 Credit Capacity
- 2 Special Selection Options
- 7 Different Coin Inputs
- Easy Price or Program Change
- "Make Selection" Control
- Input Noise Rejection on Chip
- On Chip Clock Oscillator

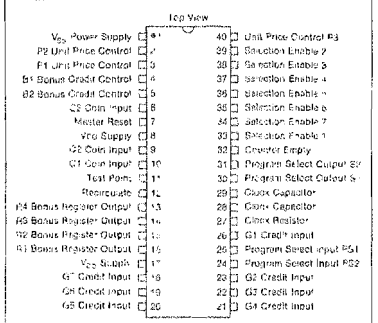
APPLICATIONS

- Arcade Equipment
- Vending Machines
- Gaming Devices
- Programmable Counters and Timers

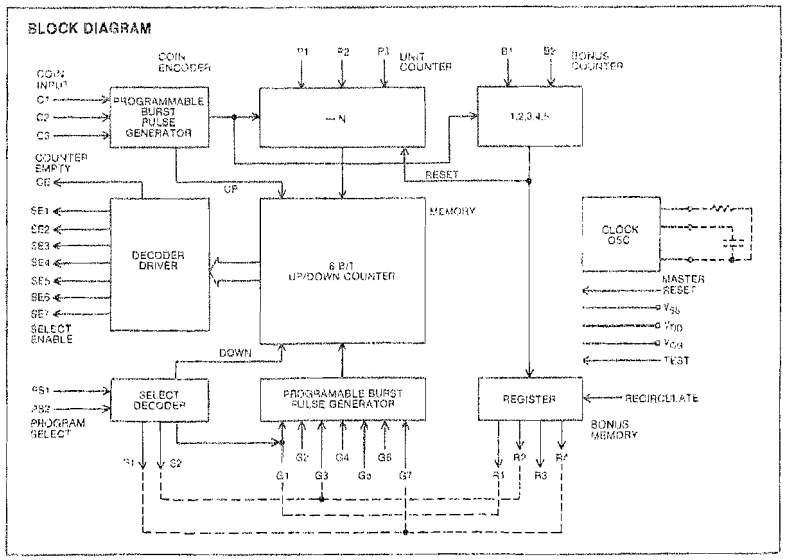
DESCRIPTION

The General Instrument AY-1-8622 is a single monolithic P channel MOS/LSI Chip designed for use as a credit accumulator in coin-operated equipment. The chip requires only a power supply and a coin acceptor to complete the cash register section. Coin inputs allow 7 different coin or paper denominations to be used. Both credit and bonus price are easily changed in the field. Two special selection options may be programmed.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PROGRAMMING THE AY-1-8622

The AY-1-8622 has been designed for the maximum versatility compatible with one package. The user can program the device to operate with different currencies and with different pricing or credit structures.

Currency Programming

C1, C2, and C3 form the 3 coin inputs, with weighting as indicated under the pin function section of this data sheet. If, for example, a nickle (5¢) is chosen as one unit, a dime (10¢) would have a weight of two units, a quarter (25¢) a weight of five units, etc. In this case, the user would program his coin acceptor to produce a "1" at C1 when a 5¢ piece is deposited, a "1" at C2 when a dime is deposited and a "1" at C3 when a 25¢ piece is deposited.

Pricing Structure Programming

Pricing structure consists of three controllable options: Unit Price Control, Bonus Credit Control, and Program Select Control. The first two of these control how many play credits the customer receives for his coin deposits. Program Select Control determines how many play credits are used by his various play options.

Unit Price Control is through inputs P1, P2, and P3. If, for example, 5¢ is one unit, and 10¢ is one play, P2 would be tied to logic "1". If 25¢ is one play, the P1, P2, and P3 would all be tied to "0".

In many applications it is desirable to present the customer with an incentive for depositing additional money to receive "bonus" plays. For example, two plays for 25¢, five plays for 50¢. This option is controlled by the Bonus Credit Control.

Bonus Credit Control, is derived through inputs B1 and B2, in conjuction with the Program Control Matrix. Unlike the unit price control section which drives the credit accumulator directly, the Bonus Credit Control drives a shift register whose outputs, R1 through R4, form part of the Program Control Matrix. B1 and B2 control how many units are required to increment the shift register. The first bonus places a "0" onto R1, the second moves it to R2, etc.

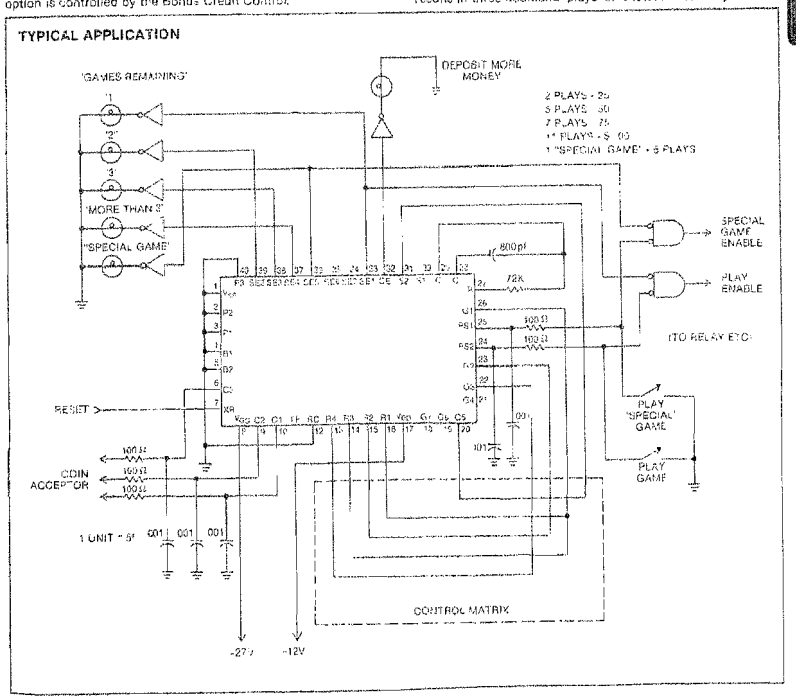
Control Matrix

The Control Matrix consists of three sections. S1 and S2 form the Program Select Outputs, G1 through G7 form the inputs to the Credit Accumulator, and R1 through R4 are the Bonus Register Outputs. The Credit Accumulator, a 6 bit up/down counter, is automatically placed in the "up" count mode when a coin input is made, and a "down" count mode when a selection is made. Although single selections and unit price inputs are fed directly into the counter, special play options and bonus credits are entered through the matrix. A "0" on G1 places 1 credit/debit into the counter, a "0" on G2 places 2 credits/debits into the counter, etc.

Typical Example

In the typical application shown one unit is 5¢. P1, P2, P3, B1 and B2 are tied to "0". As a result, there is one play for 25¢ from the Unit Price Control, and one bonus for 25¢. By tying R1 to G1, the bonus gives a bonus play for 25¢, resulting in a total of two plays for 25¢. R2 is tied to G2, so that the deposit of an additional 25¢ results in three additional plays, or a total of fives plays for 50¢.

TYPICAL APPLICATION



OPERATION

Coin inputs are encoded into a series of pulses by the coin encoder. These pulses are fed into the unit price control divider, controlled by P1, P2 and P3, and into the bonus credit control divider controlled by B1 and B2. The output from the unit price control divider goes to the 6 bit memory. The output from the bonus credit control clocks a 4 bit shift register. The first bonus credit places a "0" into R1, the second moves the "0" to R2 etc.

The memory, a 6 bit up/down counter, is placed into an "up" count mode when coin inputs are made, and a "down" count mode when selections are made. Input to it comes from the unit price control and from a pulse generator controlled by G1-G7, S1, S2. R1-R4 and G1-G7 form the program control matrix and are interconnected by the user to allow the programming of the number of credits triggered by bonuses and debits triggered by selections.

PIN FUNCTIONS

Pin No.	Name	Symbol	Description
1	V_{SS} Power Supply	V_{SS}	Ground
2,3,40	Unit Price Controls	P2,P1,P3	P1, P2, P3 determine the price in units per credit by the following Matrix P3 P2 P1 — Units per credit 0 0 1 — 1 0 1 0 — 2 1 0 0 — 3 0 1 1 — 4 0 0 0 — 5
4,5	Bonus Credit Controls	B1,B2	B1, B2 determine the number of units needed to increment the bonus shift register one place as follows B2 B1 — Units per bonus Credit 1 1 — 1 0 1 — 2 1 0 — 4 0 0 — 5
6,9,10	Coin Inputs	C3,C2,C1	C1, C2, C3 are coin inputs. Inputs are weighted as follows C3 C2 C1 — Weight 0 0 0 — no input 0 0 1 — 1 unit 0 1 0 — 2 units 0 1 1 — 4 units 1 0 0 — 5 units 1 1 1 — 8 units 1 0 1 — 10 units 1 1 0 — 20 units
7	Master Reset	MR	All counters and registers are reset by a logic "1"
8	V_{GG} Supply	V_{GG}	-27 Volt supply
11	Test Point	TP	For Testing only. Do not make external connections to this Pin
12	Recirculate	RC	Logic "1" on Pin 12 locks the bonus shift register after it reaches the 4 bonus credit level. Logic "0" on Pin 12 allows shift register to re-cycle from the fourth level to the first
13,14 15,16	Bonus Register Outputs	R4,R3 R2,R1	The bonus register outputs indicate the status of the bonus register as follows: R4 R3 R2 R1 — Bonus Credits 1 1 1 0 — 1 1 1 0 1 — 2 1 0 1 1 — 3 0 1 1 1 — 4
17	V_{DD} Supply	V_{DD}	-12 Volt supply

PIN FUNCTIONS (continued)

Pin No.	Name	Symbol	Description
18	7 Credit Input	G7	A "0" level input on a credit input enters the respective number of credits into the credit accumulator. These inputs are internally clocked by the coin inputs and program select inputs, and are for program control matrix use only. Credits are added when the coin input is addressed and are subtracted when program select inputs are enabled.
19	6 Credit Input	G6	
20	5 Credit Input	G5	
21	4 Credit Input	G4	
22	3 Credit Input	G3	
23	2 Credit Input	G2	
26	1 Credit Input	G1	
24,25	Program Select Inputs	PS2,PS1	These inputs cancel credits as follows: PS2 PS1 — Result 1 1 — No Cancellation 1 0 — Single Credit cancellation 0 1 — Option 1 selected 0 0 — Option 2 selected Selection of option 1 or 2 results in program select outputs being triggered. This allows user selection of the number of credits cancelled by both options.
27	Clock Resistor		A 800 pF capacitor between Pins 28 and 29, and a 72K resistor between Pins 27 and 29 give a nominal system frequency of 6.2KHz.
28	Clock Capacitor		
29	Clock Capacitor		
30,31	Program Select Outputs	S1,S2	Program control matrix outputs. Output states are as follows S2 S1 — Option 0 1 — Option 1 selected 1 0 — Option 2 selected Single credit select is internally connected to G1.
32	Counter Empty	CE	This Pin is at logic "1" until at least one credit is in the credit counter
33	Selection Enable 1	SE1	The Selection Enable outputs indicate the number of credits in the credit counter as follows: SE7 SE6 SE5 SE4 SE3 SE2 SE1 — Credits 1 1 1 1 1 1 0 — 1 1 1 1 1 1 0 0 — 2 1 1 1 1 0 0 0 — 3 1 1 1 0 0 0 0 — 4 1 1 0 0 0 0 0 — 5 1 0 0 0 0 0 0 — 6 0 0 0 0 0 0 0 — 7 or more
34	Selection Enable 7	SE7	
35	Selection Enable 6	SE6	
36	Selection Enable 5	SE5	
37	Selection Enable 4	SE4	
38	Selection Enable 3	SE3	
39	Selection Enable 2	SE2	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Pin Voltages with respect to V_{SS} . . . . . -20V to +0.3V
Storage Temperature . . . . . -55°C to +150°C
Operating Temperature . . . . . -20°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions
V_{DD} = -27 ... -10V
V_{DD} = -12 ... -10V
V_{SS} = 0

Characteristic	Min.	Typ	Max	Units	Condition
All Inputs					
Logic "1"	-8.0	—	-30.0	Volts	
Logic "0"	0.3	—	-2.0	Volts	
Input Impedance	20	—	100	KΩ	
Program Control Outputs					
R1, R2, R3, R4, S1, S2	—	—	—	—	
Logic "1"	V_{DD}-0.5	—	—	Volts	100KΩ to V_{DD}
Logic "0"	—	—	-2.0	Volts	0.5mA
Select Outputs					
CE, SE1 to SE7					
Logic "1"	V_{DD}-0.5	—	—	Volts	100μA
Logic "0"	—	—	-4.0	Volts	2.0mA
Coin Input Repetition Rate	—	—	30	Hz	
Coin and Program Select Date Hold Time	20	—	—	msec	
Clock Frequency	100	—	50	KHz	6.2KHz Clock
Power Consumption	—	250	400	mW	

NOTES:

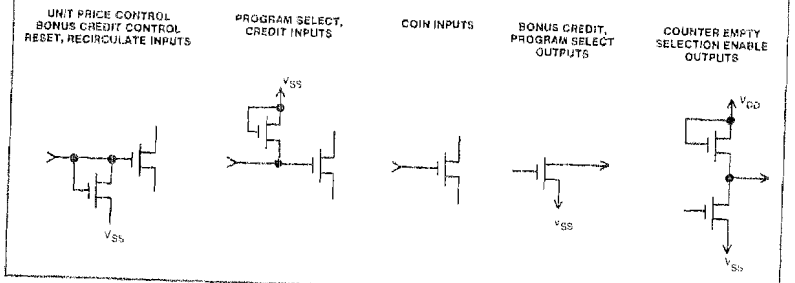
Clock Frequency: The clock frequency is determined by the values of an external timing capacitor and a resistor connected to Pin 20. An 800pF capacitor and 72K resistor will produce a clock frequency of 6.2KHz.

Master Reset: All counters and registers are reset to zero by a logic "1" on Pin 7.

Bonus Recirculate: Logic 1 on Pin 12 locks the bonus register after it reaches the 4th bonus level. Logic "0" allows the 4 bonus levels to be continuously repeated.

Test Lead: Pin 11 is internally tied to V_{DD}. No external connections should be made to this Pin.

INPUT & OUTPUT MOS STRUCTURES



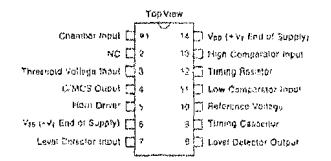
MEM 4962

Ionization Smoke Detector

FEATURES

- On-Chip Input MOSFET (Typ. 10^{13} Ω to 140°F)
- Stand-By Current Drain 10μA
- Low Battery Warning Beep
- 14-Pin DIP Package
- On-Chip Output Driver
- Designed to Meet UL 217

PIN CONFIGURATION
14 LEAD DUAL IN LINE



OPERATION

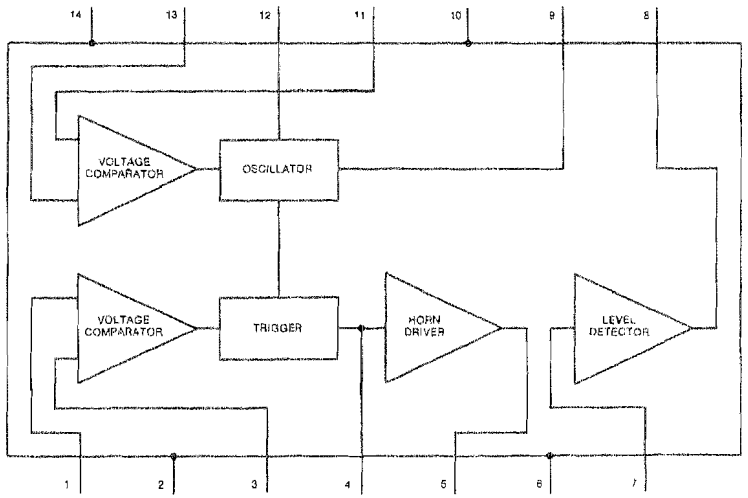
Op. Mode	Input	Osc	Output C/Mos	Output N-Ch FET
Stand-by	$V_1 < V_2$, $V_{11} < V_{12}$	Disabled	Low	Off
Alarm	$V_1 > V_3$, $V_{11} < V_{12}$	Disabled	High	On
Low Battery	$V_1 < V_2$, $V_{11} > V_{12}$	Enabled	Pulse*	Pulsed On
Low Battery Alarm	$V_1 > V_3$, $V_{11} > V_{12}$	Enabled	High	On

*With built-in nominal duty cycle of 1:1500 and nominal frequency determined by RC

LEVEL DETECTOR

V_{DD} -V_T	Output @ Pin 8
>0.2V	Low
<0.1V	High

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} 18V
Avg. Current Idd 120mA
Operating Temperature . . . . . -30 to 85°C
Storage Temperature . . . . . -30 to 100°C

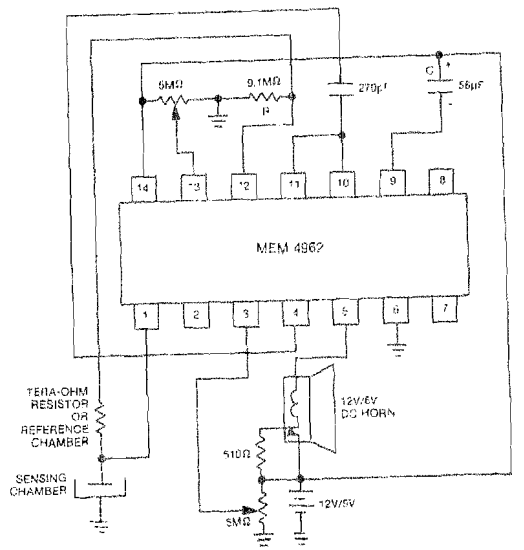
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

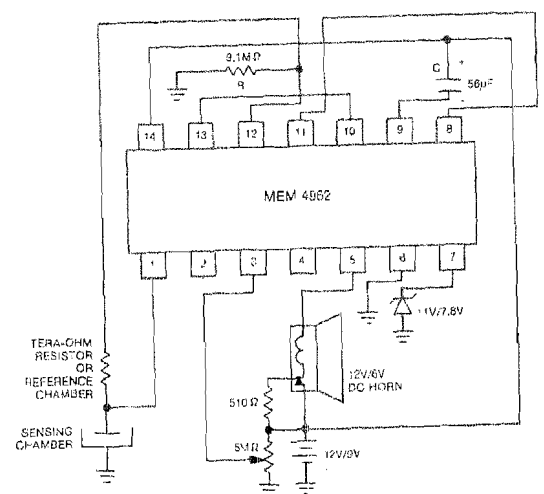
Standard Conditions (unless otherwise noted)

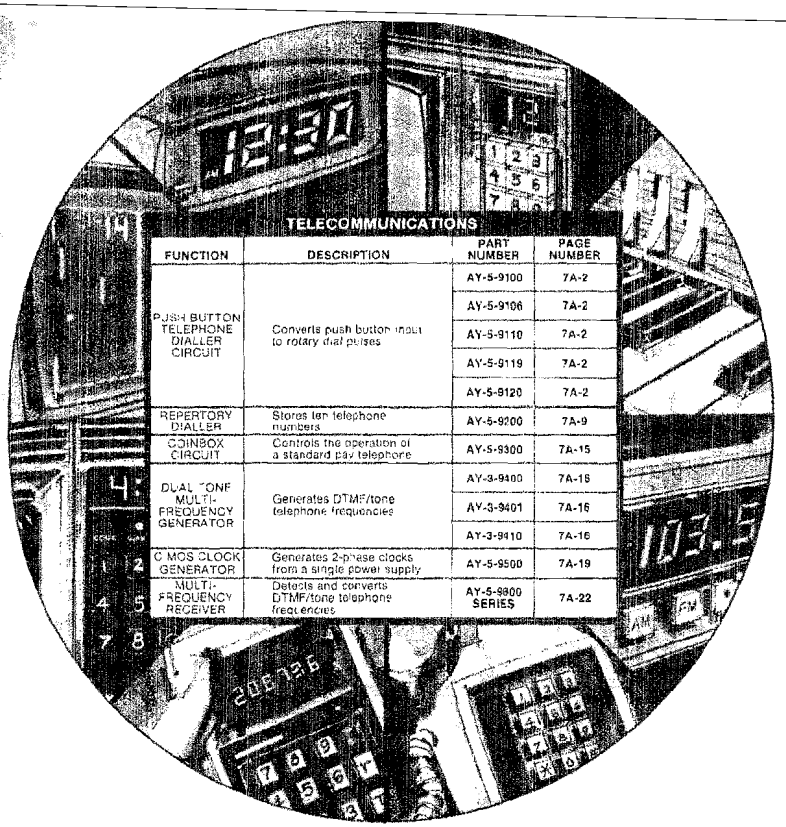
T_A = 25°C
R = 9.1MΩ (5%)
C = 56µF

Functional Block	Characteristic	Pin No.	Min	Typ	Max	Units	Conditions
Voltage Comparator	Input Leakage Current	1	—	—	1	pA	Pin 1 @ 12.6V, Others @ GND
	Pin 1 Breakdown Voltage	1	40	—	—	Volts	Other Pins @ GND
	Common Mode Input Range	1,3 11,13	0.5	—	V_{DD}-2	Volts	V_{DD} - V_{SS} = 6 to 13V
	Input Offset Voltage	1,3 11,13	—	—	50	mV	V_{DD}-V_{SS} = 11V
	Trigger Voltage	1,3 11,13	0.01	0.1	0.15	Volts	V_{DD}-V_{SS} = 6-13V
OSC.	Period	—	20	—	60	Sec	Low Battery condition V_{DD}-V_{SS} = 7.5-11V
	Duty Cycle	—	1/3000	—	1/1000	—	V_{DD}-V_{SS} = 7.5-11V
	Capacitor Charging Current	9	65	—	150	nA	Low Battery Cond., Current meter @ Pin 9 and V_{DD}, V_{DD}-V_{SS} = 7.5-11V
	Capacitor Dis-Charging Current	9	125	—	300	µA	Low Battery Cond. Current meter @ Pin 9 and V_{SS}, V_{DD}-V_{SS} = 7.5-11V
Output Devices	C/MOS Sourcing Current	4	5	—	—	mA	1k Ω load Pin 4 and V_{SS}, Alarm Condition, V_{DD}-V_{SS} = 7.5V
	Open-Drain N-Ch FET Sinking Current	5	240	—	—	mA	25 Ω load Pin 5 and V_{DD}, Alarm Condition, V_{DD}-V_{SS} = 7.5V
Complete Chip	Stand-by Current	—	—	4/7	6/10	µA	Stand-by Condition, V_{DD}-V_{SS} = 9/12V
	Low Battery Mode Current	—	—	5/9	7/13	µA	Low Battery Condition, Excluding pulse content, V_{DD}-V_{SS} = 7.5/11V
Ref. Volt.	Ref. Voltage	10	0.8	1.2	1.8	Volts	V_{DD}-V_{SS} = 7.5-11V
Level Detector	Bias Current	7	0.3	2.5/3.3	3.3/5.0	µA	V_{DD}-V_{SS} = 9/12V

TYPICAL APPLICATIONS







TELECOMMUNICATIONS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
PUSH BUTTON TELEPHONE DIALLER CIRCUIT	Converts push button input to rotary dial pulses	AY-5-9100	7A-2
		AY-5-9106	7A-2
		AY-5-9110	7A-2
		AY-5-9119	7A-2
		AY-5-9120	7A-2
REPERTORY DIALLER	Stores ten telephone numbers	AY-5-9200	7A-9
COINBOX CIRCUIT	Controls the operation of a standard pay telephone	AY-5-9300	7A-15
DUAL TONE MULTI-FREQUENCY GENERATOR	Generates DTMF/tone telephone frequencies	AY-3-9400	7A-16
		AY-3-9401	7A-16
		AY-3-9410	7A-16
C MOS CLOCK GENERATOR	Generates 2-phase clocks from a single power supply	AY-5-9500	7A-19
MULTI-FREQUENCY RECEIVER	Detects and converts DTMF/tone telephone frequencies	AY-5-9800 SERIES	7A-22

7A

TELECOMMUNICATIONS

MICRO ELECTRONICS

AY-5-9100
AY-5-9106 AY-5-9110
AY-5-9118 AY-5-9120

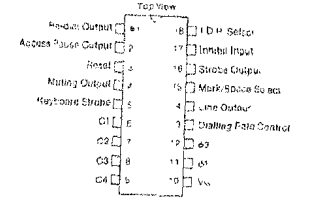
Push Button Telephone Dialler Circuits

FEATURES

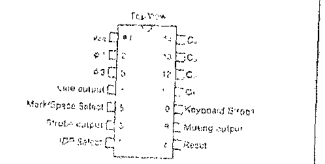
- 20 Digit Storage
- Selectable dialling rate
- Selectable mark/space ratio
- Selectable Inter-Digit Pause (except AY-5-9118)
- Dynamic circuitry — low power consumption
- Re-dial of last number (except AY-5-9118)
- Access Pause Facility (except AY-5-9118)
- Companion Repertory Dialler chip (AY-5-9200)

PIN CONFIGURATION

16 LEAD DUAL-IN-LINE
AY-5-9100/9106/9110/9120

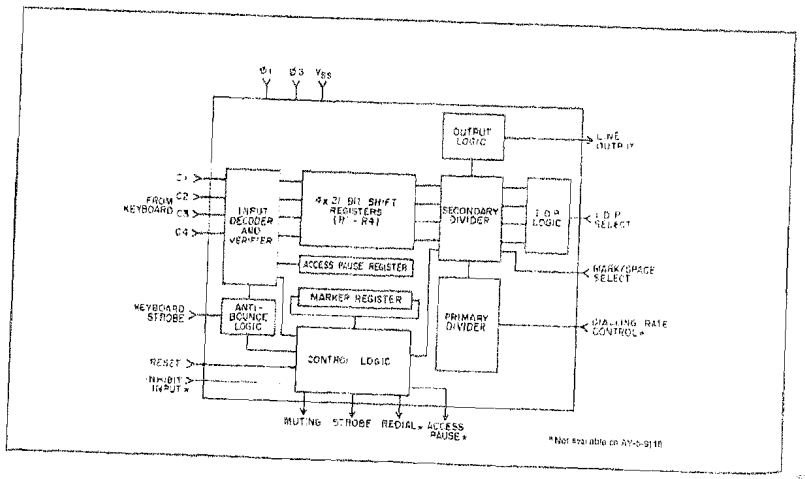


14 LEAD DUAL-IN-LINE
AY-5-9118



DESCRIPTION

The AY-5-9100 Series Push Button Dialler provides all of the logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Pulse repetition rate, interdigital pause, and mark-space ratio are all programmable. Outputs are provided for line pulsing and muting. An "inhibit input" is provided to allow storage of one number of up to 20 digits. An "Access pause" capability is provided to allow automatic operation with a PBX or WATS line system. The low power consumption enables line-powered operation in a PBX or similar system. An AY-5-9100 Series circuit may be operated alone or in conjuction with the AY-5-9200 repertory dialler.



PIN FUNCTIONS

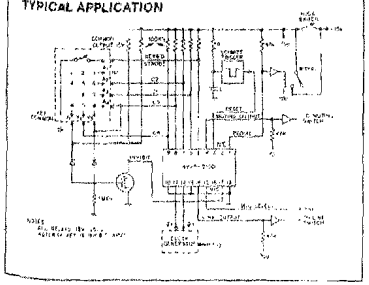
AY-5-9100 AY-5-9106 AY-5-9110 AY-5-9120 Pin No.	AY-5-9118 Pin No.	Name/Description
1	—	**Re-Dial Output** (except AY-5-9118). A logic "0" at this output indicates that redial mode has been selected
2	—	**Access Pause Output** (except AY-5-9118). A logic "0" at this output indicates that an access pause is required.
3	8	**Reset**: A logic "0" on this input clears all shift registers and resets all counters. Reset should be applied after power on to clear the device.
4	9	**Muting Output**: The muting output goes to logic "0" whenever data is being entered or transmitted. It returns to logic "1" when the access pause output turns on and when transmission is complete
5	10	**Keyboard Strobe**: This is the common signal from all the keys. A logic "0" on this input indicates that either the inhibit input or C1-C4 are to be read
6-9	11-14	**C1-C4** (except no access pause on AY-5-9118): These are the keyboard data inputs. They are encoded as follows to allow simple interface with a standard push button (2-of-7) keyboard.

		AY-5-9100/9106 AY-5-9110/9118				AY-5-9120			
Digit	Impulses	C1	C2	C3	C4	C1	C2	C3	C4
1	1	1	1	1	1	1	1	1	0
2	2	1	1	1	0	1	1	0	1
3	3	1	1	0	1	1	1	0	0
4	4	1	0	1	1	1	0	1	1
5	5	1	0	1	0	1	0	1	0
6	6	1	0	0	1	1	0	0	1
7	7	1	0	0	0	1	0	0	0
8	8	0	1	1	1	0	1	1	1
9	9	0	1	1	0	0	1	1	0
0	10	0	1	0	1	0	1	0	1
Access Pause	—	0	0	1	1	0	1	0	0

10	1	**Vss**
11	2	**φ1**
12	3	**φ3**
13	—	**Dialling Rate Control** (Fixed at 10 p.p.s. on AY-5-9118) This input controls the line pulsing frequency as follows: (See Note 1)

Input	Line Pulse Rate
φ1	600 p.p.s.
φ3	20 p.p.s.
Vss	10 p.p.s

TYPICAL APPLICATION



AY-5-9100 AY-5-9106 AY-5-9110 AY-5-9120 Pin No.	AY-5-9118 Pin No.	Name/Description
14	4	**Line Output** A logic "0" on this output is a line pulse "mark" or "break."
15	5	**Mark/Space Select** The mark to space ratio is controlled by this input as follows:

Input	Mark	Space
φ1	70	30
φ3	50	50
Logic 0	66 2/3	33 1/3
Logic 1	60	40

These ratios are exact and do not depend on clock frequency

16	5	**Strobe Output** This output goes to logic "0" to indicate that a digit is being out-pulsed
17	—	**Inhibit Input** (except AY-5-9118) The inhibit input is used to inhibit out-pulsing and to place the device in re-dial mode

The keyboard strobe must be taken to logic "0" at any time the inhibit input is strobed, except when an Access Pause is being signalled.

This input normally operates as a "toggle flip-flop". If it is taken to a logic "1" any time other than when an access pause is being signalled, the circuit will lock into the redial mode and the redial output will go to logic "0". The chip will remain in the re-dial mode until this input is taken to logic "1" again.

If the chip is cleared before inhibit is toggled, digits entered are accepted, but out-pulsing does not commence until the inhibit is re-strobed. If a number is being outpulsed when the inhibit is strobed, dialling ceases until the inhibit is re-strobed. If the inhibit is strobed when a dialling sequence is completed, the redial output goes to logic "0" and the number is stored. Re-strobing the inhibit starts the dialling sequence.

When an access pause is signalled, this input no longer operates as a toggle, but rather as a gate, with a logic "1" inhibiting further out-pulsing.

18	7	**I.D.P. Select** This input controls the inter-digital-pause as follows: (See Note 1):

Input	IDP: AY-5-9100/9106/9120		
	10p.p.s.	20p.p.s.	600p.p.s
φ3	400ms	200ms	6.66ms
Vss	800ms	400ms	13.33ms
φ1	1000ms	500ms	16.33

Input	IDP: AY-5-9110			IDP: AY-5-9118
	10p.p.s	20p.p.s.	500p.p.s.	10p.p.s
φ3	700ms	350ms	11.66ms	700ms
Vss	900ms	450ms	15ms	900ms
φ1	800ms	400ms	13.33ms	800ms

A pre-digital pause equal in length to the inter-digital pause precedes the first digit of any number.

NOTE 1: Line Pulse Frequency and Inter-Digital Pause are specified with an 18KHz clock frequency.

OPERATION

The 4 bit code from the keyboard arrives on inputs C1-C4 of the Push Button Dialer. A fifth input from the keyboard, the Keyboard Strobe, is also required. In its quiescent state the five inputs are at logic 1 (−volts). A logic 0 on the Keyboard Strobe input indicates to the input circuitry that it is to read the data on C1-C4, thus allowing 1:1 as an allowable code from the keyboard.

When a digit key is depressed the logic detects the 1-0 transition on the Keyboard Strobe input. When this occurs a timer with a minimum count time of 8.5 msec. is started. If the common input is removed before this period has elapsed, the counter will be reset to its starting state. If the Keyboard Strobe input is stable for at least 8.5 msec. the code is fed to the code verifier and converter.

If the code is invalid it is ignored. If valid it is converted to the proper BCD code and written into recirculating shift registers R1-R4. If an access pause is decoded, it is written into the access pause register.

Simultaneous with the data being written into R1-R4, the muting output goes to logic "0", to disconnect the transmission circuitry. When all digits that have been keyed into the circuit have been dialled out the muting output returns to logic "1".

During dialling if an access pause is required, the muting output will reconnect the transmission circuitry so that the caller can listen for the dial tone and ensure himself that the system is functioning correctly.

The digit store has a capacity of 20 digits. The numbers are read non destructively allowing redial.

Four 21 bit registers hold the number in BCD format, the number is stored in parallel. A fifth register holds a marker bit (Signified as A) showing the first number entered. This fifth register has a gated 22nd bit allowing the marker bit (A) to be 'slipped' backwards one bit with respect to the number. Gating ensures that all numbers are sequentially entered, the first aligning itself with the marker A. When the first number is to be located into the counter, A is decoded in its 21st position and the parallel enable signal reads the first digit into the counter. Gating is enabled to allow A to be shifted through the 22nd bit of the marker store, so aligning itself with the next number to be dialled out. When A is decoded at the 21st bit and no number is in the stored digit register, A remains aligned in this state until 'redial' is depressed and the marker store goes into its 22nd bit mode until A aligns with the first digit.

Gating ensures that only 20 digits are entered into R1-4. One empty state at least is required to indicate to the system that a number is complete.

TIMING DIAGRAMS

Fig.1 Clock Waveforms

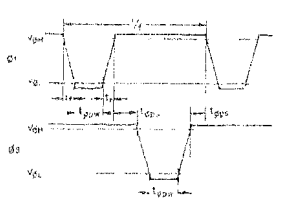


Fig.2 Reset and Keyboard Strobe Timing

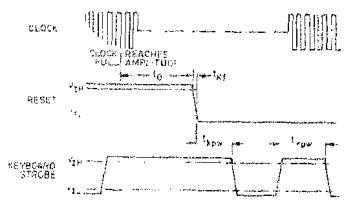


Fig.3 Line, Muting and Strobe Output Timing

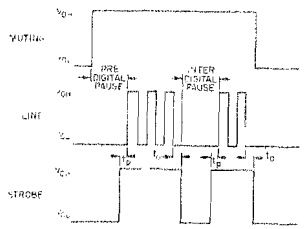
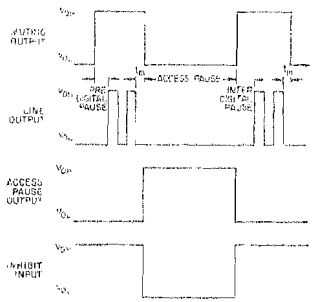


Fig.4 Line, Muting and Access Pause Output Timing



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{cc})	20V to +0.3V
Storage temperature	−65°C to +150°C
Operating temperature	−25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

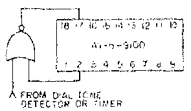
Standard Conditions (unless otherwise noted)
V_{ss} = 0V T = −25°C to +70°C
Negative logic conventions are followed for this data sheet.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig 1)						
Logic '1'	$V_{\phi 1}$	−13.5	—	16.5	V	
Logic '0'	$V_{\phi 0}$	+0.3	-	1.0	V	Match clocks within 0.5V
Frequency	f	10	18	30	KHz	See Note 2
Capacitance	C_{ϕ}	—	90	150	pF	Each clock input, V_{ss} = 0V, f = 1MHz
Rise Time	t_r	1	-	8	μs	
Fall Time	t_f	1	—	4	μs	
Leakage	$I_{\phi L}$	—	—	30	μA	$V_{\phi H}$ = 16.5, T = −55°C
Pulse Width	$t_{\phi w}$	5	—	40	μs	
Pulse Separation	$t_{\phi s}$	5	—	40	μs	
All Outputs (Note 3)						
On Resistance (Logic '0')	R_{on}	—	—	1	KΩ	V_{out} = +1 volt
Off Leakage (Logic '1')	I_{off}	—	-	10	μA	V_{off} = −10V, T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_D	—	—	3	ms	
Line-Strobe Delay	t_D	33	-	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_D increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.2, 4)						
Line-Muting Delay	t_{MD}	33	—	—	ms	MARK/SPACE = 66 2/3–33 1/3 (t_{MD} increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IH}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	-	−1.0	V	
Leakage	I_{IL}	—	—	1	μA	V_{IH} = −16.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	—	—	10	μs	
Capacitance	C_I	—	-	5	pF	V_I = 0V, F = 1MHz
Keyboard Strobe Input (See Fig 2)						
Pulse Width	t_{KPW}	10	—	-	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig 2)						
Logic '1'	V_{IH}	−4.0	—	−16.5	V	
Logic '0'	V_{IH}	+0.3	—	−1.0	V	
Leakage	I_{IL}	—	—	1	μA	V_{IH} = −16.5, T_A = 25°C
Capacitance	C_I	—	—	5	pF	V_{IH} = 0V, f = 1MHz
Fall Time	t_{RI}	3	—	100	μs	
Delay Time	t_D	3	-	-	ms	After clocks reach full amplitude
Power	—	—	0.9	2	mW	V_{cc} = 16.5V

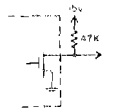
**Typical values are at +25°C and nominal voltages

NOTES 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18KHz
3. Outputs require external pull-down resistors (47KΩ typical)

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE



7A

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS})	−20V to +0.3V
Storage temperature	−65°C to +150°C
Operating temperature	25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = 0V T_A = +25°C

Negative logic conventions are followed for this data sheet

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	V_{ϕ_H}	−4.0	–	−8.5	V	
Logic '0'	$V_{\phi_{IH}}$	+0.3	–	−0.2	V	Match clocks within 0.05V
Frequency	f	8	9	20	KHz	See Note 2
Capacitance	C_ϕ	–	90	120	pF	Each clock input, V_ϕ=0V, f = 1MHz
Rise Time	t_r	1	–	8	µs	
Fall Time	t_f	1		4	µs	
Leakage	$I_{\phi\phi}$	–	–	10	µA	V_{IH} = −8.5V, T_A = +80°C
Pulse Width	$t_{\phi PW}$	5	–	40	µs	
Pulse Separation	$t_{\phi\phi}$	5	–	40	µs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OH}	0.1	–	–	mA	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	–	–	10	µA	V_{OH} = −8.5V T_A = 25°C
Line Output (See Fig. 3)						
Strobe-Line Delay (Note 4)	t_s	–		6	ms	
Line-Strobe Delay (Note 4)	t_o	66	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig.3, 4)						
Line-Muting Delay (Note 4)	t_m	66	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IH}	−2.0	–	−8.5	V	
Logic '0'	V_{IH}	+0.3	–	−0.2	V	
Leakage	I_{IH}	–	–	1	µA	V_{IH} = −8.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	–	–	10	µs	
Capacitance	C_I	–	–	5	pF	V_{IH} = 0V, F = 1MHz
Keyboard Strobe Input (See Fig.2)						
Pulse Width (Note 4)	t_{KPW}	20	–	–	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig 2)						
Logic '1'	V_{IH}	−2.0	–	−8.5	V	
Logic '0'	V_{IH}	+0.3	–	−0.2	V	
Leakage	I_{IH}	–	–	1	µA	V_{IH} = −8.5, T_A = 25°C
Capacitance	C_I	–	–	5	pF	V_{IH} = 0V, f = 1MHz
Fall Time	t_{RF}	–	–	100	µs	
Delay Time (Note 4)	t_D	6	–	–	ms	After clocks reach full amplitude
Power	–	–	0.12	–	mW	V_ϕ = 8.5V, f = 9KHz
	–	–	0.24	–	mW	V_ϕ = 8.5V, f = 18KHz

**Typical values are at +25°C and nominal voltages.

NOTES 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 9KHz

3. Outputs require external pull-down resistors (47K Ω typical)

4. These times will be halved for 18KHz operation

ACCESS PAUSE OPERATION

TYPICAL OUTPUT INTERFACE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS})	−20V to +0.3V
Storage temperature	−65°C to +150°C
Operating temperature	25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = 0V T_A = +25°C

Negative logic conventions are followed for this data sheet

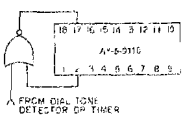
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig.1)						
Logic '1'	V_{ϕ_H}	−10	−13	−16.5	V	
Logic '0'	$V_{\phi_{IH}}$	+0.3	–	−1.0	V	Match clocks within 0.8V
Frequency	f	10	15	30	KHz	See Note 2
Capacitance	C_ϕ	–	90	150	pF	Each clock input, V_ϕ=0V, f = 1MHz
Rise Time	t_r	1	–	8	µs	
Fall Time	t_f	1	–	4	µs	
Leakage	$I_{\phi\phi}$	–	–	90	µA	$V_{\phi IH}$ = −16.5, T_A = +80°C
Pulse Width	$t_{\phi PW}$	5	–	40	µs	
Pulse Separation	$t_{\phi\phi}$	5	–	40	µs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OH}	0.25	–	–	mA	V_{OH} = −1 volt
Off Leakage (Logic '1')	I_{LL}	–	–	10	µA	V_{OH} = −10V T_A = 25°C
Line Output (See Fig.3)						
Strobe-Line Delay	t_s	–	–	3	ms	
Line-Strobe Delay	t_o	33	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_o increases for other MARK/SPACE RATIOS)
Muting Output (See Fig 3, 4)						
Line-Muting Delay	t_m	33	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_m increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IH}	−4.0	–	−16.5	V	
Logic '0'	V_{IH}	+0.3	–	−1.0	V	
Leakage	I_{IH}	–	–	1	µA	V_{IH} = −16.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	–	–	10	µs	
Capacitance	C_I	–	–	5	pF	V_{IH} = 0V, F = 1MHz
Keyboard Strobe Input (See Fig 2)						
Pulse Width	t_{KPW}	10	–	–	ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig.2)						
Logic '1'	V_{IH}	−4.0	–	−16.5	V	
Logic '0'	V_{IH}	+0.3	–	−0.5	V	
Leakage	I_{IH}	–	–	1	µA	V_{IH} = −16.5, T_A = 25°C
Capacitance	C_I	–	–	5	pF	V_{IH} = 0V, f = 1MHz
Fall Time	t_{RF}	3	–	100	µs	
Delay Time	t_D	3	–	–	ms	After clocks reach full amplitude
Power	–	–	0.7	2	mW	V_ϕ = −16.5V

**Typical values are at +25°C and nominal voltages

NOTES 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18 KHz.

3. Outputs require external pull-down resistors (47K Ω typical).

ACCESS PAUSE OPERATION



TYPICAL OUTPUT INTERFACE

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Input Voltages (with respect to V_{SS})	20V to +0.3V
Storage temperature	-65°C to +150°C
Operating temperature	-25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V T_A = -25°C to +70°C

Negative logic conventions are followed for this data sheet

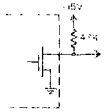
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
Clocks (see Fig. 1)						
Logic '1'	$V_{\phi 1}$	-3.8	–	-8.5	V	
Logic '0'	$V_{\phi 0}$	+0.3		-0.2	V	Match clocks within 0.5V
Frequency	f	15	18	21	KHz	See Note 2
Capacitance	C_{ϕ}	–	90	150	pF	Each clock input, V_{ϕ} = 0V, f = 1MHz
Rise Time	t_r	–	–	6	µs	
Fall Time	t_f	–	–	4	µs	
Leakage	$I_{\phi L}$	–		10	µA	V_{ϕ} = -8.5, T_A = +80°C
Pulse Width	$t_{\phi w}$	10		40	µs	
Pulse Separation	$t_{\phi s}$	5	–	40	µs	
All Outputs (Note 3)						
Output Current (Logic '0')	I_{OL}	0.1	–	–	mA	V_{out} = 1 volt
Off Leakage (Logic '1')	I_L	–	–	10	µA	V_{out} = -8.5, T_A = 25°C
Line Output (See Fig. 3)						
Strobe-Line Delay	t_D	–	–	3	ms	
Line-Strobe Delay	t_C	33	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_C increases for other MARK/SPACE RATIOS)
Muting Output (See Fig. 3, 4)						
Line-Muting Delay	t_M	33	–	–	ms	MARK/SPACE = 66 2/3–33 1/3 (t_M increases for other MARK/SPACE RATIOS)
All Inputs (Except Reset)						
Logic '1'	V_{IH}	-2.0		-8.5	V	
Logic '0'	V_{IL}	+0.3		-0.2	V	
Leakage	I_{IL}	–	–	1	µA	V_{IH} = -8.5, T_A = 25°C
Rise and Fall Time	t_r, t_f	–	–	10	µs	
Capacitance	C_I	–	–	5	pF	V_{IH} = 0V, f = 1MHz
Keyboard Strobe Input (See Fig. 2)						
Pulse Width	t_{KEY}	10			ms	Effective only when RESET input is at Logic '1'
Reset Input (See Fig. 2)						
Logic '1'	V_{IH}	-2.0	–	-8.5	V	
Logic '0'	V_{IL}	+0.3	–	-0.2	V	
Leakage	I_{IL}	–		1	µA	V_{IH} = -8.5V, T_A = 25°C
Capacitance	C_I	–		5	pF	V_{IH} = 0V, f = 1MHz
Fall Time	t_{RF}	3	–	100	µs	
Delay Time	t_R	3	–	–	ms	After clocks reach full amplitude
Power	–	–	0.24	–	mW	V_{SS} = -8.5V

** Typical values are at +25°C and nominal voltages

NOTES 2. Line Pulse Rate depends upon frequency of clock input. Standard clock frequency is 18 KHz

3. Outputs require external pull-down resistors (47K Ω typical)

TYPICAL OUTPUT INTERFACE



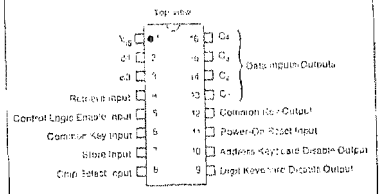
Repertory Dialler

FEATURES

- Stores 10 x 22 digit telephone numbers, including access pauses
- Devices can be 'stacked' to give a store expandable in blocks of 10 numbers.
- Operates in conjunction with the AY-5-9100 Push-Button Dialler
- Single or Dual Keyboard operation
- Interfaces to standard MF Tone Dialler Keyboards
- Applications in Repertory Diallers and Security Systems.
- Will operate MF Tone Diallers such as the AY-3-9400
- Low power consumption, typically 2.25mW

PIN CONFIGURATION

16 LEAD DUAL IN LINE



DESCRIPTION

The AY-5-9200 is a 10 number store designed to work in conjunction with the AY-5-9100 Push Button Telephone circuit to form a Repertory Dialler, each of the 10 numbers containing up to 22 digits or access pauses.

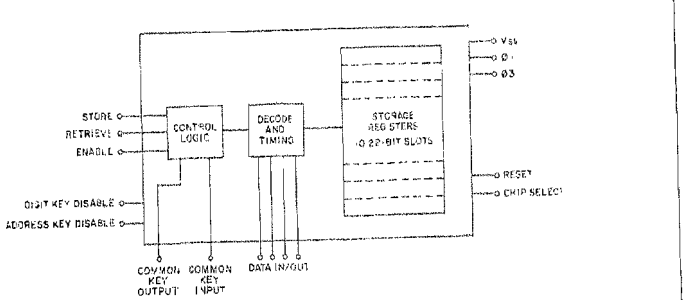
The keyboard, AY-5-9100 and as many AY-5-9200's as required are all connected to a 4 line data bus. Numbers for direct dialling are routed to the AY-5-9100, numbers to be stored go straight to the AY-5-9200. Numbers that are being retrieved are transmitted from the AY-5-9200 to the AY-5-9100 while control outputs from the AY-5-9200 determine the routing of the data.

The system may operate either with a single 12 button keyboard, which is used for both address and digit entry, or with separate address and digit keyboards. Single keyboard operation would normally be employed in a 10 number Repertory Dialling telephone. Dual keyboard operation is usual for 10 to 100 number Repertory Diallers.

The AY-5-9200 may also be used in MF tone dialling systems, the output data rate being directly compatible.

Four phase logic is used to achieve minimum power consumption, the circuits being manufactured using the MTNS P-channel silicon gate MOS process.

BLOCK DIAGRAM



Pin.No.	Name	Function
1	V_{SS}	This is the ground and substrate connection and is used as a reference for all the electrical parameters
2-3	Clocks $\phi 1$, $\phi 3$	These inputs form the two supply clocks, and alternate negative-going pulses are required. These are described in the Electrical Characteristics and fig. 1. Any deviation from the nominal 18KHz will result in a proportional modification of the on-chip timings.
4	Retrieve Input	The retrieve input must be taken to a logic '1' for at least 10ms to indicate when a retrieve operation is to be performed. Anti-bounce logic is provided on this input
5	Control Logic Enable Input	This input must be taken to a logic "1" for the duration of any store or retrieve operation. The control logic is reset when the input returns to logic '0'. Anti-bounce is provided for this input
6	Common Key Input	This input is taken from the common contact on all keyboards. A '1' to '0' transition will indicate a key closure. Anti-bounce is provided to ensure only a single depression is read
7	Store Input	This input must be taken to a logic '1' for the duration of any store operation. Anti-bounce logic is provided for both logic transitions.
8	Chip Select Input	When at logic '0' all inputs and outputs (except for Common Key input and output) are inhibited. It may be permanently wired to logic '1' if only one AY-5-9200 is used in the system
9	Digit Keyboard Disable Output	The digit keyboard must be disabled while information is being transferred from the Store chip to the Push Button Dialler during a Retrieve operation. This output goes to a logic '0' during this period. In a single keyboard system this output is the one to be used.
10	Address Keyboard Disable Output	The address keyboard is to be disabled, both during a Retrieve operation when information is being transferred between chips and during the Store operation after an address has been allocated, until the Store operation is finished. This output goes to a logic '0' during these periods
11	Power-On-Reset Input	An initial reset is required for clearing the chip when power is initially applied. This input must be held at a logic '0' initially, going to a logic '1' to activate the chips
12	Common Key Output	This output is fed directly to the Common Key input of the associated AY-5-9100 Push Button Dialler and goes to a logic '0' to indicate a valid code signal. It controls the routing of data into the AY-5-9100. (See Function Description for further details.)
13-16	C_1 C_2 C_3 C_4	Data Input/Outputs. These four lines are connected to the system. Address and dialled digit information is input on these pins and dialling information is fed out from these pins to the Push-button Dialler. The standard keyboard code accepted by the AY-5-9200 is shown below. When outputting information, the output is normally at a logic '1' and goes to a logic '0' for a data bit

NOTE
Chip Select, Retrieve, Control Logic Enable and an address can all be applied simultaneously to the Store Chip. Also Store and Control Logic Enable signals can be applied simultaneously.

KEYBOARD CODE

Digit	No. of Impulses	Code			
		C_1	C_2	C_3	C_4
1	1	1	1	1	1
2	2	1	1	1	0
3	3	1	1	0	1
4	4	1	1	0	0
5	5	1	0	1	1
6	6	1	0	1	0
7	7	1	0	0	1
8	8	0	1	1	1
9	9	0	1	1	0
0	10	1	1	0	1
Access Pause		0	0	1	1

FUNCTION DESCRIPTION

The following description applies to a Push Button Repertory Dialler using the AY-5-9100 and AY-5-9200 circuits. The system provides normal push button telephone facilities with access pause and redialling, together with a repertory dialling store expandable in blocks of 10 numbers.

The AY-5-9100 is a standard Push Button Dialler circuit with normal dialling and redialling facilities. It also has the capability of storing access pauses and waiting until a dial tone is detected by external circuitry before dialling is recommenced. This chip can operate by itself when a storage facility is not required. A detailed description of this device is contained in the AY-5-9100 data sheet.

The AY-5-9200 contains all the control logic and store facility required to store ten telephone numbers. Each number may be up to 22 characters in length, each character being either a digit or access pause; a dynamic memory technique being used for the data storage. Digits, access pauses and memory addresses are entered into the AY-5-9200 as 4-bit codes on 4 input/output pins which are also connected to the digit input pins of the AY-5-9100 as in Figs. 4 and 5. While data is being transferred between the AY-5-9200 and the AY-5-9100, the keyboards are externally disabled by signals generated by the AY-5-9200, so that further key depressions have no effect until the transfer of data has been completed. Further address inputs are inhibited until the call is terminated.

The digit keyboard common key output is routed through the control logic and depending on the state of the logic, the Common Key output to the Push Button Dialler chip is enabled or disabled. This prevents digits to be stored and memory addresses from entering the Push Button Dialler.

The Common Key output from the AY-5-9200 is controlled as follows:

	C.S.	C.L.E.	
Logic Level	'0'	'0'	Common output is a direct replica of Common input and digits are dialled directly by the AY-5-9100
Logic Level	'1'	'1'	Common signals to the Push Button Dialler are generated only as a number is being retrieved (see Fig. 3). After a retrieve operation. Common signals are gated through, allowing further dialling unless externally inhibited
Logic Level	'0'	'1'	No Common signals are generated and the output device goes off

The control logic operates so that the first key depression at the beginning of an operation determines the subsequent sequence. Invalid key depressions at a later stage in a sequence are then ignored by the control logic.

The system is expanded by connecting further AY-5-9200 chips to the busses and using the Chip Select input to enable the required chip.

When a separate address keyboard is to be used an address keyboard strobe can be fed to the 'Retrieve' input, thus allowing a single button depression when retrieving a number from the store.

OPERATION MODES

1. STORE OPERATION

DEPRESS STORE
This sets the logic into a store mode. This signal must be present throughout the store operation. Thus, either electrical or mechanical bistable switching is required, or the 'Store' button must remain depressed during the sequence. The Control Logic Enable and Chip Select inputs should be activated at the same time. The Common Key output is inhibited and the address and digit codes are routed into the AY-5-9200 chip. The order of application of the signals is not important, they may be applied simultaneously with Address if required.

DEPRESS ADDRESS (one digit)
The address code, if valid, is latched and the memory location associated with this address is cleared to prevent corrupting the new number with old information. The Common Key output remains disabled. The Address Keyboard is also disabled for the remainder of the Store operation.

ENTER NUMBER DIGITS (and Access Pauses)
The number to be stored is then entered using the digit keyboard and is stored in the addressed location. The maximum allowable number of digits or access pauses is 22. Chip select must be at logic '1' during digit entry.

RELEASE STORE, CONTROL LOGIC ENABLE AND CHIP SELECT
This is accomplished by re-setting the electrical or mechanical bistable or releasing the Store button. The control logic is then reset and disabled.

2. RETRIEVE OPERATION

DEPRESS RETRIEVE
For separate address keyboard systems this signal can be generated automatically with the address. The control logic is set to a retrieve mode and the address inputs are enabled. Control Logic Enable and Chip Select must be at logic '1' for the whole of the Retrieve operation, including the data transfer period. The Retrieve input must be returned to logic '0' before the end of data transfer to prevent a repeat operation.

DEPRESS ADDRESS (Digit)
The address is decoded and latched, both keyboard disable outputs go active, disabling the keyboards. After a minimum period of 60mS, the first digit code is transmitted to the Push Button Dial chip together with a Common signal. The Common is stable for a minimum period of 60mS, the Common only being present while the code is stable. The data transmission continues at 60mS on, 60mS off until the whole number has been transferred, after which the chip is reset, the keyboard disable signals are removed and the Common signal is enabled to the Push Button Dialler chip. (See Fig. 3.)

3. ERASE OPERATION

This operation is basically a Store operation with no digits being input.

DEPRESS STORE
This sets up the logic as in the Store operation.

DEPRESS ADDRESS (Digit)
This then clears the decoded address.

RELEASE STORE
This is accomplished either by releasing 'Store' input, or re-setting the mechanical or electrical 'Store' bistable.

4. RECALL AND NORMAL DIALLING

These are performed as for the Push Button Dialler on its own. See AY-5-9100 data sheet for full description.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS}	−20V to +0.3V
Storage temperature range	−65°C to +150°C
Ambient operating temperature range	−55°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS}=0V

V_{Φ}=−15±1.5V (see fig. 1 for waveform)
Clock frequency=16 KHz
Operating Temperature (T_A)=−55°C to +80°C
Negative logic conventions are followed for this data sheet.

Characteristic	Min.	Typ.**	Max.	Units	Conditions
Clock					
Logic '0' level	+0.3	—	−1	Volts	Note 1
Logic '1' level	−13.5	—	−16.5	Volts	
Frequency	10	16	30	KHz	
Rise Time (Tr)	0.1	—	4	μs	
Fall Time (Tf)	0.1	—	8	μs	
Width (Tw)	5	—	40	μs	At logic '1' min. level
Separation (Ts)	5	—	40	μs	At logic '0' max. level
Capacitance	—	70		pF	Per phase V_{Φ}=0V, f=1MHz (Note 2)
Leakage	—	—	10	μA	V_{Φ}=−16.5V, T_A=25°C
Inputs					
Logic '0' level	+0.3	—	−1	Volts	
Logic '1' level	−5	—	−16.5	Volts	
Capacitance	—	—	5	pF	V_{IN}=0V, f=1MHz
Leakage	—	—	1	μA	V_{IN}=−16.5V, T_A=25°C
Common Key Input					
Pulse Width (Tc)	10	—	—	ms	At logic '0' max. level see fig. 2
Reset Input					
Pluse Width (Td)	3	—		ms	After clocks reach full amplitude
Fall Time (Te)	—	—	100	μs	Fig.2
Anti-bounce on all Inputs except Chip Select & Reset	4.2	—	—	ms	
Outputs					
All outputs including C_1 to C_4 when acting as outputs					
Logic '0' output current	0.6	—	—	mA	V_0=−1V
Logic '1' output leakage	—	—	10	μA	V_0=−10V
Digit Output Rate	—	8.35	—	Hz	
Power	—	2.25	—	mW	

**Typical values are at +25°C and nominal voltages

NOTES:
1. Clock logic '0' levels should be within 0.5V of each other.
2. The effective dynamic clock capacitance while operating is 260pF

TIMING DIAGRAMS

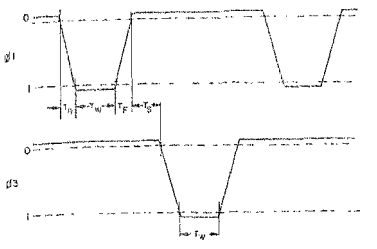


Fig.1 CLOCK WAVEFORMS

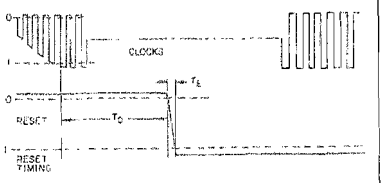


Fig.2 CLOCK WAVEFORMS WITH RESET TIMING

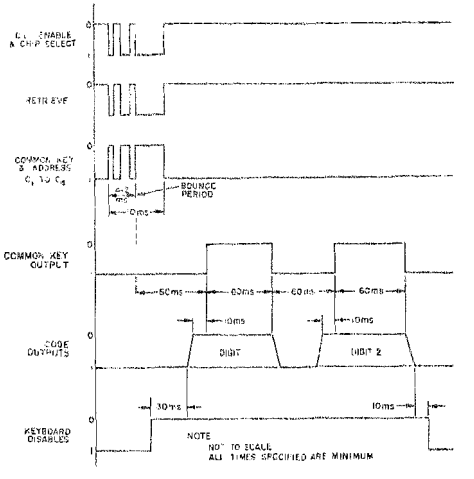


Fig.3 "RETRIEVE" WAVEFORMS

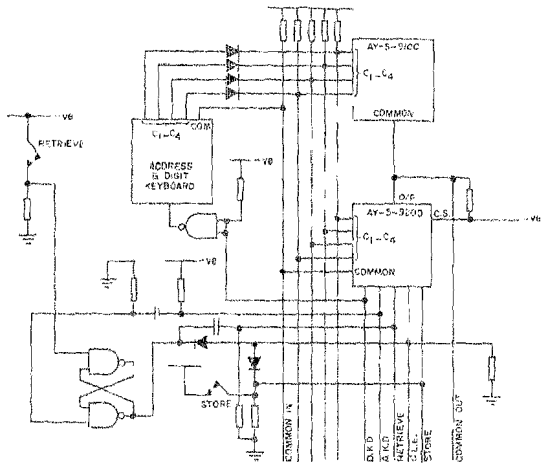


Fig.4 SINGLE KEYBOARD SYSTEM FOR REPERTORY DIALLER

Note for Figs.4 and 5
Logic CD4011A (C-MOS)
Resistors 100K
Capacitors 0.1uF
Diodes 1N914

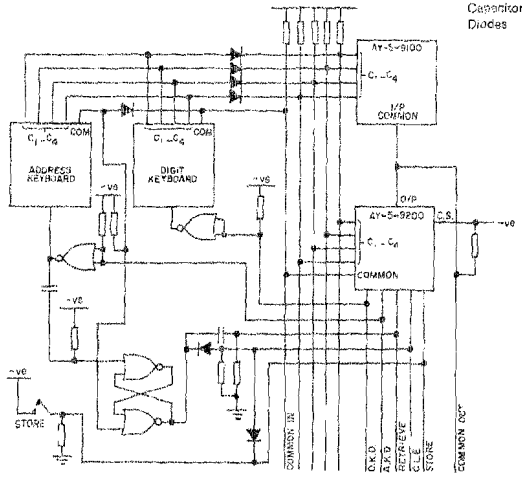


Fig.5 DUAL KEYBOARD SYSTEM FOR REPERTORY DIALLER

Telephone Coinbox Circuit

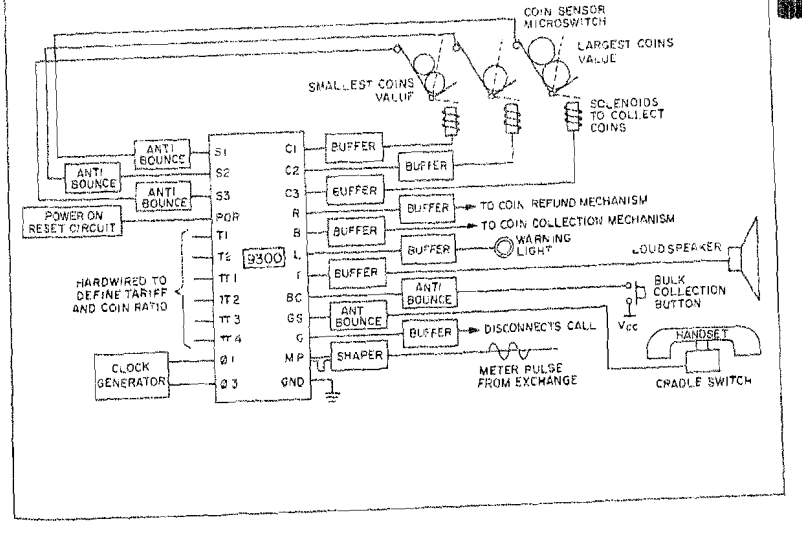
FEATURES

- Up to three coin denominations recognized
- 16 coin value ratios selectable.
- 9 tariff rates selectable
- Tone outputs for switch-on, coin input, bulk collect, last pay period, cut-off.
- Lamp outputs for last coin and last pay period

DESCRIPTION

The AY-5-9300 is a P-Channel MOS integrated circuit designed to control the operation of a standard coinbox telephone. The device registers the insertion of coins and automatically debits the sum when a meter pulse is received. Lamp and tone signals are provided to inform the user and the exchange of the progress of the call. The use of four-phase dynamic logic provides very low power dissipation (2mW typical). The AY-5-9300 is offered in a 24 pin dual-in-line package

BLOCK DIAGRAM



7A

Dual Tone Multi-Frequency Generators

FEATURES

- No tuning required, inherent accuracy ± 0.25%
- Uses low cost ceramic resonator
- 12 tone pairs (16 tone pairs with AY-3-9401/9410 and choice of high group pre-emphasis with AY-3-9410)
- Total harmonic distortion less than 8% (but dependent on external filter)
- Instant generation of tone outputs
- Low voltage drop
- Low power consumption (less than 35mW)
- Good thermal and voltage stability
- Keyboard lock out inhibits output if more than one key depressed
- N-channel ion implant construction
- High group pre-emphasis fixed at 3.52dB (AY-3-9400), 2dB (AY-3-9401), 3/5dB (AY-3-9410)
- Pre-emphasis can be varied by simple component adjustment

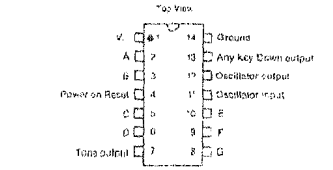
DESCRIPTION

The AY-3-9400/9401/9410 DTMF circuits generate all the tone pairs required for multifrequency tone dialing. The tones are generated from a single ceramic controlled master oscillator, ensuring high accuracy and stability of the output frequencies and eliminating the need for any adjustments. The digitally synthesised tones give precisely controlled characteristics.

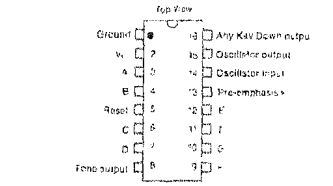
The AY-3-9400/9401/9410 is fabricated using the ion implant N-channel low voltage process, and employs novel logic techniques to minimize power consumption and voltage drops. The circuit is suitable for operation direct from telephone line power, or it can be used with main power or battery supplies.

PIN CONFIGURATION

14 LEAD DUAL IN LINE
AY-3-9400

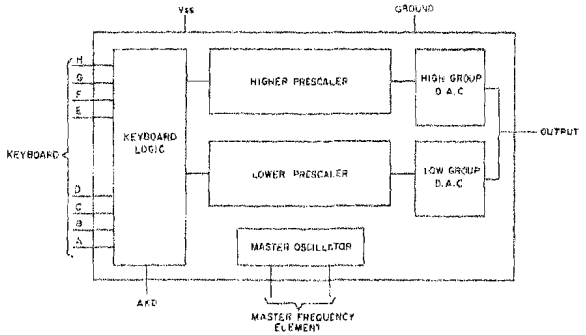


16 LEAD DUAL IN LINE
AY-3-9401/AY-3-9410



* 2dB on AY-3-9401, 3dB8 on AY-3-9410

BLOCK DIAGRAM



AY-3-9401/9410

OPERATION

When a key is pressed the chip will immediately start operating, the output tones both starting from zero on the first negative half cycle. The first cycle will be of full amplitude assuming the power supply is at the correct level. If power is applied at the same time as a key is pressed, the power on reset circuit will operate, preventing spurious outputs.

When two or more keys are pressed together, one or both tones will be switched off. The tones will start from zero as soon as the extra keys have been released. When all keys are released, the tone outputs will immediately cease.

If only one key contact is made, a single tone corresponding to the closed contact will be output. The "Any Key Down" output goes to logic '0' as soon as a key depression is recognized.

The tones are output on a single pin, as a mixture of pulse width modulated constant amplitude square waves. This output signal is constructed into resultant sine waves in the external low pass filter. The approximation chosen yields a total harmonic distortion of less than 8%.

The amplitude of the output signal is directly proportional to the V_{cc} supply voltage.

A low pass filter buffer amplifier is used to remove switching noise and interface the tones to the line. There is an option of either a low impedance or a high impedance output (see figs. 1a and 1b).

NOTES

1. Pre-emphasis selection for the AY-3-9401: Connect pin 13 to ground for 2dB pre-emphasis. Pre-emphasis selection for the AY-3-9410: Connect pin 13 to Vcc for 3dB high group pre-emphasis, or to ground for 6dB pre-emphasis. The circuits are otherwise identical in operation to the AY-3-9400.
2. See MEO2 specification for the resonator.

PERIPHERAL CIRCUITS

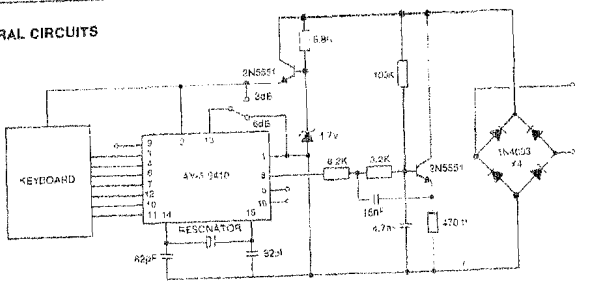


Fig.1a HIGH IMPEDANCE BUFFER

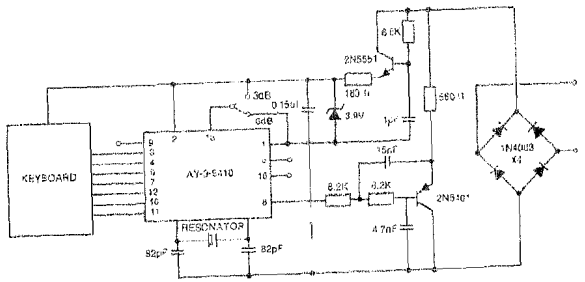


Fig.1b LOW IMPEDANCE BUFFER

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to ground pin	+10V to −0.3V
Storage temperature range	−55°C to +150°C
Ambient operating temperature range	−25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{CC} = +3.5 to +8V
Fclock = 559.7KHz
Operating Temperature (T_A) −25°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Input Logic '1'	+3.3	—	+8	Volts	logic '1' activates tone
Input Logic '0'	−0.3	—	+0.4	Volts	
Input pull down resistance	20	—	100	Kohm	resistor to ground
Input capacitance	—	—	10	pF	
Tone output Low Group	—	0.553	—	Vrms	V_{CC} = 4V, Note 1, Note 3
Tone output High Group	—	0.783	—	Vrms	V_{CC} = 4V, Note 1, Note 3
High group pre-emphasis	—	3.52	—	dB	1.6dB typ. for AY-3-9401.
Output impedance	—	—	500	ohms	Note 2, Note 3
Any Key Down output					
On resistance	—	—	1	Kohm	Vout = +1V
Off Leakage	—	—	10	µA	Vout = +8V
Total Distortion	—	—	−25	dB	
Harmonic component	—	—	−30	dB	
Supply current	—	—	8	mA	V_{CC} = +3.5V
	—	—	10	mA	V_{CC} = +8V

**Typical values are at +25°C and nominal voltages

NOTE
1. The amplitudes of the output signals are directly related to the V_{CC} supply voltage
2. The chip output is intended to drive a low pass filter having an input impedance of greater than 8K ohms.
3. The output would be buffered to drive the line, the buffer can be arranged to have either a high impedance current output or a low impedance voltage output (See Figs.1a and 1b)

FREQUENCY OUTPUTS

All output frequencies are derived from a 559.7KHz master oscillator.
The output frequencies are as follows

	Nominal frequency Hz	Actual Frequency Hz	Error %	Key
Low Group	697	695.28	−0.25	A
	770	768.82	−0.15	B
	852	850.61	−0.16	C
	941	940.68	−0.03	D
High Group	1209	1211.48	+0.21	E
	1336	1332.62	−0.25	F
	1477	1478.69	+0.25	G
	1633	1631.78	−0.07	H

TYPICAL CHARACTERISTIC CURVES

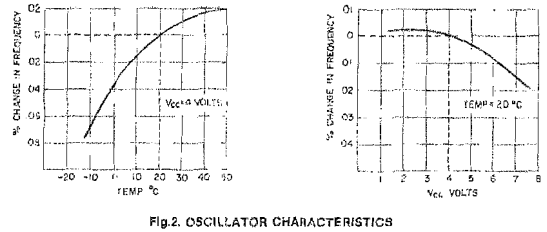


Fig.2. OSCILLATOR CHARACTERISTICS

AY-5-9500

C-MOS Clock Generator

FEATURES

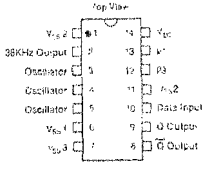
- Generates 2 phase clock from single power supply
- Operates with AY-5-9100 Push Button Dialler and AY-5-9200 Repertory Dialler
- Very Low power consumption, allowing use of line powered telephones
- Minimizes external components in Push Button Telephones
- Stable generation of clock frequencies

DESCRIPTION

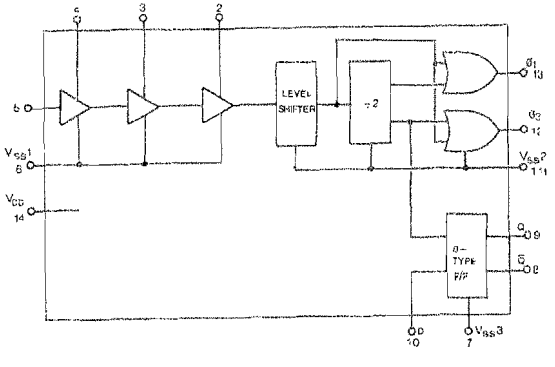
The AY-5-9500 is a C-MOS circuit designed to generate the 2 phase clock required by the AY-5-9100 Push Button Telephone chip and the AY-5-9200 Repertory Dialler circuit

It consists of an RC oscillator, a level shifter, a 2 phase clock generator and driver, and a clocked D-type bistable. The RC oscillator is set by external components to run at 36KHz and is normally operated from a 4 Volt supply to minimize power consumption. The oscillator output is shifted and used to drive the 2 phase clock generator which is normally run on a 14 Volt supply. The D-type bistable is either used as a Reset generator for the AY-5-9100, or it is used to drive a Cockroft-Walton voltage multiplier to generate the 14 Volt supply

PIN CONFIGURATION
14 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{DD} pin	−18V to +0.3V
Storage temperature range	−65°C to +150°C
Ambient operating temperature range	−25°C to +70°C

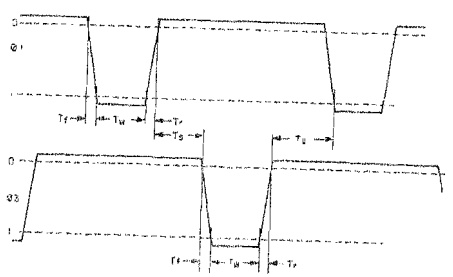
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

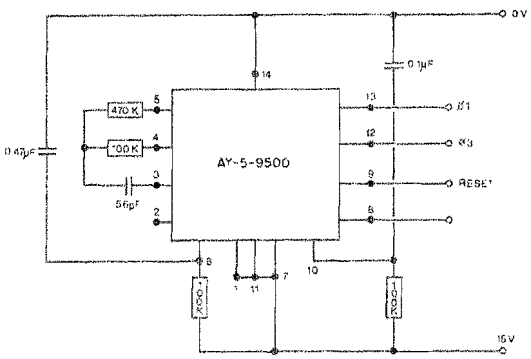
Standard Conditions (unless otherwise noted)

V_{DD} = 0V
$V_{SS}1$ = −4 to −15V
$V_{SS}2$ = −4 to −15V
$V_{SS}3$ = −4 to −15V
F Clock = 36KHz ± 10%
Operating Temperature (T_A) = +25°C

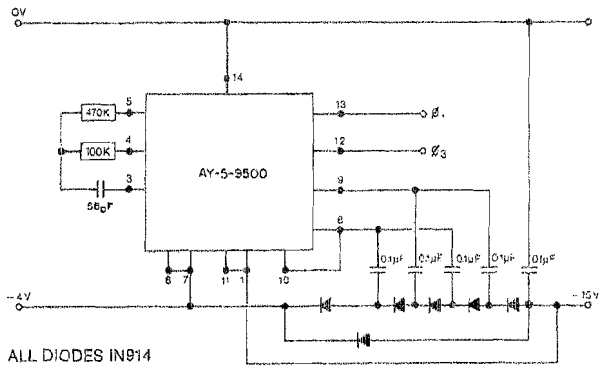
Parameter	Min	Typ	Max	Units	Conditions
CLOCK OUTPUTS					
Rise Time (Tr)	—	90	200	ns	At 360pF load
Fall Time (Tf)	—	120	250	ns	At 360pF load
Width (Tw)	10	—	—	µs	At 36KH$_z$
Separation (Ts)	10	—	—	µs	At 36KH$_z$
Stability	—	—	±5	%	With supply and temperature
OUTPUT 'ON' RESISTANCE					
Ø1, Ø3	—	0.3	2	KOhm	$V_{SS}2$ = −4V
Q, $\overline{Q}$	—	200	750	Ohm	$V_{SS}3$ = −4V
SUPPLY CURRENT					
$I_{SS}1$	—	130	200	µA	$V_{SS}1$ = −4V
$I_{SS}2$	—	100	200	µA	$V_{SS}2$ = −15V, 10pF load
$I_{SS}3$	—	30	50	µA	$V_{SS}3$ = −15V

TIMING DIAGRAM





SINGLE SUPPLY OPERATION



DC-DC CONVERTOR CONNECTION

Dual Tone Multi-Frequency Receivers

FEATURES

- No tuning required; inherent discrimination better than ±0.1%
- Digitally defined bandwidths with no inherent voltage or temperature drift
- Acquisition time typically 25 ms (tone inputs to common output).
- Frequency correlation provides good S/N performance.
- Inter-tone separation checked for correct IDP period.
- Many programmable features provide wide applications
- High reliability and low cost using P-channel process
- On-chip analog amplifiers for analog preprocessing
- Interfaces directly with the AY-5-9100 for M.F.—Stronger converters (AY-5-9801/9805)
- Handshaking facility to interface directly with CP1600 microprocessor
- Three-State code outputs.

AY-5-9800 SERIES

Part Number*	Output Code	On-Chip OP Amps	Pins
AY-5-9801/9821	4-Bit	Yes	28
AY-5-9802/9822	1 of 16	Yes	40
AY-5-9803/9823	2 of 8	Yes	40
AY-5-9804/9824	Binary	Yes	28
AY-5-9805/9825	4-Bit	No	24
AY-5-9806/9826	1 of 16	No	40
AY-5-9807/9827	2 of 8	No	24
AY-5-9808/9828	Binary	No	24

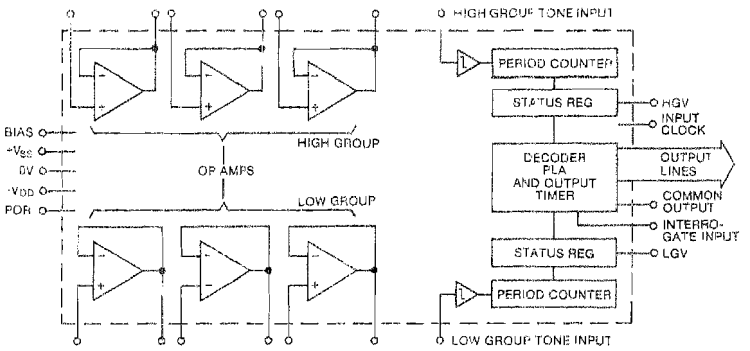
*Part numbers AY-5-9801 through 9808 are supplied in ceramic packages. Part numbers AY-5-9821 through 9828 are supplied in plastic packages.

PROGRAMMABLE OPTIONS

These options can all be provided by a single layer mask change

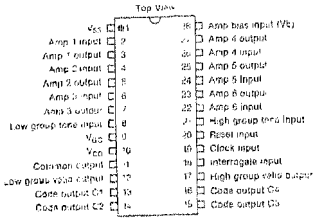
- Programmable center frequencies
- Programmable accuracies
- Variable "Acquire" criteria (1 out of 5 to 5 out of 5)
  Variable "Release" criteria (1 out of 5 to 5 out of 5)
- Normally arranged for 2 of 8 detection, but can be reprogrammed for single tone (1 of 8) detection.
- Common output can be delayed by 1-32 ms after tones are detected valid
  Note: IDP period - common delay = common width.
- Common output pulse can be programmed from 1-31 mS
- Output code can be any 4 bit code in 24/28 lead DIP or any 16-bit code in 40 lead DIP (e.g. 2 of 7, 1 of 12 etc.)

BLOCK DIAGRAM

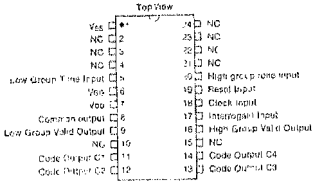


PIN CONFIGURATIONS

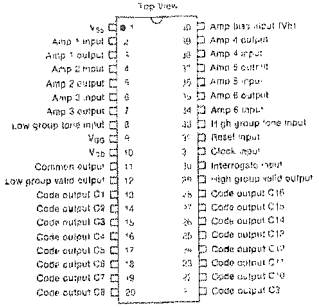
28 LEAD DUAL IN LINE
AY-5-9801/9821
AY-5-9804/9824



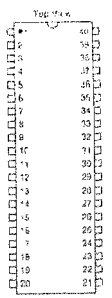
24 LEAD DUAL IN LINE
AY-5-9805/9825
AY-5-9808/9828



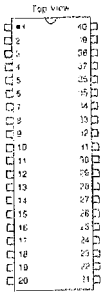
40 LEAD DUAL IN LINE
AY-5-9802/9822



40 LEAD DUAL IN LINE
AY-5-9806/9826
Not yet defined



40 LEAD DUAL IN LINE
AY-5-9803/9823
Not yet defined



24 LEAD DUAL IN LINE
AY-5-9807/9827
Not yet defined

7A

DESCRIPTION

The AY-5-9600 series circuits are fabricated in P channel MTNS process thus minimizing cost and providing high reliability. The basic chip block diagram is shown on the previous page. For analog preprocessing six amplifiers and two source followers are included on-chip, external components being used to determine the filter characteristics. The major functions are mask programmable thus giving a flexible system at a low cost.

The tone pair is separated into two individual tones using the analog circuitry, the separated tones being applied to the Schmidt triggers to square incoming signals which are then processed by the digital circuitry. The high and low group logic is similar; only the decode values for frequency recognition are different. The incoming signal is divided by two or three to eliminate the effects of changing mark/space ratio and its period counted by a timer which is clocked by the accurate 1MHz clock. If the period value is within encoded limits, the result is stored. Five cycles of incoming signal are stored and a decision is made with this information as to whether the tone is valid. A programmable logic array scans the five cycle store for both an "Acquire" criteria and "Release" criteria. If the "Acquire" criteria is exceeded (e.g. 4 out of 5), and the "Release" criteria is not reached (e.g. less than 2 out of 5), the frequency is deemed to be valid. If both high and low frequencies are detected, a time-out timer is started. This timer is mask programmable and will normally require 25ms of valid tone pair signal. Once this period has elapsed the Common Output pulses high, again for a preprogrammed period. After this pulse, the system will not respond again until an IOP of a preprogrammed duration occurs, after which a new input tone pair can be applied.

The Code Outputs and Common Output can be configured for a wide variety of systems. A typical device, AY-5-9501/9821, provides four Three-State Code outputs suitable for microprocessor controlled systems and direct interfacing to the AY-5-9100 for DTMF-Strowger converters. A handshaking interface is provided using the Interrogate input thus allowing very simple microprocessor interfacing. The outputs will directly drive low power TTL, CMOS or MOS and, being Three-State, can be bussed in large systems.

Input Clock — The recommended clock frequency is 1MHz which will then give a frequency detect range of 620—3400Hz with a discrimination of ± 1μs. The discrimination of 1633Hz using a 1MHz clock will be better than ± 0.1%. Any deviation of the 1MHz clock will result in a proportional deviation of the tone recognition bands.

Power-On-Reset—An external power-on reset is required which is used to reset all counters, etc. An on-chip resistor pulls this input to V_{DD}. a 0.1μF capacitor connected from the P.O.R. input to Vss will provide automatic power-on-reset. This input can be used as a chip select putting all Three-State outputs into their high impedance state when held high.

Input Amplifiers—Input amplifiers are suitable for use in band-pass and general buffer amplifiers. They have an open loop gain of approximately 250 and are trimmed by a single 'Bias Input'.

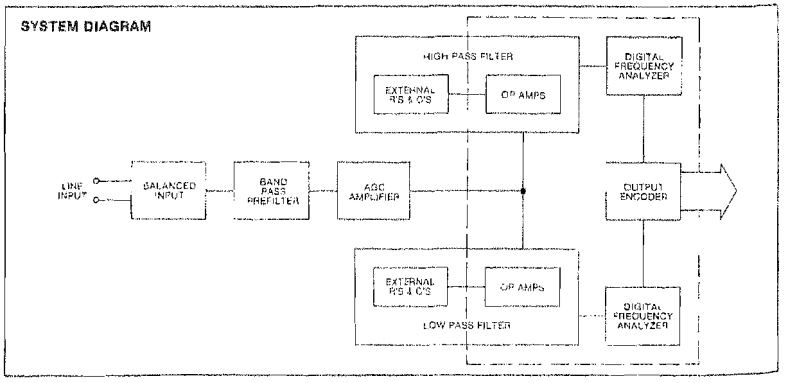
Period Counters—The input frequency is interrogated by the period counter. Each counter has eight values decoded, these representing F0 low limit, F1 high limit, etc. Once a positive going edge is detected, the period counter is started and if the next positive going edge occurs during a time slot decode, the circuit deems the tone to be valid and a bistable indicating the tone decoded is set. Special logic is incorporated to prevent the counter from being continuously triggered in the presence of noise.

Status Word Register—The Status Word Register is a five bit register which is filled with 1's for an in-band signal but filled with 0's for out-of-band signals. With the data in this register a decision is performed which sets a bistable (Acquires the signal) or resets a bistable (Releases the signal). Thus by changing the preprogrammed acceptance standard, a direct trade-off between S/N ratio and stimulation rate can be obtained for different systems.

Output Logic—Two outputs, HGV and LGV, indicate the current state of the correlator for each group. A valid high group frequency, if present for longer than the correlation time, will cause the HGV (high group valid) output to go low. Similarly with the LGV (low group valid) output. Once both high and low group tones have been detected valid, a preprogrammed timer is started. If the tone pair is still valid after the timer has counted out the Common Output goes high for a preprogrammed period and the Code Outputs present the programmed outputs corresponding to the tone pair input.

If the interrogate input is used for handshaking, the Code Outputs are only presented after the Interrogate input goes high, the Interrogate input going low removes both the Codes and the Common Output.

SYSTEM DIAGRAM



OUTPUT CODE CHART

Input Tone Pair		Normal Digit Representation	AY-5-9501/9821 AY-5-9505/9825 Output Code*				AY-5-9502/9822 AY-5-9506/9826 Output Code	AY-5-9503/9823 AY-5-9507/9827 Output Code	AY-5-9504/9824 AY-5-9508/9828 Output Code**			
Low Group (Hz)	High Group (Hz)	C1	C1	C2	C3	C4	1 of 16	2 of 8	C1	C2	C3	C4
697	1209	1	1	1	1	1	C1	C1,C5	1	1	1	0
697	1336	2	1	1	1	0	C2	C1,C6	1	1	0	1
697	1477	3	1	1	0	1	C3	C1,C7	1	1	0	0
697	1633	—	0	0	0	1	C4	C1,C8	0	0	0	1
770	1209	4	1	0	1	1	C5	C2,C5	1	0	1	1
770	1336	5	1	0	1	0	C6	C2,C6	1	0	1	0
770	1477	6	1	0	0	1	C7	C2,C7	1	0	0	1
770	1633	—	0	0	1	0	C8	C2,C8	0	0	1	0
852	1209	7	0	1	1	1	C9	C3,C5	0	1	0	0
852	1336	8	0	1	1	0	C10	C3,C6	0	1	1	1
852	1477	9	0	1	0	1	C11	C3,C7	0	1	1	0
852	1633	—	0	1	0	0	C12	C3,C8	0	1	0	1
941	1209	*	0	0	1	1	C13	C4,C5	0	0	1	1
941	1336	0	1	0	1	0	C14	C4,C6	0	0	1	0
941	1477	#	0	0	0	1	C15	C4,C7	0	0	0	1
941	1633	—	1	0	0	0	C16	C4,C8	1	1	1	1

*Compatible with AY-5-9100 **Compatible with AY-5-9120.

7A

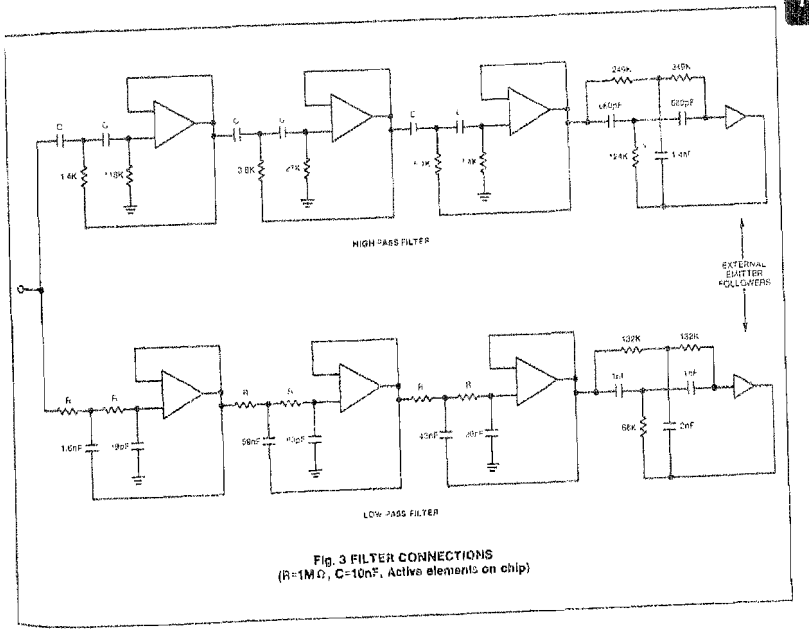


Fig. 3 FILTER CONNECTIONS
(R=1MΩ, C=10nF, Active elements on chip)

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature Range ..... -65°C to +150°C
Ambient operating temperature ..... -25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied -- operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -8.5 ±0.5V
V_{GG} = -17V ±1V
Clock frequency = 1 MHz
Operating Temperature (T_A) = +25°C

Characteristics	Min	Typ	Max	Units	Conditions
Clock					
Logic '0' level	+0.3	—	+1.0	V	
Logic '1' level	-6.5	-8.5	-18	V	
Frequency (see NOTE below)	0.01	1.0	1.1	MHz	
Rise Time	10	—	50	ns	
Fall Time	10	—	50	ns	
Width	450	500	550	ns	
Capacitance	—	—	20	pF	
Leakage	—	—	10	µA	
Logic Inputs					
Logic '0' level	+0.3	—	+1.0	V	
Logic '1' level	-3.7	-5	-18	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	
Logic Outputs					
(i) Code outputs					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	460	—	—	µA	V_O = -5V
(ii) Common output					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	620	—	—	µA	V_O = -5V
Pulse delay	1	—	31	ms	
Pulse width	1	32	32	ms	
(iii) Group valid outputs (HGV & LGV)					
Logic '0' output current	500	—	—	µA	V_O = -1V (External pull-down resistors to V_{DD} required).
Signal Input	.5	—	2	V	Peak to peak sine wave
"Handshake" Routine					
(See Fig. 1 for timing diagram) T1, T2	—	—	2.5	µs	
Pull-down resistor (to V_{DD})	50	150	500	KΩ	
Power-on Reset					
Pull-down resistor (to V_{DD})	50	150	500	KΩ	
Pulse Width	10	—	—	µs	
Amplifiers					
Open loop gain	—	500	—	—	F_{in} = 1KHz
Open loop bandwidth	—	1	—	MHz	
Output impedance	—	—	6	KΩ	F_{in} = 1KHz
Power Dissipation	—	—	350	mW	V_{DD} = -9V V_{GG} = -18V

NOTE: Any deviation from the nominal 1MHz clock frequency will result in a corresponding deviation of the frequency detection bands. Other frequencies than 1MHz clock can be preprogrammed in, but circuit characteristics will be modified.

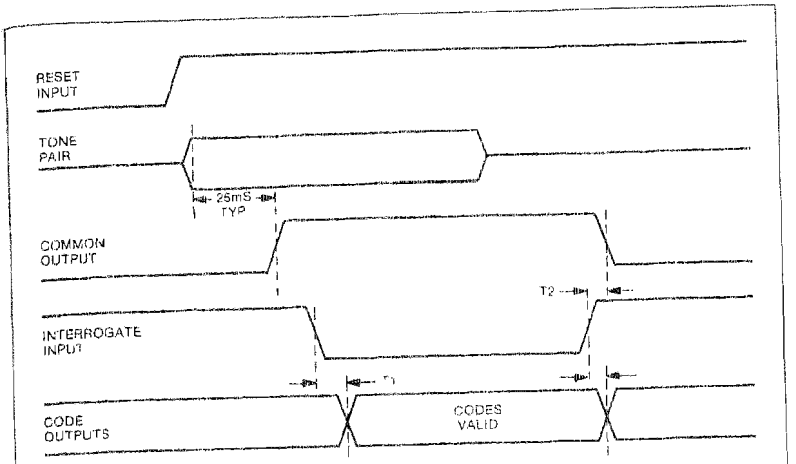
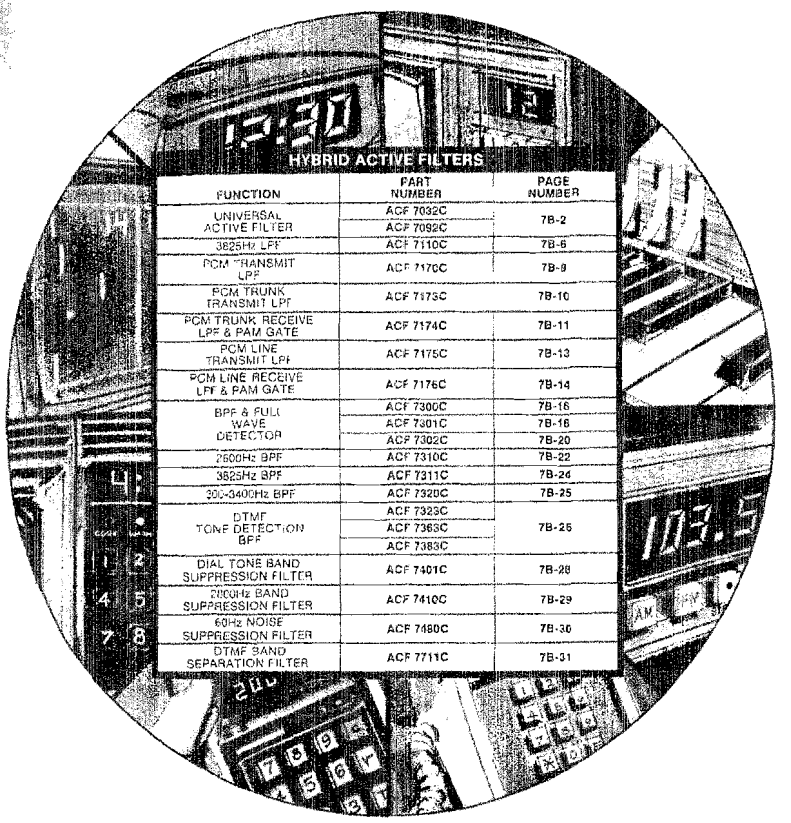


Fig.1 "HANDSHAKING" TIMING DIAGRAM



HYBRID ACTIVE FILTERS

HYBRID ACTIVE FILTERS

MICRO ELECTRONICS

7B

Universal Active Filters

FEATURES

- Low Pass, High Pass, Band Pass, and Band Reject responses from the same unit
- Independent control of Frequency, Q and Amplifier Gain
- External resistors need not temperature track internal NPO capacitors
- 10Hz. to 10KHz. operating frequency range.
- 0.5 to 50 adjustable Q range.

DESCRIPTION

The schematic diagram for the ACF 7032C/7092C is shown in Figure 1. The filter is composed of 4 operational amplifiers. The first three form the basic state variable configuration (triad) and the fourth can be utilized for increased gain or in the biquadratic configuration with the addition of external components. Two filter inputs are provided; a non-inverting input and an inverting input.

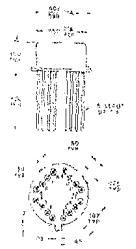
In the Triad configuration, amplifier A_1 is a summing amplifier providing the high pass output, amplifiers A_2 and A_3 are integrators providing band pass and low pass outputs. The external resistors establish the operating parameters for each filter mode. R_1 and R_2 determine the resonant frequency (Fn). R_7 and R_3 or R_7 and R_8 determine the values for gain and Q.

APPLICATIONS

General Instrument Hybrid universal active filters are low cost units that can be used to generate any filter response. Some common applications for these filters are found in sonar systems, telephone and paging systems, navigation systems, modems, transducers, biomedical measuring systems, process control equipment, data acquisition systems, radar systems, audio signal processing equipment and seismology.

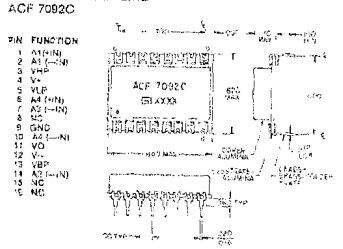
PIN CONFIGURATIONS

16 LEAD TO-8
ACF 7032C



PIN	FUNCTION
1	A1 (–IN)
2	VO
3	VLP
4	N/C
5	A3 (–IN)
6	N/C
7	GND
8	A2 (–IN)
9	VBP
10	V+
11	N/C
12	A1 (+IN)
13	VHP
14	A2 (+IN)
15	V–
16	A4 (–IN)

16 LEAD DUAL IN LINE
ACF 7092C



PIN	FUNCTION
1	A1(+IN)
2	A1 (–IN)
3	VHP
4	V+
5	VLP
6	A4 (+IN)
7	A3 (–IN)
8	N/C
9	GND
10	A3 (–IN)
11	VO
12	V–
13	VBP
14	A2 (+IN)
15	NC
16	NC

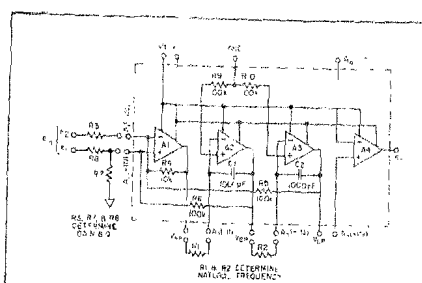


Fig 1 SCHEMATIC

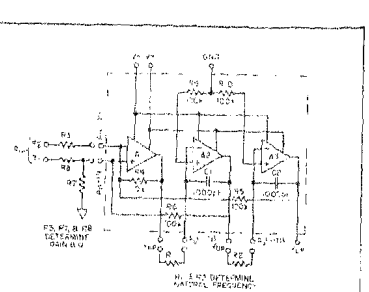


Fig. 2 TRIAD CONFIGURATION

ACTIVE FILTER DESIGN WITH UNIVERSAL FILTERS

TRIAD TRANSFER FUNCTIONS

The Triad configuration illustrated in Figure 2 gives transfer functions at the various points, HP, BP, and LP as shown in Table 1 for infinite gain band width operational amplifiers.

Table 1 TRANSFER FUNCTIONS

$$G_{HP}(s) = \frac{V_{HP}}{\text{SIN}} = \frac{G_\infty S^2}{S^2 + \frac{Wn}{Q} S + Wn^2} \qquad \text{HIGH PASS}$$

$$G_{BP}(s) = \frac{V_{BP}}{\text{SIN}} = \frac{G_0 \frac{Wn}{Q} S}{S^2 + \frac{Wn}{Q} S + Wn^2} \qquad \text{BAND PASS}$$

$$G_{LP} = \frac{V_{LP}}{\text{SIN}} = \frac{G_{(0)} Wn^2}{S^2 + \frac{Wn}{Q} S + Wn^2} \qquad \text{LOW PASS}$$

Fn = Wn/2π = Natural or corner frequency for low or high pass outputs. Center frequency for band pass output

S = Transform variable

G_∞ = Gain at infinite frequency (high pass)

G_0 = Gain at center frequency (band pass)

$G_{(0)}$ = Gain at zero frequency (low pass)

$$Q = \frac{\text{Center frequency}}{\text{Bandwidth}} \qquad \text{BAND PASS}$$

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at Infinite Frequency}} \qquad \text{HIGH PASS}$$

$$Q = \frac{\text{Gain at Natural Frequency}}{\text{Gain at DC}} \qquad \text{LOW PASS}$$

DESIGN EQUATIONS

The design equations for the transfer functions listed in Table 1 are:

$$Wn = \sqrt{a_3 W_1 W_2} \qquad W_1 = \frac{1}{R_1 C_1} \quad W_2 = \frac{1}{R_2 C_2}$$

$$Q = \left[\frac{1}{a_3 (1 + a_4 + a_5)}\right] \sqrt{\frac{a_3 W_2}{W_1}} \qquad a_4 = \frac{1}{1 + \frac{R_6}{R_7} + \frac{R_8}{R_7}}$$

$$a_2 = \frac{1}{1 + \frac{R_6}{R_7} + \frac{R_8}{R_7}} \qquad a_3 = \frac{R_4}{R_5} \qquad a_5 = \frac{R_4}{R_8}$$

	Non-Inverting Figure 3	Inverting Figure 4
G_∞	$a_1 (1 + a_3 + a_5)$	a_5
G_0	$-a_1 / a_2$	$\frac{a_5}{a_3 (1 + a_4 + a_5)}$
$G(0)$	$\frac{a_1 (1 + a_3 + a_5)}{a_3}$	a_5 / a_3

Note:
Since operational amplifiers have finite gain-bandwidths, the Q will be greater than calculated. A correction factor will be required and will operate on the desired Fn Q product. See Step #1 of Triad tuning procedure.

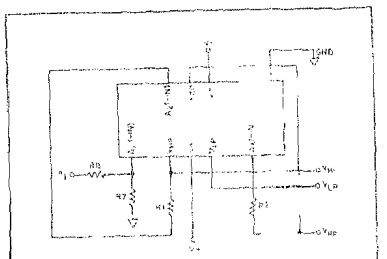


Fig. 3 NON-INVERTING CONFIGURATION

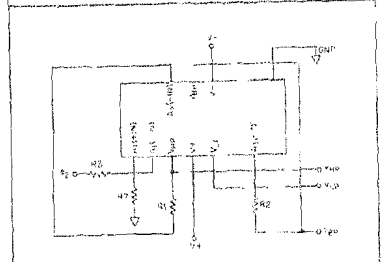


Fig. 4 INVERTING CONFIGURATION

TRIAD TUNING PROCEDURE

The following four step tuning procedure allows the selection of the external resistors R_1, R_2, R_7 and R_3 or R_8. The procedure is based on first selecting an output function (low-pass, band-pass or high-pass) and the inverting or non-inverting configuration. If other gains are desired the uncommitted operational amplifier can be used.

Step #1: Determine Design Q

Calculate the product of the desired Fn and Q. If this product exceeds 10,000 refer to Figure 5 to obtain the corresponding design FnQ. Divide the design FnQ product by Fn to determine the design Q for all subsequent calculations. The design Q now includes the effects of operational amplifier finite gain bandwidths.

If the desired FnQ product is less than 10,000, use the desired Q as the design Q for all subsequent calculations. The operational amplifier's finite gain-bandwidth in this lower FnQ region has a second order effect on the Q and can be ignored.

Step #2: Calculate R_3 or R_8 as a Function of Design Q

R_3 or R_8 can be calculated from the equations listed in Table II.

Table II R_5 OR R_8 CALCULATION

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low-Pass	$R_8 = \frac{37.8k\Omega}{Q\ design}$	$R_5 = 100k\Omega$
Band-Pass	$R_8 = \frac{Q\ desired \times 100k}{Q\ design}$	$R_5 = Q\ design \times 31.6k\Omega$
High Pass	$R_8 = \frac{31.6k\Omega}{Q\ design}$	$R_5 = 10k\Omega$

Step #3: Calculate R_1 and R_2 as a Function of Fn

For basic unity gain configuration, $R_1 = R_2$

$$R_1 = R_2 = \frac{5.04 \times 10^7}{Fn}$$

LOW FREQUENCY OPERATION

For very low frequencies (fn ≤ 50Hz) additional capacitance can be used to shunt the internal integrating capacitors from pins 5 to 7 and 13 to 14. R_1 and R_2 are then calculated as follows:

$$R_1 = R_2 = \frac{1}{2\pi Fn}\sqrt{\frac{R_A}{R_B C_1 C_2}}$$

Step #4: Calculate R_7 as a Function of Design Q

R_7 can be calculated from the equations listed in Table III

Table III R_7 CALCULATIONS

Configuration	Non-Inverting Figure 3	Inverting Figure 4
Low Pass	$R_7 = \frac{100k\Omega}{3.1R\ (Q\ desired) - 1}$	$R_7 = \frac{100k\Omega}{3.1R\ (Q\ design) - 1}$
Band-Pass	$R_7 = \frac{100k\Omega}{3.1R\ (Q\ design)\ 2}$	$R_7 = \frac{100k\Omega}{3.1R\ (Q\ design)}$
High-Pass	$R_7 = \frac{100k\Omega}{0.32\ (Q\ design) - 1}$	$R_7 = \frac{100k\Omega}{0.64\ (Q\ design) - 1}$

BIQUAD TRANSFER FUNCTION

The BIQUAD configuration for generating Cauer or Band Reject responses is shown in Figure 6

The transfer function is:

$$\frac{e_o}{e_{IN}} = A\left[\frac{S^2 + aWnS + bWn^2}{S^2 + \frac{Wn}{Q}S + Wn^2}\right]$$

The parameters for the Transmission Zeros (numerator) are given by:

$$a = \frac{R_{13}}{R_{14}}\sqrt{\frac{R_E}{R_A}} \qquad A = -\left(\frac{R_{14}}{R_{13}}\right)\times\left(\frac{R_4}{R_5}\right) \times G(0)$$

$$b = \frac{R_{13}}{R_{11}} \times \frac{R_9}{R_4}$$

provided that $R_{12} \gg R_{14} \quad R_{10} \left(\frac{R_{11}R_{13}}{R_{11} + R_{13}}\right)$

The tuning procedure for Wn and Q is the same as in the TRIAD configuration.

A Band Reject filter can be obtained by making Constant (b) = 1 and R_{12} infinite which makes the Constant (a) = zero. The transfer function then becomes:

$$\frac{e_o}{e_{IN}} = \frac{S^2 + Wn^2}{S^2 + \frac{Wn}{Q}S + Wn^2}$$

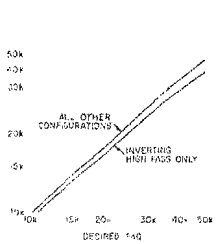


Fig. 5 FnQ CORRECTION

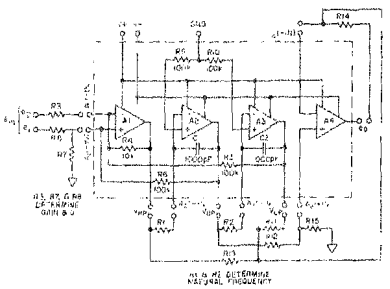


Fig. 6 BIQUAD CONFIGURATION

PERFORMANCE SPECIFICATIONS

MAXIMUM RATINGS

Supply Voltages ..... ± 18 V
Supply Current (± 15 Volt Supplies) 12mA
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +125°C

ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless other specified, these parameters apply over a temperature range of 0°C to +70°C with ± 15 VDC supplies

Characteristic	Min	Typ	Max.	Units	Conditions
FnQ Product	5	—	50,000	—	
Fn Range	10	—	10,000	Hz	Self Resonant Frequency
Fn Accuracy	—	± 1.5	±2.5	%	Note 1 T_A = 25°C
Fn Temp. Coeff	—	± 40	±75	ppm/°C	Note 2
Q Range	0.5	—	50	—	
Q Accuracy	—	± 7	—	%	
Q Temp. Stability	—	± FnΩ×10⁻⁶	—	—	0°C ≤ T_A ≤ 70°C
Pass band gain	1	—	10	—	Note 5
Input offset voltage	—	2	10	mV	T_A = 25°C
	—	—	15	mV	0°C ≤ T_A ≤ 70°C
Input offset current	—	5	200	nA	T_A = 25°C
	—	—	300	nA	0°C ≤ T_A ≤ 70°C
Input bias current	—	40	500	nA	T_A = 25°C
	—	—	300	nA	0°C ≤ T_A ≤ 70°C
Input voltage range	± 12	± 14	—	V	
Input Resistance	0.3	5	—	MΩ	
Large Signal Voltage Gain	20,000	300,000	—	—	RL ≥ 2k, Vo = ± 10V, T_A = 25°C RL ≥ 2k, Vo = ± 10V, 0°C ≤ T_A ≤ 70°C
	15,000	—	—	—	
Supply Voltage Rejection Ratio	—	30	300	mV/V	
Output Resistance	—	—	100	Ω	
Load Resistance	1.0kΩ	—	—	Ω	
Output Voltage Swing	—	—	20	V P-P	Fn = 10Hz to 1KHz (Low pass)
	—	—	8	V P-P	Fn = 10Hz to 1KHz (Band pass)
	—	—	2	V P-P	Fn = 10Hz to 1KHz (High pass)
	—	—	8	V P-P	Fn = 10KHz (Low pass)
	—	—	3	V P-P	Fn = 10KHz (Band pass)
	—	—	0.8	V P-P	Fn = 10KHz (High pass)
Common mode rejection ratio	70	90	—	dB	

Note 1. The 25°C Fn accuracy is determined by the internal capacitor tolerance (±1%), and the R_4/R_5 tolerance (±2%) and does not include the tolerance of the external resistors R1 and R2

Note 2. The internal capacitors have a temperature coefficient of ± 30 ppm/°C. The remaining portion of the temperature coefficient is due to the change of the operational gain band width products over temperature

Note 3. Gain greater than 1 can be provided with the uncommitted amplifier

ENVIRONMENTAL SPECIFICATION

(The hybrids are capable of meeting the following specifications)

Thermal Shock ..... -55°C to +125°C, 15 cycles (Mil-Std-883, Method 1011, Test Condition B)
Temperature Cycling ..... -55°C to +125°C, 10 cycles (Mil-Std-883, Method 1010, Test Condition B)
Moisture Resistance ..... Omit initial conditioning (Mil-Std-883, Method 1004) 80% to 98% RH and +10°C to +65°C no power applied
Mechanical Shock ..... 3000 g's (Mil-Std-883, Method 2002, Test Condition C)
Vibration Variable Frequency ..... 50G's peak acceleration (Mil-Std-883, Method 2007, Test Condition B)
Constant Acceleration ..... A=5,000 g's to axis, X, Y₂ Z (Mil-Std-883, Method 2001, D=20,000 g's to Y- axis, Test Conditions A and C)
Solderability ..... All terminals, no special preparation (Mil-Std-883, Method 2003)
Intermittent Life ..... 1,000 hours at rated voltage in 70°C free air (Mil-Std-883, Method 1005) 1.5 hours ON, 0.5 hours OFF
Seal leak rate ..... 5×10⁻⁸cc/s Calculated rate per Mil-Std-883 Method 1014, Test Condition A

7B

3825Hz Low Pass Filter

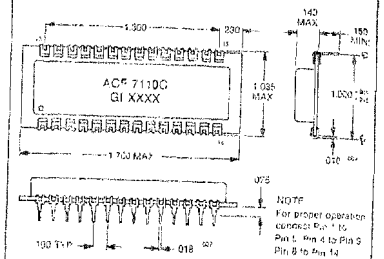
FEATURES

- 0 Insertion Loss
- High Out of Band Attenuation
- Low Noise
- Low In Band Ripple
- Can be operated from a single-ended power system

DESCRIPTION

The ACF 7110C is a linear hybrid low pass RC active filter. The ACF 7110C filter provides for low pass filtering of speech frequencies while attenuating the 3825 Hz signaling frequency to a minimum attenuation of 60 dB. The reference 1.0KHz gain of this filter is 0 dB with a maximum in band ripple specification of plus or minus 0.15 dB. This filter is packaged in a dual in line configuration.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Stage 1 Output	15	T.P.
2	Input	16	N.C.
3	N.C.	17	N.C.
4	Stage 2 Output	18	T.P.
5	Stage 2 Input	19	N.C.
6	N.C.	20	N.C.
7	+15 Volts P.S.	21	N.C.
8	Stage 3 Output	22	T.P.
9	Stage 3 Input	23	N.C.
10	N.C.	24	N.C.
11	Output (low impedance)	25	T.P.
12	Output (600 Ω)	26	N.C.
13	T.P.	27	-15 Volts P.S.
14	Stage 4 Input	28	GND

MAXIMUM RATINGS

V_{CC} (Max) ..... ±16 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

V_{CC} = ± 12 Volts
T_A = +25°C
R_S = 50 Ω
R_L = 600 Ω

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-0.4	0	+0.4	dB	1.0KHz, V_{OUT} = 1.0 V_{RMS}
Gain Stability	-1.0	—	+1.0	dB	0°C to +70°C from ref. 1.0KHz gain
Frequency Response					Referenced to 1.0KHz Gain, V_{OUT} = 1.0 V_{RMS}
	-0.15	—	+0.15	dB	300Hz to 2400Hz
	-0.2	—	+0.15	dB	2900Hz
	-0.25	—	+0.15	dB	3000Hz
	-0.75	—	+0.15	dB	3250Hz
	-50	—	—	dB	3825Hz
	-43	—	—	dB	3850Hz to 4050Hz
	-35	—	—	dB	4050Hz to 5000Hz
	-22	—	—	dB	5000Hz to 20.0KHz
	-25	—	—	dB	20.0KHz
	-25	—	—	dB	56.0KHz
Input Impedance	10	—	—	KΩ	
Output Impedance	—	—	600	Ω	
Harmonic Distortion	-38	—	—	dBm	V_{IN} = +8.0 dBm, 300Hz to 2400Hz. Second or Third Harmonic Output
Output Offset Voltage	—	—	50	mV	
Current Drain	—	—	20	mA	V_{CC} = ±15 Volts
Noise	—	—	275	uV	Unweighted noise in the pass band

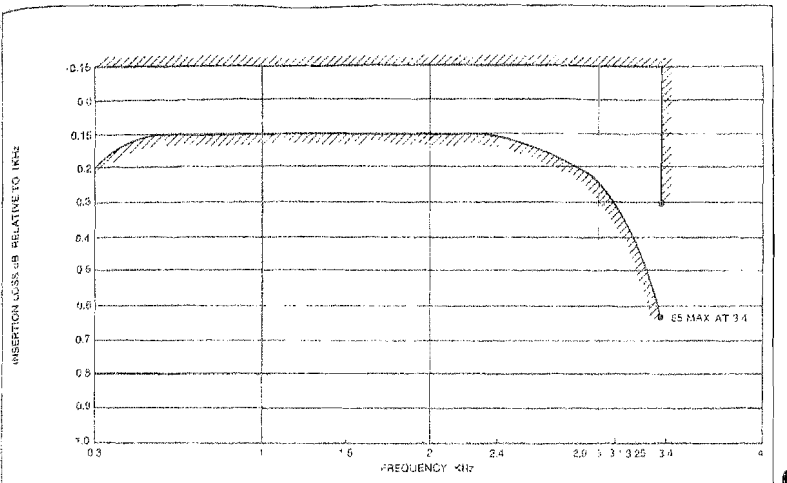


Fig.1 LOW PASS FILTER PASSBAND PERFORMANCE LIMITS

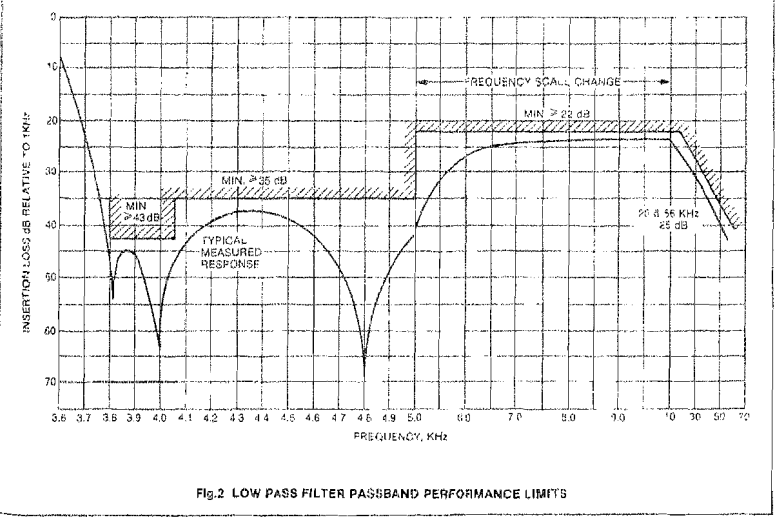


Fig.2 LOW PASS FILTER PASSBAND PERFORMANCE LIMITS

PCM Transmit Low Pass Filter

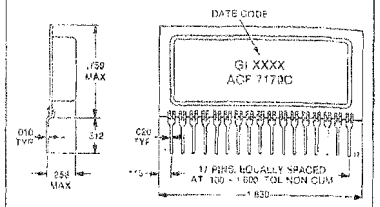
FEATURES

- Pass band ripple ±0.15dB, from 100 to 3KHz, 0° to 70°C
- Stop band attenuation, 39 dB, 4.6KHz to 100KHz
- Low power dissipation, 25 mW typical
- Insertion Loss — 0 dB
- Can be adjusted to meet these specifications for power supplies from ±4 volts to ±15 volts or equivalent single ended supplies

DESCRIPTION

The ACF 7170C is a linear hybrid low pass active filter with a Cauer type response (transfer function based on elliptic functions). The hybrid will pass a signal in the pass band with ±.15 dB ripple to 3KHz and be 39 dB down at 4.6KHz with equal rejection out to 100KHz. The filter is designed to be used in PCM transmit applications.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	NC	10	V_{CC}
2	NC	11	Output
3	NC	12	Int Conn
4	NC	13	Int Conn
5	Input	14	NC
6	Int Conn	15	NC
7	Int Conn	16	NC
8	GND	17	NC
9	V_{EE}	18	NC

NOTE: An external connection is required between Pins 6 & 7 and Pins 12 & 13

MAXIMUM RATINGS

V_{CC} ..... ±12V
Input Voltage ..... V_{CC}
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$
V_{CC} = 10 ±.25V
$-V_{CC}$ = 10 ±.25V } (Note 1)
R_L = 2KΩ (Note 2)
R_S = 50Ω (Note 1)

Characteristic	Min	Typ	Max	Units	Conditions
Passband Freq. Range	0	—	3	KHz	
Passband Ripple	—	0.1	±0.15	dB	100Hz to 3KHz
Gain	-0.15	—	+0.15	dB	Ref Freq. 1KHz
Cutoff Freq. Attn	0	—	-1.0	dB	3.4KHz
Stop Band Atten	15	—	—	dB	4.0KHz
Stop Band Atten	39	42	—	dB	4.6KHz to 100KHz
Input Impedance	500	—	—	KΩ	100Hz to 3KHz
Output Impedance	—	50	100	Ω	100Hz to 3KHz
Output Signal Level	—	—	7.5	Vp-p	100Hz to 3KHz
Power Dissipation	—	25	50	mW	

NOTES
1. Or equivalent single ended supplies
2. 600 ohm load capability can be supplied by the factory

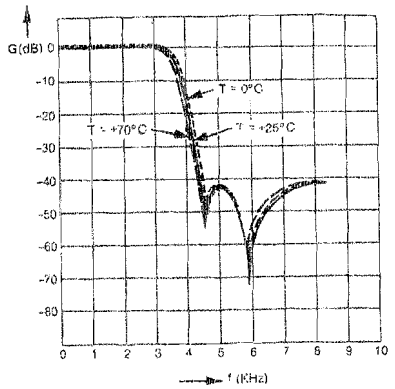


Fig.1 LOW PASS DATA FILTER TRANSMISSION CHARACTERISTICS

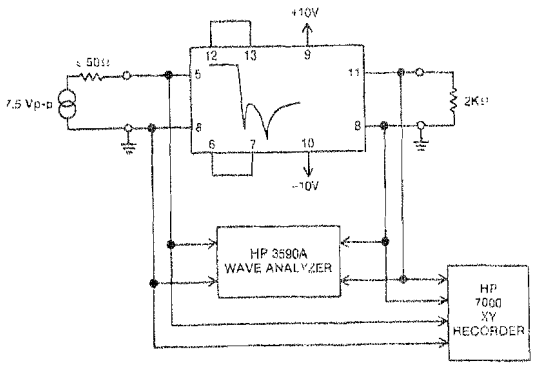


Fig.2 TEST CIRCUIT

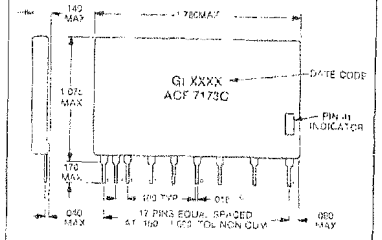
ACF 7173C

PCM Trunk Transmit Low Pass Filter

FEATURES

- Exceeds AT & T D3 Channel Bank Compatibility Specifications.
- Low Noise -15dBRNC @ Gain = +10db
- 60Hz Attenuation -14.5 db Min.
- Adjustable Gain 0 to +29db
- Output Clamp Voltage 4.5 Volts maximum
- Output Power Supply Rejection Ratio - 40db minimum (Freq 300Hz to 4KHz)
- Low Power Dissipation -240 milliwatts maximum
- Maximum output voltage = 4.0 Volts

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Mechanical Support	10	NA
2	NA	11	GND
3	NA	12	NA
4	Input	13	Negative V_{CC}
5	NA	14	NA
6	NA	15	Gain Adjust - Potentiometer Termination
7	Mechanical Support		
8	NA	16	Gain Adjust - Potentiometer Wiper
9	Positive V_{CC}	17	Output

DESCRIPTION

The ACF7173C is a linear hybrid low pass active filter with a Cauer type response. It is capable of exceeding AT & T D3 Channel Bank Compatibility Specifications and is designed to be used in PCM "Trunk" Transmit applications. This RC Active Filter will pass a signal in the pass band with 0.2db p-p ripple from 300Hz to 3000Hz and be 32db down at 4.6KHz with equal rejection to 12KHz minimum.

MAXIMUM RATINGS

V_{CC} ..... ±18 Volts
Input Voltage ..... V_{CC}
Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

R_S = 600Ω V_{OUT} = 8Vp-p
R_L = 1.2K V_{CC} = ±12 Volts

Characteristic	Min.	Typ	Max.	Units	Conditions
Frequency Response (See Note 1)					Referenced to 1KHz V_{OUT} = V_{RMS}
	-14.5	—	—	dB	60Hz
	-1.0	—	0	dB	180Hz to 300Hz
	-0.1	—	+0.1	dB	300Hz to 3000Hz
	+1.2	—	0	dB	3400Hz
	-14.5	—	—	dB	4000Hz
	-32.0	—	—	dB	4600Hz to 12kHz
Input Impedance	100K	—	—	ohms	
Output Impedance	—	—	10	ohms	
Envelope Delay Distortion	—	102	200	µsec	800-2700Hz
	—	53	100	µsec	1000-2500Hz
	—	30	60	µsec	1150-2300Hz
Guaranteed Gain Adjustment Range	0	—	+29.25	dB	Freq = 1KHz, Fig. 1
Output Clamp Voltage	±4.2	—	±4.5	Volts	Input Voltage ±12 Volts
Noise (See Note 2)	—	—	-15	dBRNC	Gain = 10db
Output Power Supply Rejection Ratio	-40	—	—	dB	Gain = -29db Freq. = 100Hz to 4KHz
	-30	—	—	—	Freq = 4kHz to 10kHz
Current Drain	—	8	10	mA	V_{CC} = -12
	—	8	10	mA	V_{CC} = +12
Single Freq. Distortion	-55	—	—	dB	Referenced to Freq = 1020Hz & 300Hz to 4kHz
DC Output Offset Voltage	—	—	10	±mV	
Load Capacitance	—	—	5000	pF	No evidence of oscillation

NOTES
1 Test Equipment - HP3330B Synthesizer, HP3570A Network Analyzer
2 Test Equipment - NEC Model TTS-37BAQ Noise Measuring Test Set

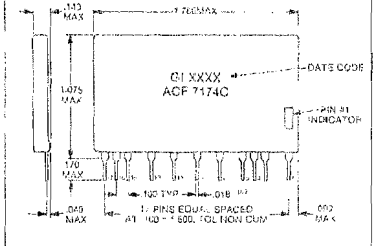
ACF 7174C

PCM Trunk Receive Low Pass Filter and PAM GATE

FEATURES

- DEMOD PAM GATE and Trunk Receive Filter in one Pkg
- Exceeds AT & T D3 Channel Bank Compatibility Specifications.
- Low Noise +2DBRNC Max
- Adjustable Gain -16 to +3.56dB
- Output Power Supply Rejection Ratio 40dB minimum (Freq. 300Hz to 4KHz)
- Low Power Dissipation 240mW maximum

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Mechanical Support	10	NA
2	NA	11	Ground
3	PAM GATE Bias - Positive V_{CC}	12	NA
4	Input	13	Negative V_{CC}
5	PAM GATE Input	14	NA
6	NA	15	Gain Adjust - Potentiometer Termination
7	Mechanical Support		
8	NA	16	Gain Adjust - Potentiometer Wiper
9	Positive V_{CC}	17	Output

DESCRIPTION

The ACF7174C is a PAM GATE a Linear low pass active filter Cauer response with SINX/X correction packaged in a hybrid. It is capable of exceeding AT & T D3 Channel Bank Compatibility Specifications and is designed to be used in PCM "Trunk" Receive applications. The hybrid demultiplexes, holds and filters the input information.

MAXIMUM RATINGS

V_{CC} ..... 18 Volts
Input Voltage ..... V_{CC}
Storage Temperature ..... -65°C to 150°C
Operating Temperature ..... 0°C to 70°C

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

V_{CC} = ±12 Volts
R_S = 10Ω
R_L = 1.2K

Characteristic	Min	Typ	Max	Units	Conditions
Frequency Response (See Note 1)					Referenced to 1KHz V_O = 1 V_{RMS}
	-1.0	—	0	dB	180Hz to 300Hz,
	-0.1	—	0.1	dB	300Hz to 3000Hz
	-1.2	—	0	dB	3400Hz
	-14.5	—	—	dB	4000Hz
	-26.0	—	—	dB	4600Hz to 12KHz
Input Impedance	—	20K	—	ohms	
Output Impedance	—	—	10	ohms	
Envelope Delay Distortion	—	102	200	µsec	800-2700Hz
	—	53	100	µsec	1000-2500Hz
	—	30	60	µsec	1150-2300Hz
Guaranteed Gain Adjustment Range	-16	—	+3.56	dB	Freq. = 1KHz, V_{IN} = 8Vp-p
Noise (See Note 2)	—	—	+2	dBRNC	V_O = 1.3Vp-p
Power Supply Rejection Ratio	-40	—	—	dB	Freq. = 300Hz to 4KHz
	-30	—	—	dB	Freq. = 4KHz to 10KHz
Current Drain	—	5	10	mA	V_{CC} = ±12V
Single Freq. Distortion	-55	—	—	dB	Referenced to Freq. 1020Hz & V_O = 8Vp-p 300Hz to 4kHz
Gate "On" vs "Off" Isolation	-80	—	—	dB	Freq. 300Hz to 3000Hz Gain = maximum R_L = 600Ω, Fig. 2

NOTES:
1 Test Equipment - HP3330B Synthesizer, HP3570A Network Analyzer
2 Test Equipment - NEC Model TTS - 37BAQ Noise Measuring Test Set

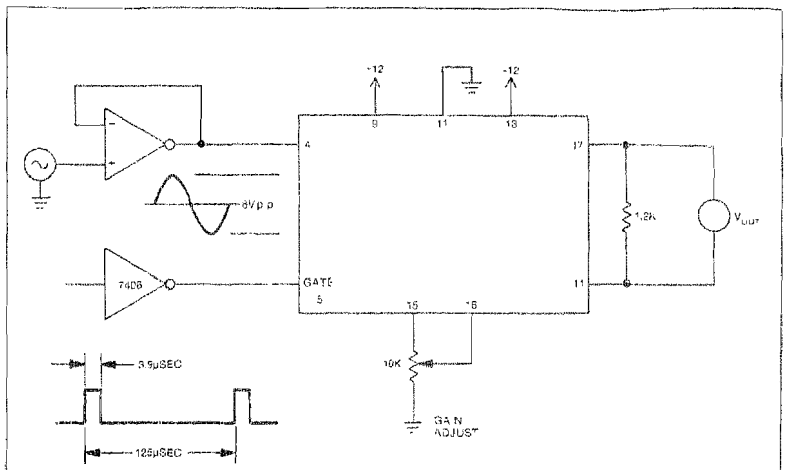


Fig.1

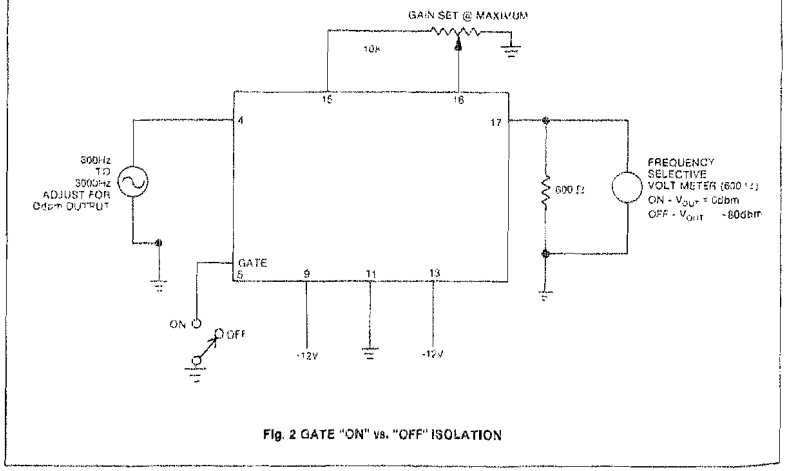


Fig. 2 GATE "ON" vs. "OFF" ISOLATION

PCM Line Transmit Low Pass Filter

FEATURES

- Exceeds AT & T D3 Channel Bank Compatibility Specifications
- Low Noise 12dBRNC @ Gain = +8.25db
- Output Clamp Voltage ±4.5 Volts Maximum
- Output Power Supply Rejection Ratio 40db minimum (Freq. 300Hz to 4KHz)
- Low Power Dissipation 240 milliwatts maximum

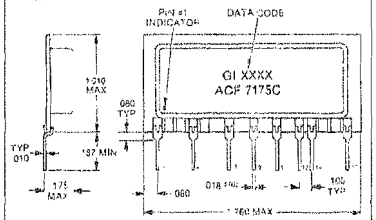
DESCRIPTION

The ACF7175 is a linear hybrid low pass active filter with a Cauer type response. It is capable of exceeding AT & T D3 Channel Bank Compatibility Specifications and is designed to be used in PCM "Line" Transmit applications. This RC Active Filter will pass a signal in the pass band with 0.6 db p-p ripple from 300Hz to 3000Hz and be 30db down at 4.6KHz with equal rejection to 12KHz minimum.

MAXIMUM RATINGS

V_{CC} ..... ±18 Volts
Input Voltage ..... V_{CC}
Storage Temperature ..... -65°C to 150°C
Operating Temperature ..... 0°C to 70°C

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Mechanical Support	10	NA
2	NA	11	GND
3	NA	12	NA
4	Input	13	Negative V_{CC}
5	NA	14	Mechanical Support
6	NA	15	NA
7	Mechanical Support	16	NA
8	NA	17	Output
9	Positive V_{CC}		

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

V_{OUT} = 8Vp-p
V_{CC} = ±12 Volts
R_S = 600Ω
R_L = 1.2K

Characteristic	Min	Typ	Max	Units	Conditions
Frequency Response (See Note 1)					Referenced to 1KHz, V_{OUT} = $1V_{RMS}$, DC Blocking
	-0.3	—	0.3	dB	300Hz to 3000Hz
	-14.5	—	0	dB	4000Hz
	-30.0	—	—	dB	4600Hz to 12KHz
Input Impedance	100K	—	—	ohms	
Output Impednace	—	—	10	ohms	
Envelope Delay Distortion	—	102	150	μsec	800-2700Hz
	—	53	75	μsec	1000-2500Hz
	—	30	40	μsec	1150-2300Hz
Gain	8.15	—	8.35	dB	Freq. = 1KHz
Output Clamp Voltage	±4.2	—	±4.5	Volts	Input Voltage ≤ ±12 Volts
Noise (See Note 2)	—	+6	+12	dBRNC	
Output Power Supply Rejection Ratio	-40	—	—	dB	Freq. 300Hz to 4KHz
	-30	—	—	—	Freq. 4KHz to 10KHz
Current Drain	—	8	10	mA	V_{CC} = +12V
	—	8	10	mA	V_{CC} = -12V
Single Freq. Distortion	-55	—	—	dB	Referenced to Freq. 1020Hz & V_O = 8 Vp-p, 300Hz to 4kHz.
DC Output Offset Voltage	-10	0	10	mV	
Load Capacitance	—	—	5000	pF	No evidence of oscillation

NOTES:
1. Test Equipment - HP 3330B Synthesizer, HP 3570A Network Analyzer
2. Test Equipment - NEC Model TTS-37BAQ Noise Measuring Test Set

PCM Line Receiver Low Pass Filter and PAM GATE

FEATURES

- DEMOD PAM GATE and Line Receive Filter in one package
- Exceeds AT & T D3 Channel Bank compatibility specification
- Low noise -10dbrnc maximum
- Output Power Supply Rejection Ratio — 40db maximum (Freq 300Hz to 4kHz)
- Low Power Dissipation — 240mw maximum

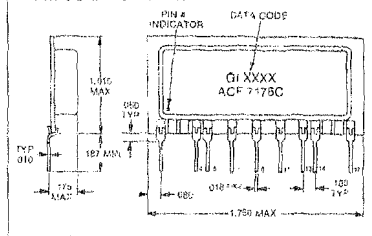
DESCRIPTION

The ACF 7176 is a PAM GATE, a linear low pass active filter Cauer response with SINX/X correction packaged in a hyorid. It is capable of exceeding AT & T D3 Channel Bank Compatibility Specifications and is designed to be used in PCM "Line" receiver applications. The hybrid demultiplexes, holds and filters the input information.

MAXIMUM RATINGS

V_{CC}	±18 Volts
Input Voltage	V_{CC}
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to +70°C

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Mechanical Support	10	NA
2	NA	11	GND
3	NA	12	NA
4	Input	13	Negative V_{CC}
5	PAM GATE Input	14	Mechanical Support
6	NA	15	NA
7	Mechanical Support	16	NA
8	NA	17	Output
9	Positive V_{CC}		

ELECTRICAL CHARACTERISTICS (at 25°C unless otherwise specified)

V_{CC} = ±12 volts
R_S = 10Ω
R_L = 1.2K

Characteristic	Min.	Typ.	Max.	Units	Conditions
Frequency Response (See Note 1)					Referenced to 1KHz, V_O = 1 VRMS
	-0.3	–	+0.3	dB	300Hz to 3000Hz
	-14.5	–	–	dB	4000Hz
	-28.0	–	–	dB	4600Hz to 12KHz
Input Impedance	–	20K	–	ohms	
Output Impedance	–	–	10	ohms	
Envelope Delay Distortion	–	102	150	usec	800-2700Hz
	–	53	75	usec	1000-2500Hz
	–	30	40	usec	1150-2300Hz
Gain	-8.4	-8.25	-8.0	dB	Freq = 1KHz
Noise (See Note 2)	–	–	+10	dBRNC	
Power Supply Rejection Ratio	-40	–	–	dB	Freq 300Hz to 4KHz
	-30	–	–	–	Freq 4KHz to 10KHz
Current Drain	–	8	10	mA	V_{CC} = ±12V
Single Freq. Distortion	-55	–	–	dB	Referenced to Freq 1020Hz & V_O = 8 V p-p 300Hz to 4kHz
Gate "On" vs. "Off" Isolation	-80	–	–	dB	Freq. 300Hz to 3000Hz

NOTES
1. Test Equipment — HP3300B Synthesizer, HP3570A Network Analyzer
2. Test Equipment — NEC Model TTG-376AQ Noise Measuring Test Set

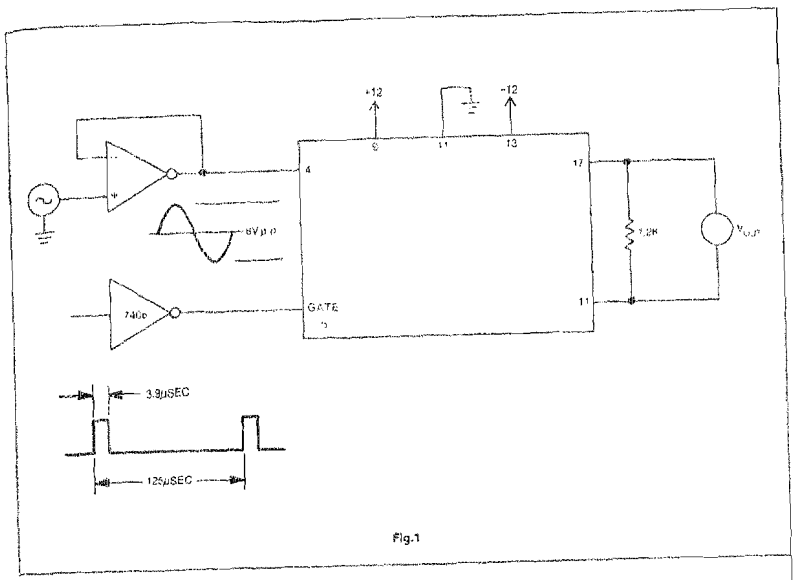


Fig.1

LINE RECEIVE

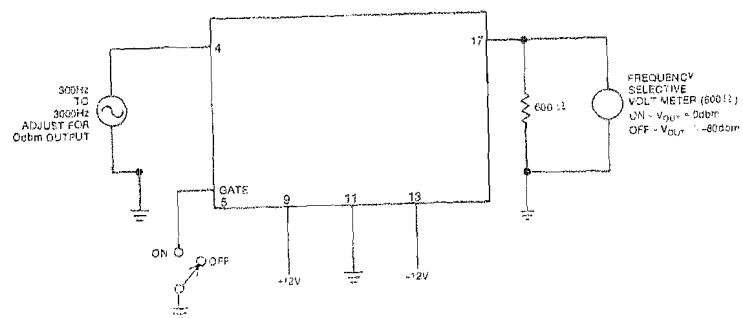


Fig. 2 GATE "ON" vs. "OFF" ISOLATION

ACF 7300C

Band Pass Filter and Full Wave Detector

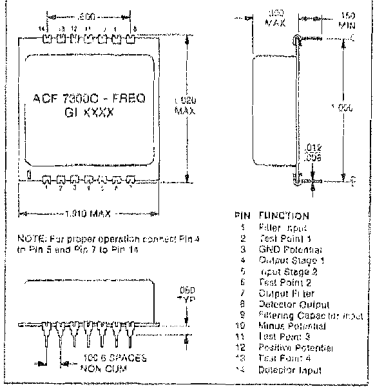
FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 20 dB minimum attentuation at stop band frequencies
- 0 dB insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

DESCRIPTION

The ACF 7300C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 540Hz to 1980Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

PACKAGE INFORMATION
PIN CONFIGURATION



NOTE: For proper operation connect Pin 4 to Pin 5 and Pin 7 to Pin 14

PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	Test Point 3
12	Positive Potential
13	Test Point 4
14	Detector Input

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Filter Load Resistance = 5KΩ
Detector Load Resistance = 5KΩ
Source Impedance, Filter or Detector = 50Ω

Characteristic	Min.	Typ.	Max.	Units	Conditions
Filter					
Input Impedance	10	—	—	K ohms	
Voltage Gain					See Figure 1.
	—	0	0.5	dB	Ideal Center Frequency (F_O)
	—	0	1.5	dB	Pass Band (±10Hz from F_O)
	-20	—	—	dB	Stop Band (±110Hz from F_O)
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	ohms	
Detector					
Input Impedance	25	—	—	K ohms	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	V_{DC}/V_{RMS}	See Figure 2
Output Impedance	—	—	25	ohms	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.6	3.0	mA	

Standard factory tuned filters available with the following ideal center frequencies:
540Hz, 660Hz, 780Hz, 900Hz, 1020Hz, 1140Hz, 1380Hz, 1500Hz, 1620Hz, 1740Hz, 1860Hz, and 1980Hz. To order one of the above tuned filters, specify the device as follows: ACF 7300C - Frequency e.g. ACF 7300C - 0540
Other factory tuned frequencies are available upon request and nominal set up charge.

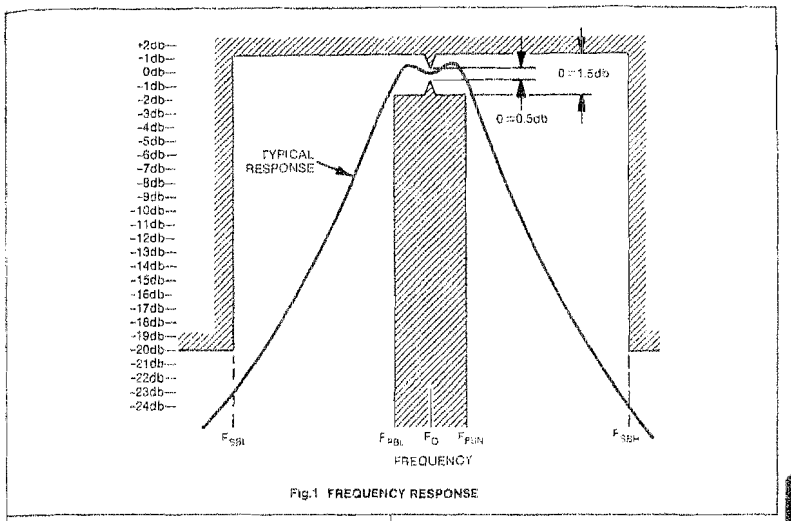


Fig.1 FREQUENCY RESPONSE

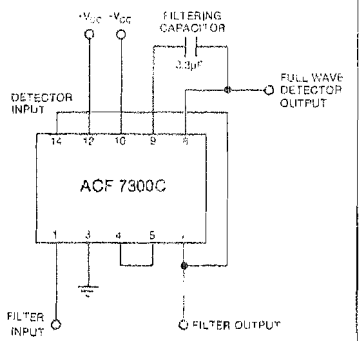


Fig.2 TYPICAL APPLICATION

Table I

Center Frequency (FO)(Hz)	Low Stop Band Frequency (FSBL)(Hz)	Low Pass Band Frequency (FPBL)(Hz)	High Pass Band Frequency (FPBH)(Hz)	High Stop Band Frequency (FSBH)(Hz)
540	430	530	550	650
660	550	650	670	770
780	670	770	790	890
900	790	890	910	1010
1020	910	1010	1030	1130
1140	1030	1130	1150	1250
1380	1270	1370	1390	1490
1500	1390	1490	1510	1610
1620	1510	1610	1630	1730
1740	1630	1730	1750	1850
1860	1750	1850	1870	1970
1980	1870	1970	1990	2090

7B

Band Pass Filter and Full Wave Detector

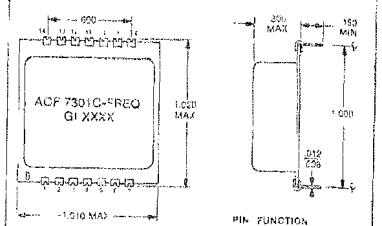
FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 0db insertion loss in pass band
- 20db minimum attenuation at stop band frequencies
- Fixed band width filter
- Internal full wave detector

DESCRIPTION

The ACF 7301C consists of a four (4) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 700Hz to 1700Hz, and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION
1	Filter Input
2	Test Point 1
3	GND Potential
4	Output Stage 1
5	Input Stage 2
6	Test Point 2
7	Output Filter
8	Detector Output
9	Filtering Capacitor Input
10	Minus Potential
11	NC
12	Positive Potential
13	NC
14	Detector Input

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = ±12 Volts
0°C to +70°C
Load Resistance, Filter Output or Detector Output = 5K ohms
Source Impedance, Filter Input or Detector Input = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	10	—	—	K ohms	
Voltage Gain					See Figure 1
	—	0	0.5	±dB	Ideal Center Frequency (F_O)
	—	0	1.5	±dB	Pass Band (±15Hz from F_O)
	-20	—	—	dB	Stop Band (±185Hz from F_O)
Input Voltage	5	—	—	V_{RMS}	
Output Impedance	—	—	25	ohms	
Detector					
Input Impedance	25	—	—	K ohms	
Input Voltage	5	—	—	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2
Output Impedance	—	—	25	ohms	
Output Offset Voltage	—	—	20	mVolts	
Power Supply Current	—	1.5	3.0	mA	

Standard factory tuned filters available with the following ideal center frequencies, 700Hz, 900Hz, 1100Hz, 1300Hz, 1500Hz, and 1700Hz. To order one of the above tuned filters, specify the device as follows. ACF 7301 C - Frequency, e.g. ACF 7301 C - 0700. Other factory tuned frequencies are available upon request and a nominal set up charge.

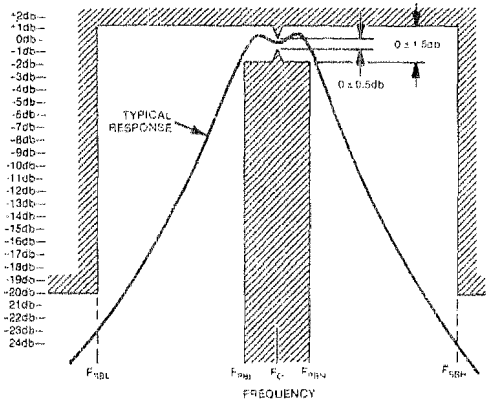


Fig.1 FREQUENCY RESPONSE

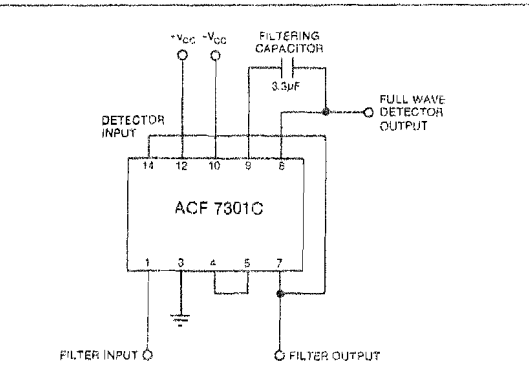


Fig.2 TYPICAL APPLICATION

7B

TABLE 1

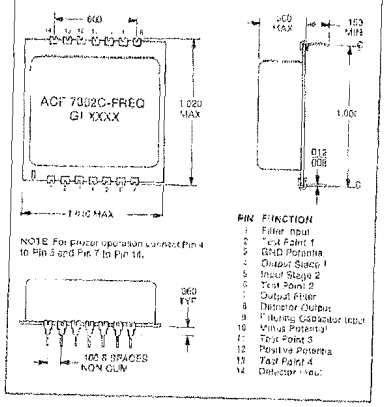
Center Frequency (FO) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FBBH) (Hz)
700	505	685	715	885
900	715	885	915	1085
1100	915	1085	1115	1285
1300	1115	1285	1315	1485
1500	1315	1485	1515	1685
1700	1515	1685	1715	1895

Band Pass Filter and Full Wave Detector

FEATURES

- Low Power Dissipation
- Can be operated from a single ended power system
- 20dB minimum attentuation at stop band frequencies
- 0dB Insertion loss in pass band
- Fixed band width filter
- Internal full wave detector

PACKAGE INFORMATION
PIN CONFIGURATION



DESCRIPTION

The ACF 7302C consists of six (6) pole, fixed band width, band pass filter, factory tunable over a center frequency (F_O) range of 2280Hz to 3825Hz and a full wave detector. This RC active filter and detector is packaged in a dual in line package. Only one external capacitor is required for filtering the detector output, the balance of the circuitry is self contained requiring no additional components for proper operation.

MAXIMUM RATINGS

V_{CC} (Max) . . . . . ±18 Volts
V_{CC} (Min) . . . . . ±5 Volts
Input Voltage Range . . . . . Power Supply Potential
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = 12 Volts
0°C to +70°C
Filter and Detector Load Resistance = 5K ohms
Filter and Detector Source Impedance = 50Ω

Characteristic	Min	Typ	Max	Units	Conditions
Filter					
Input Impedance	10	--	--	K ohms	
Voltage Gain	--	0	0.5	dB	See Figure 1 Ideal Center Frequency (F_O)
	--	0	1.5	dB	Pass Band (±15Hz from F_O)
	-22	--	--	dB	Stop Band (±120Hz from F_O)
Input Voltage	5	--	--	V_{RMS}	
Output Impedance	--	--	25	ohms	
Detector					
Input Impedance	25	--	--	K ohms	
Input Voltage	5	--	--	V_{RMS}	
Voltage Gain	0.95	1.0	1.05	VDC/V_{RMS}	See Figure 2
Output Impedance	--	--	25	ohms	
Output Offset Voltage	--	--	20	mVolts	
Power Supply Current	--	3.0	5.0	mA	

Standard factory tuned filters available with the following ideal center frequencies: 2280Hz, 2400Hz, 2600Hz, 3825Hz. To order one of the above tuned filters, specify the device as follows, ACF 7320 C - Frequency, e.g. ACF 7322 C - 2280. Other factory tuned frequencies are available upon request and a nominal set up charge.

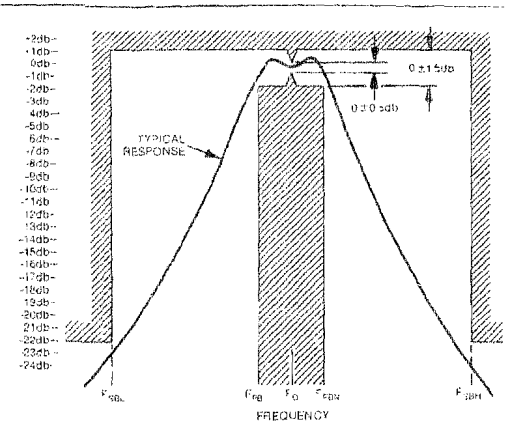


Fig.1 FREQUENCY RESPONSE

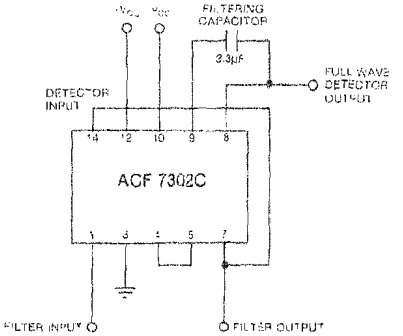


Fig.2 TYPICAL APPLICATION

7B

Table I

Center Frequency (FC) (Hz)	Low Stop Band Frequency (FSBL) (Hz)	Low Pass Band Frequency (FPBL) (Hz)	High Pass Band Frequency (FPBH) (Hz)	High Stop Band Frequency (FSBH) (Hz)
2280	2160	2265	2295	2400
2400	2280	2385	2415	2520
2600	2480	2585	2615	2720
3825	3705	3810	3840	3945

2600Hz Band Pass Filter

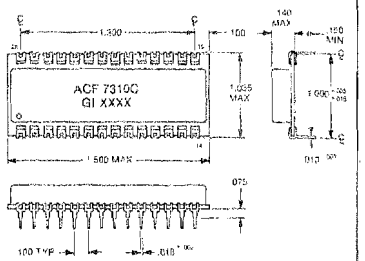
FEATURES

- 0 Insertion Loss
- Low Power Dissipation
- Narrow Band Width
- High Out of Band Attenuation
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7310C is a linear hybrid band pass RC active filter. The ACF 7310C is a sharply tuned filter designed to detect and pass the 2600Hz signaling frequency. This filter provides for a minimum attenuation of 30 dB, plus and minus 200Hz from the ideal center frequency. The filter is self contained and requires no external components for proper operation. This filter is packaged in a dual in line configuration.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Input	10	Stage 2 Input	20	NC
2	NC	11	NC	21	NC
3	NC	12	Stage 2 Output	22	+7 VDC
4	NC	13	NC	23	NC
5	NC	14	Output	24	+12 VDC
6	GND	15	Stage 3 Input	25	NC
7	NC	16	NC	26	Stage 1 Output
8	NC	17	NC	27	NC
9	NC	18	NC	28	NC

NOTE: For proper operation connect Pin 26 to Pin 10, Pin 12 to Pin 15

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-0.5	0	+0.5	dB	Ideal Center Frequency (F_C), 2600Hz
Frequency Response					Referenced from F_O Gain
	-70	—	—	dB	DC to 1500Hz
	-60	—	—	dB	2100Hz
	-30	—	—	dB	2400Hz
	-3	—	—	dB	2540Hz
	—	—	-3	dB	2660Hz
	—	—	-3	dB	2840Hz
	-3	—	—	dB	2860Hz
	-30	—	—	dB	2800Hz
	-50	—	—	dB	3100Hz
	-70	—	—	dB	3600Hz to 50KHz
Ripple	—	—	-0.5	dB	2541Hz to 2659Hz (Reference Fig. 1)
Input Impedance	25	—	—	KΩ	
Output Offset Voltage	—	—	20	mV	
Output Impedance	—	—	25	Ω	
Harmonic Distortion	—	—	1.0	%	V_{OUT} = 10 V_{RMS}, Freq. = 2600Hz
Current Drain	—	—	5.0	mA	

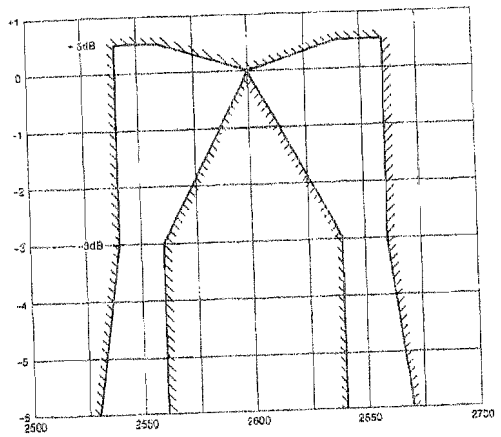


Fig.1 ACF7310C PASS BAND ATTENUATION LIMITS EXPANDED

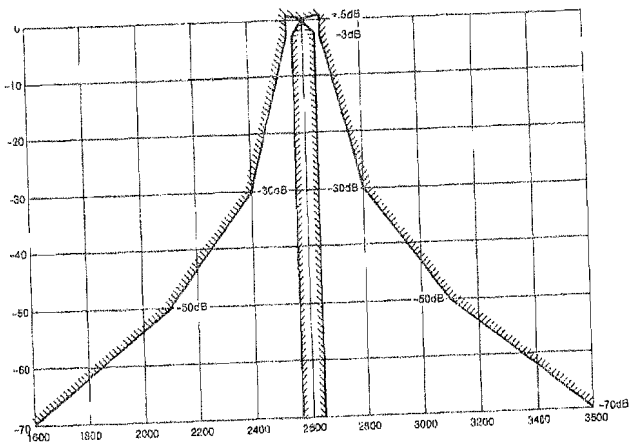


Fig.2 ACF 7310C PASS BAND ATTENUATION LIMITS

ACF 7311C

3825Hz Band Pass Filter

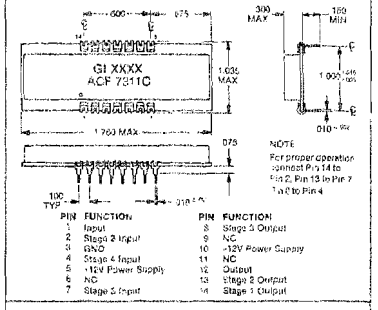
FEATURES

- 0 dB Insertion loss
- Low Power Dissipation
- Narrow Band Width
- High Out of Band Attenuation
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7311C is a linear hybrid band pass RC active filter. The ACF 7311C is a sharply tuned filter designed to detect and pass the 3825Hz signaling frequency. The filter provides for a minimum attenuation of 40 dB, plus and minus 200Hz from the ideal center frequency. The filter is self contained and requires no external components for proper operation. This filter is packaged in a dual in line package.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Input	8	Stage 3 Output
2	Stage 2 Input	9	NC
3	GND	10	+12V Power Supply
4	Stage 4 Input	11	NC
5	+12V Power Supply	12	Output
6	NC	13	Stage 2 Output
7	Stage 3 Input	14	Stage 1 Output

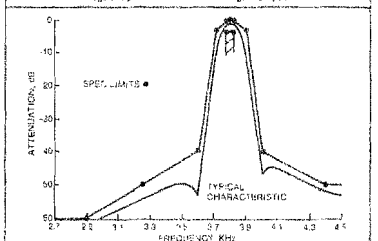


Fig.1 FREQUENCY RESPONCE CHARACTERISTICS

Maximum Ratings

V_{CC} (Max) ..... ± 18 Volts
V_{CC} (Min) ..... ± 5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)
V_{CC} = ±12 Volts
T_A = 25°C
R_S = 50 Ω
R_L = 10 K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage	-0.4	0	+0.4	dB	Ideal Center Frequency (F_O), 3825Hz
Gain Stability	-1.0	—	+1.0	dB	0°C to +70°C, from Ref. Gain @ F_O
Frequency Response					Referenced from F_O Gain
	-60	—	—	dB	DC to 2800Hz
	-50	—	—	dB	3250Hz
	-40	—	—	dB	3610Hz
	—	—	-3.0	dB	3735Hz
	-3.0	—	—	dB	3775Hz
	—	—	+0.5	dB	3724Hz to 3914Hz
	-3.0	—	—	dB	3875Hz
	—	—	-3.0	dB	3915Hz
	-40	—	—	dB	4040Hz
	-50	—	—	dB	4400Hz
	-50	—	—	dB	4400Hz to 150KHz
Input Impedance	10	—	—	K Ω	
Output Impedance	—	—	25	Ω	
Harmonic Distortion					V_{in} = 0 dBm, 300Hz to 3400Hz, Second or Third
	-37	—	—	dB	Harmonic Output
Intermodulation Distortion	-34	—	—	dB	V_{in} = -5.0 dBm, Each of two frequencies, (f_1 & f_2), 300Hz to 3400Hz, Intermodulation Product (2 f_1 - f_2) at 3825Hz
Output Offset Voltage	—	—	25	mV	
Current Drain	—	—	10	mA	V_{CC} = ± 15 Volts

ACF 7320C

300-3400Hz Band Pass Filter

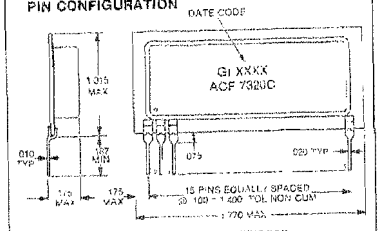
FEATURES

- Low Noise
- Low Power Dissipation
- Low In-band ripple
- 0dB Insertion loss
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7320C is a linear hybrid band pass RC active filter. The ACF 7320C provides for frequency attenuation of greater than 15dB out of the pass band frequencies of 300Hz to 3400Hz. The filter is self contained and requires no external components for proper operation. This filter is packaged in a single in line package

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Input	9	GND
2	NC	10	Negative V_{CC}
3	NC	11	Output
4	NC	12	NC
5	NC	13	NC
6	NC	14	NC
7	NC	15	NC
8	Positive V_{CC}		

NOTE: An external connection is required between Pins 2 & 3, 4 & 12, 5 & 15, and 13 & 14. Pins 6 & 7 are internal test points

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)
V_{CC} = ± 15 Volts
0°C to +70°C
Load Resistance = 5kΩ
Source Impendance = 50Ω

Characteristic	Min.	Typ	Max	Units	Conditions
Input Impedance	10	—	—	K ohms	dc to 50kHz
Gain	+0.98	0	-1.11	dB	F = 1.0kHz
Frequency Response	—	—	—	—	
dc to 170Hz	-15	—	—	dB	
300 to 3400Hz	-0.15	—	+0.15	dB	
3750 to 10000Hz	+15	-25		dB	
Input Voltage			3.0	V_{RMS}	
Output Impendance	—	—	20	ohms	
Output Noise	—	—	-70	dBm	Input & output terminated with 600 ohms
Output Distortion	—	—	1.0	percent	V_{OUT} = 3.0 V_{RMS}
Power Supply Current		5.0	10.0	mA	

7B

ACF7323C ACF7363C ACF7383C

DTMF Tone Detection Band Pass Filter

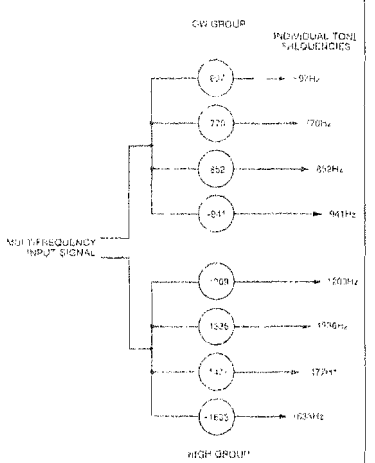
FEATURES

- Standard model tone frequency settings of 697, 770, 852, 941, 1209, 1336, 1477 and 1633 and MF frequencies of 700, 900, 1100, 1300, 1500, 1700
- ± 0.3% F_0 tolerance
- ± 0.0075%/°C F_0 temperature coefficient
- ± 0.15%/°C Q temperature coefficient
- Preset Q, 22 ±10% (4.5% B.W.)
- Filter design factory tunable over F_0 range of 500 to 5KHz and Q range of 10 to 30
- Low power consumption 72mW max at ±12VDC
- Can be operated with single-ended power supplies

DESCRIPTION

The General Instrument ACF 7323C/ACF 7363C/ACF 7383C Band Pass Active Filters are pre-tuned active filters designed specifically for tone receiver applications. These filters are available in hermetically sealed 12-lead TO-8, D.D.I.L., and S.I.L. packages.

TYPICAL APPLICATION
8-SECTION TONE FILTER



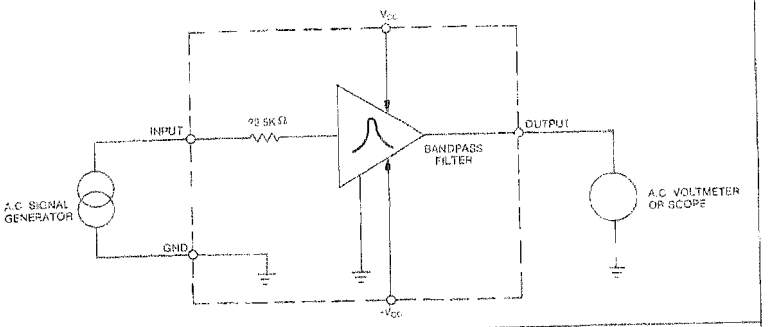
ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

$+V_{CC}$ = +12V
$-V_{CC}$ = -12V

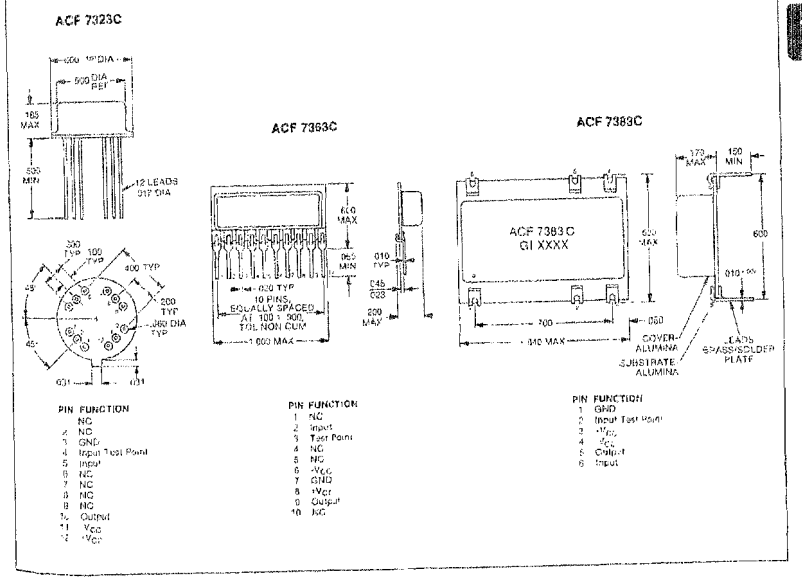
Characteristic	Min	Typ	Max.	Units	Conditions
Frequency Range	500	--	3000	Hz	Note 1
Q Range	10	--	30	--	Note 1
F_0 Accuracy	--	±0.2	±0.3	%	
F_0 Temp Coef	--	±35	±75	ppm/°C	(0°C to 70°C)
Q Accuracy	--	--	±10	%	
Q Temp Coef	--	±500	±1000	ppm/°C	(0°C to 70°C)
Voltage Gain	-1	0	+1	dB	@F_0 (0°C to 70°C)
Input Impedance	22.5	30	37.5	KΩ	
Output voltage	--	7	--	V_{RMS}	600 Ω Load
Output Impedance	--	--	1	Ω	10 to 10KHz
Output Noise	--	0.25	0.75	mV_{RMS}	10 to 10KHz
Output Offset Voltage	--	±40	±60	mV	
Positive Supply Voltage	+5	+12	+18	V	
Negative Supply Voltage	-5	-12	-18	V	
Power Supply Current @±15V	--	1.5	3.0	mA	
Operating Temp Range	0	--	70	°C	
Storage Temp Range	-55	--	150	°C	

NOTE 1:
For the eight standard models, Q is preset to 22 and F_0 is preset at the tone frequencies 697, 770, 852, 941, 1209, 1336, 1477 and 1633. The model number designation is ACF 73XXC — F_0 (e.g., ACF 7323C—0697). Other values of Q are indicated by a dash number (e.g., ACF 7323C—0697—18).

TEST CIRCUIT



PACKAGE INFORMATION
PIN CONFIGURATION



7B

ACF 7401C

Dial Tone Band Suppression Filter

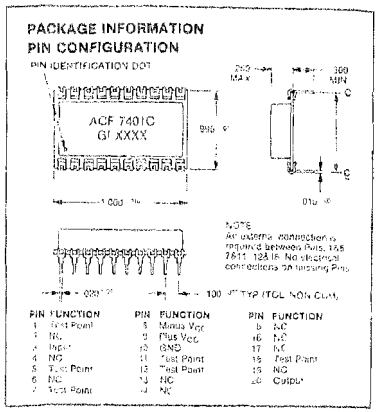
FEATURES

- 60dB Minimum attenuation at 350Hz and 440Hz
- 30dB Minimum attenuation at 80Hz
- 0dB Insertion loss in passband
- Can be operated from a single - ended power system

DESCRIPTION

The ACF 7401C is a dual tuned band suppression RC active filter which has been designed to reject frequencies of 350Hz and 440Hz, which are present on a telephone line. The unit is total self contained an requires no external components for proper operation. The filter provides for 0dB insertion loss in the pass band of 697Hz through 1633Hz, the normal DTMF Tone Frequencies. The filter also provides for 60Hz attenuation for low noise operation. This filter is packaged in a dual in line package.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	Test Point	9	Minus V_{CC}	17	NC
2	NC	10	Plus V_{CC}	18	NC
3	Input	11	GND	19	Test Point
4	NC	12	Test Point	20	Test Point
5	Test Point	13	Test Point	21	NC
6	NC	14	NC	22	Output
7	Test Point	15	NC		
8	NC	16	NC		

MAXIMUM RATINGS

V_{CC}	18 Volts
V_{CC} (Min)	5 Volts
Input Voltage Range	Power Supply Potential
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	0°C to 70°C

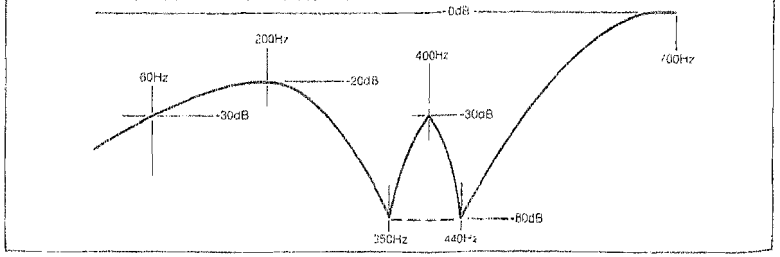
ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = 12 Volts R_S = 50Ω
R_L = 5KΩ 0°C to 70°C

Characteristics	Min	Typ	Max	Units	Conditions
Input Impedance	30	--	--	K ohms	
Input Voltage Range	—	—	V_{CC}	volts	
Frequency Response					Referenced to 941Hz Gain
60Hz	-30	—	--	dB	
350Hz	-60	—	--	dB	
440Hz	-60	—	—	dB	
680 to 1750Hz	-0.5	0	0.5	dB	
1750 to 3000Hz	-0.8	0	+0.8	dB	
16000Hz	—	-3.5	—	dB	
Output Impedance	—	—	25	ohms	
Output Voltage Range	5.	—	—	Volts p-p	
Power Supply Current	—	—	3.0	mA	

NOTE 1 Or equivalent single - ended power supply

TYPICAL FREQUENCY RESPONSE CHARACTERISTICS



ACF 7410C

2600Hz Band Suppression Filter

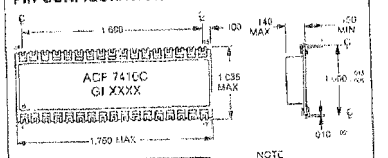
FEATURES

- 69 dB attenuation from 2585Hz to 2615Hz
- Low Power Dissipation
- Narrow Band Rejection
- Low Ripple
- Can be operated with single-ended power system

DESCRIPTION

The ACF 7410C is a linear hybrid band suppression RC Active Filter. The ACF 7410C is a sharply tuned filter designed to reject the 2600Hz signaling frequency. This filter provides for a 9 dB attenuation to match the characteristics of a passive filter system. In addition, the filter provides a minimum attenuation of 69 dB plus and minus 15Hz from the ideal center frequency of 2600Hz. This filter is packaged in a dual in line configuration.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	T.P.	9	+12VDC	18	-12VDC	26	NC
2	NC	10	NC	19	Output	27	Stage 2 Input
3	NC	11	NC	20	T.P.	28	NC
4	NC	12	T.P.	21	NC	29	Stage - Output
5	NC	13	NC	22	Stage 3 Input	30	NC
6	NC	14	NC	23	NC	31	T.P.
7	T.P.	15	NC	24	Stage 2 Output	32	Input
8	NC	16	NC	25	T.P.	33	NC
		17	GND			34	NC

MAXIMUM RATINGS

V_{CC} (Max)	±18 Volts
V_{CC} (Min)	±5 Volts
Input Voltage Range	Power Supply Potential
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	0°C to +70°C

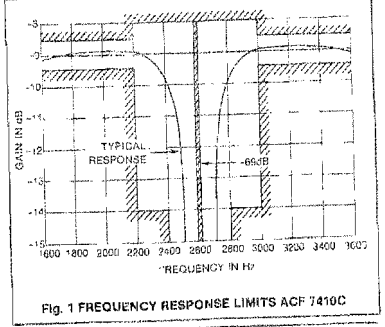


Fig. 1 FREQUENCY RESPONSE LIMITS ACF 7410C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

at V_{CC} = ±12 Volts,
T_A = 25°C
R_S = 50 Ω,
R_L = 10K

Characteristic	Min	Typ	Max	Units	Conditions
Voltage Gain	-9.5	-9.0	-8.5	dB	1000Hz
Frequency Response					Referenced from the 1000Hz Gain as 0 dB
	-0.5	0	+0.5	dB	250Hz to 220Hz
	+1.0	—	-5.0	dB	2200Hz to 2400Hz
	-60	—	--	dB	2585Hz to 2615Hz
	+1.0	—	-5.0	dB	2800Hz to 3000Hz
	-0.5	0	+0.5	dB	3000Hz to 3400Hz
Input Impedance	25	—	--	KΩ	
Output Offset Voltage	---	—	100	mV	
Output Impedance	---	—	25	Ω	
Harmonic Distortion	---	—	0.5	%	V_{OUT} = 4.0 V_{pp}, Freq = 1.0kHz
Current Drain	—	—	6.0	mA	

ACF 7480C

PRELIMINARY INFORMATION

60Hz Noise Suppression Filter

FEATURES

- Small Size
- Low Power Dissipation
- 60 dB typical attenuation
- Can be operated from single-ended power system

DESCRIPTION

The ACF 7480C is a linear hybrid RC notch active filter providing for 60 Hertz suppression. The ACF 7480C provides for a typical attenuation of 60dB plus or minus 0.1Hz from the center frequency. The filter is self contained and requires no external components for proper operation.

PACKAGE INFORMATION
PIN CONFIGURATION

NOT YET DEFINED

MAXIMUM RATINGS

V_{CC} (Max) ..... ± 18 Volts
V_{CC} (Min) ..... ± 5 Volts
Input Voltage Range ..... Power Supply Potential
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified)

V_{CC} = 15 Volts
0°C to +70°C
Load Resistance = 10KΩ
Source Impedance = 50Ω

Characteristic	Min	Typ	Max.	Units	Conditions
Input Impedance	100	—	—	K ohms	
dc to 50Hz	—	0	±0.25	dB	
57Hz, 63Hz	-3.0	—	—	dB	
59.75Hz, 60.25Hz	-40.0	—	—	dB	
59.90Hz, 60.10Hz	-50	-60.0	—	dB	
70Hz to 20KHz	—	0	-0.25	dB	
Output Impedance	—	—	25	ohms	
Output Voltage	18	—	—	Vp-p	Less than 0.5% Harmonic Distortion at 1.0KHz
Power Supply Current	—	3.0	6.0	mA	
Gain	—	0	±5	dB	Referenced to 1.0KHz

ACF 7711C

DTMF Band Separation Filter

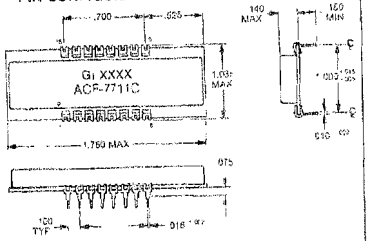
FEATURES

- Dual Filter in one package
- 25dB minimum out of band attenuation
- Low in band ripple
- 0 dB insertion loss
- 30 dB minimum out of band attenuation at 941Hz and 1209Hz respective
- Low power dissipation
- Can be operated from a single-ended power system

DESCRIPTION

The ACF 7711C is a dual RC active filter which has been designed to provide channel isolation between the low frequency group of the Tone (DTMF) frequencies of 697Hz through 941Hz, and the high frequency group of the Tone (DTMF) frequencies of 1209Hz through 1633Hz. This dual filter is packaged in a dual in line package.

PACKAGE INFORMATION
PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	Low Group Output	9	Interstage Input #4
2	Plus V_{CC}	10	Test Point #3
3	Test Point #2	11	High Group Output
4	Low Group Input	12	High Group Input
5	Interstage Output #3	13	Test Point #1
6	GND #1	14	Minus V_{CC}
7	GND #2	15	Interstage Output #2
8	Test Point #4	16	Interstage Input #1

NOTE: An external connection is required between Pins 3&13, 6&8, 6&7, 8&10, 15&16

MAXIMUM RATINGS

V_{CC} (Max) ..... ±18 Volts
V_{CC} (Min) ..... ±5 Volts
Input Voltage (at V_{CC} max) ..... ±15 Volts
Storage Temperature Range ..... -65° c to +150°C
Operating Temperature Range ..... 0°C to +70°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted)

V_{CC} = ± 12V (Note 1)
R_L = 5K Ω
R_S = 50 Ω
0°C to 70°C

Characteristic	Min	Typ	Max.	Units	Conditions
Low Group Filter Section					
Input Impedance	30	—	—	K ohms	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	941Hz Reference to 941Hz Gain
Frequency Response					
300Hz to 941Hz	-.75	0	+.75	dB	
1209Hz	-30	—	—	dB	
1209Hz to 1700Hz	-25	—	—	dB	
Output Voltage Range	±3.2	—	—	Volts	No Clipping
Output Impedance	—	—	10	ohms	
High Group Filter Section					
Input Impedance	60	—	—	K ohms	
Input Voltage Range	—	—	±12	Volts	
Gain	—	0	±0.25	dB	1209Hz Reference to 1209Hz Gain
Frequency Response					
1209Hz to 1700Hz	-.75	0	+1.5	dBp-p	
941Hz	-30	—	—	dB	
941Hz to 300Hz	-25	—	—	dB	
Output Voltage Range	±10	—	—	Volts	No Clipping
Output Impedance	—	—	10	ohms	
Power Supply Current	—	4.0	6.0	mA	

NOTE:
1. Or equivalent single - ended power supplies

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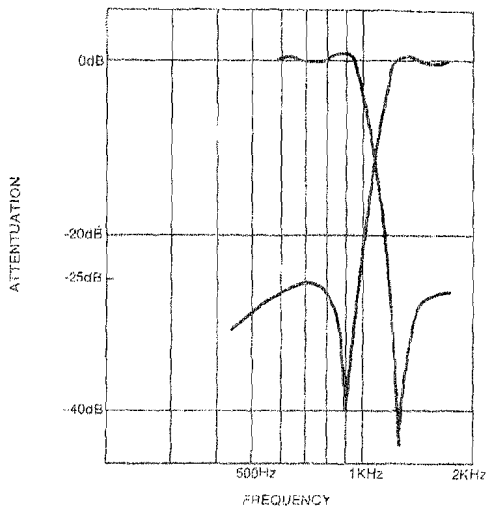


Fig.1 TYPICAL FREQ RESPONSE

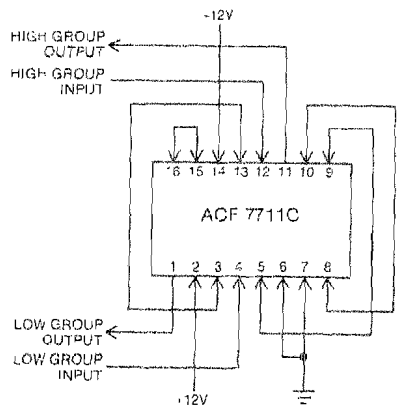


Fig.2 TONE SEPARATION FILTER TERMINATION

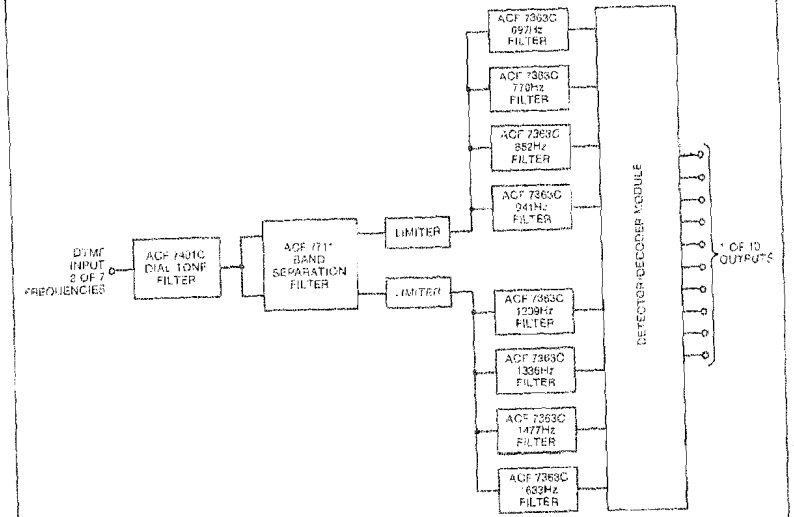
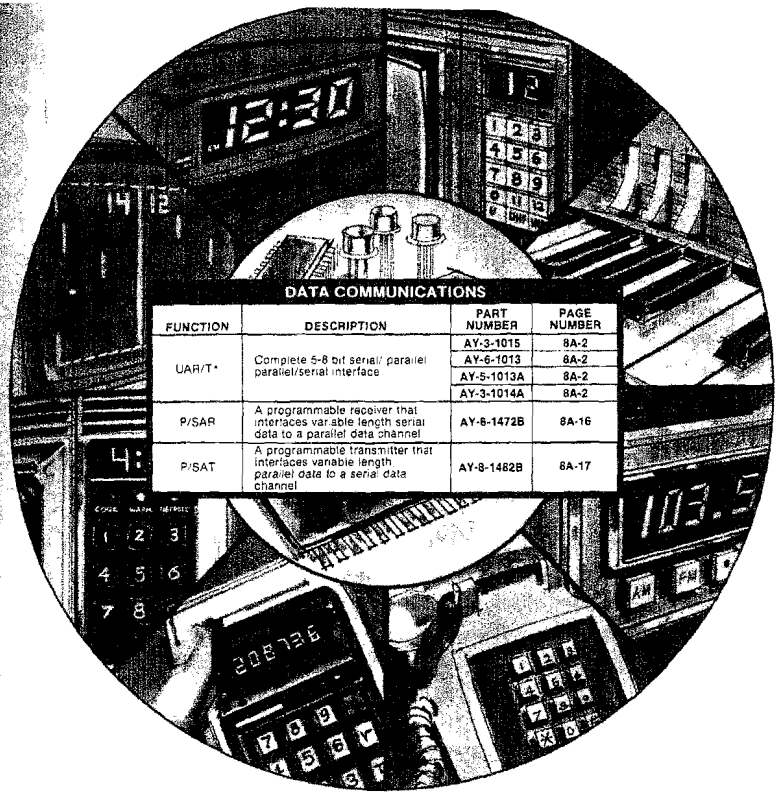


Fig.3 TYPICAL DTMF RECEIVER APPLICATION

7B



DATA COMMUNICATIONS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
UAR/T*	Complete 5-8 bit serial/ parallel parallel/serial interface	AY-3-1015	8A-2
		AY-6-1013	8A-2
		AY-5-1013A	8A-2
		AY-3-1014A	8A-2
P/SAR	A programmable receiver that interfaces variable length serial data to a parallel data channel	AY-6-1472B	8A-16
P/SAT	A programmable transmitter that interfaces variable length parallel data to a serial data channel	AY-8-1482B	8A-17

DATA COMMUNICATIONS

MICRO ELECTRONICS

8A

UAR/T Universal Asynchronous Receiver/Transmitter

FEATURES

- DTL and TLL compatible—no interfacing circuits required—drives one TTL load.
- Fully Double Buffered—eliminates need for system synchronization, facilitates high-speed operation.
- Full Duplex Operation—can handle multiple bauds. (receiving-transmitting) simultaneously
- Start Bit Verification—decreases error rate with center sampling
- Receiver center sampling of serial input; 46% distortion immunity.
- High Speed Operation.
- Three-State Outputs—bus structure capability.
- Low Power-minimum power requirements.
- Input Protected—eliminates handling problems.

AY-5-1013A
- GIANT P-channel nitride process.
- 0 to 30kbaud/0 to 40kbaud.
- Pull up resistors to V_{CC} on all inputs.

AY-6-1013
- GIANT P-channel nitride process.
- 0 to 20kbaud.
- Extended Operating Temperature Range.
  -40°C to +85°C (plastic package)
  -55°C to +125°C (ceramic package)
- Pull-up resistors to V_{CC} on all inputs.

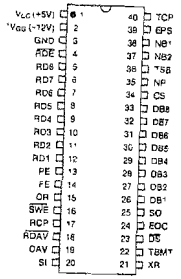
AY-3-1014A/1015
- Single Supply Operation
  +4.75V to +14V (AY-3-1014A)
  +4.75V to +5.25V (AY-3-1015)
- CMOS compatible (AY-3-1014A).
- 1⅛ stop bit mode.
- External reset of all registers.
- GIANT II N-channel Ion Implant Process
- 0 to 30k baud
- Pull-up resistors to V_{CC} on all inputs (AY-3-1015).

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1⅛ stop bit capability with the AY-3-1014A/1015), and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. The device is constructed on a single monolithic chip. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

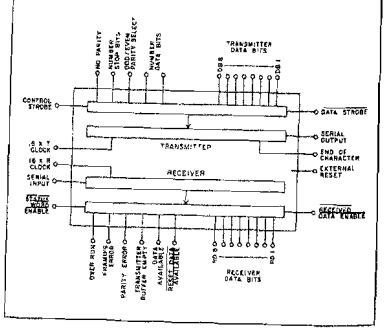
PIN CONFIGURATION
40 LEAD DUAL IN LINE

Top View



*Pin 2: AY-3-1014A/1015 — No Connection

BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name (Symbol)	Function
1	V_{CC} Power Supply (V_{CC})	-5V Supply
2	V_{GG} Power Supply (V_{GG})	-12V Supply (Not connected for AY-3-1014A/1015)
3	Ground (V_{SS})	Ground
4	Received Data Enable (RDE)	A logic "0" on the receiver enable line places the received data onto the output lines
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified; the LSB always appears on RD1. These lines have tri-state outputs; i.e., they have the normal TTL output characteristics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented
13	Parity Error (PE)	This lines goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state
16	Status Word Enable (SWE)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud
18	Reset Data Available (RDAV)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tri-state. Fig. 12,34.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 11, 12, 33, 34
21	External Reset (XR)	Resets all registers (except that the received data register is not reset in the AY-5-1013/1013A and AY-6-1013). Sets SO, EOC and TBMT to a logic "1". Resets DAV, and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer empty flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 18, 20, 40, 42
23	Data Strobe (DS)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 17, 19, 39, 41
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted. See Fig. 15.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. If not used, this lead must be tied to a logic "0"
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. For the AY-3-1014A/1015, the combined selection of 2 stop bits and 5 bits/character will produce 1⅛ stop bits
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud

8A

TRANSMITTER OPERATION

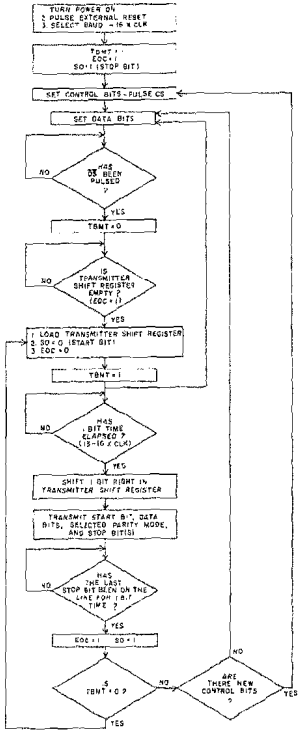


Fig.1

Initializing

Power is applied, external reset is enabled and clock pulse is applied having a frequency of 16 times the desired baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits with control bits selection *normally occurring before* data bits selection. However, one may set both $\overline{DS}$ and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe ($\overline{DS}$) is pulsed the TBMT signal will change from a logic "1" to a logic "0" indicating that the data bits holding register is filled with a previous character and is unable to receive new data bits, and transmitter shift register is transmitting previously loaded data. TBMT will *return* to a logic "1". When transmitter shift register is empty, data bits in the holding register *are immediately loaded* into the transmitter shift register for transmission. The shifting of information from the holding register to the transmitter shift register will be followed by SO and EOC going to a logic "0", and TBMT will also go to a logic "1" indicating that the shifting operation is completed and that the data bits holding register is ready to accept new data. *It should be* remembered that one full character time is now available for *loading* of the next character without loss in transmission speed due to double buffering (separate data bits holding register and transmitter shift register).

Data transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit(s). When the last stop bit *has been on line for one bit time*, EOC will go to a logic "1" indicating that new character is ready for transmission. This new character will be transmitted only if TBMT is a logic "0" as was previously discussed

RECEIVER OPERATION

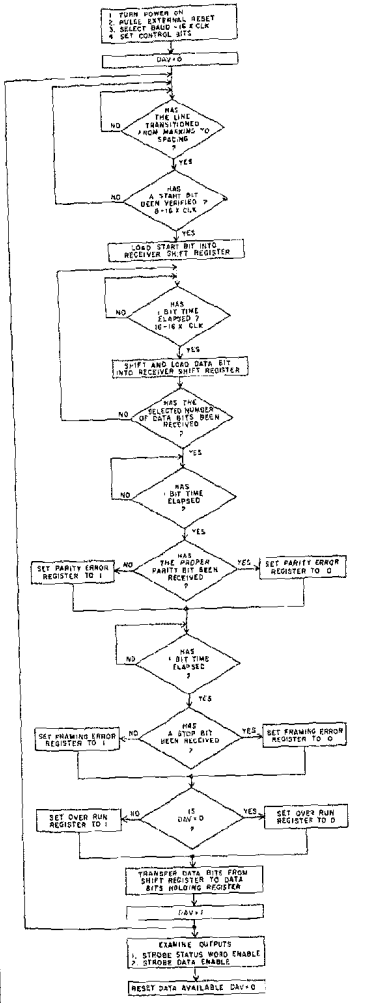


Fig.2

Initializing

Power is applied, external reset is enabled, *and clock pulse is* applied having a frequency of 16 times the desired baud. The previous conditions will set data available (DAV) to a logic "1"

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. *Data reception starts* when serial input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0", when center sampled, 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions *from a logic "1" to a logic "0" (marking to spacing)* when the 16x clock is in a logic "1" state, the bit time, for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the perity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0"

Once a full character is received, internal logic locks at the data available (DAV) signal to determine if data has been the read out If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the status word *holding register will be set to a logic "1"* If the DAV signal is at a logic "0" the receiver will assume that data has been read out After DAV goes to a *logic "1", the receiver shift register* is now ready to accept the next character and has one full character time to remove the received character.

8A

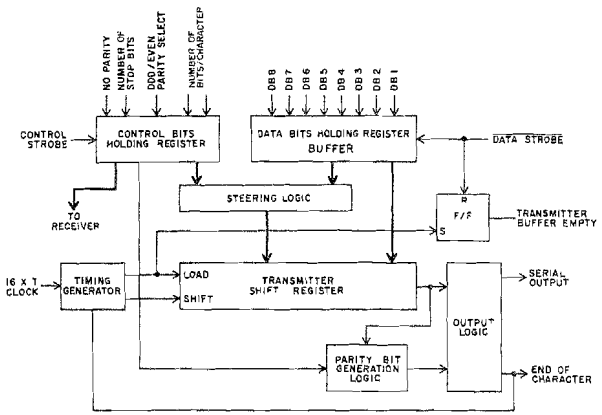


Fig.3 TRANSMITTER BLOCK DIAGRAM

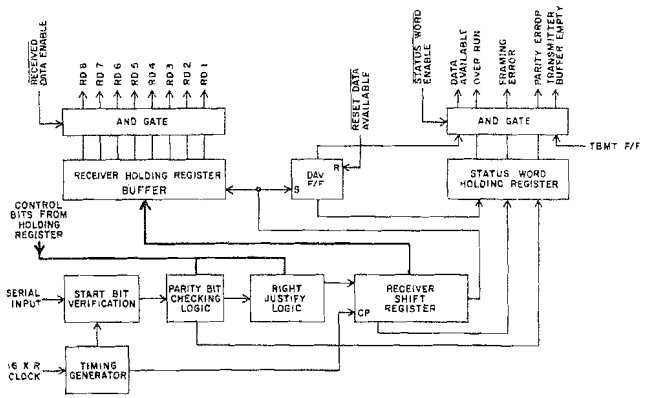


Fig.4 RECEIVER BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} (with respect to V_{CC})	-20 to +0.3V
Clock and logic input voltages (with respect to V_{CC})	-20 to +0.3V
Storage Temperature	-65° C to +150° C
Lead Temperature (soldering, 10 seconds)	+330° C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied --operating ranges are specified below

Standard Conditions (unless otherwise noted)

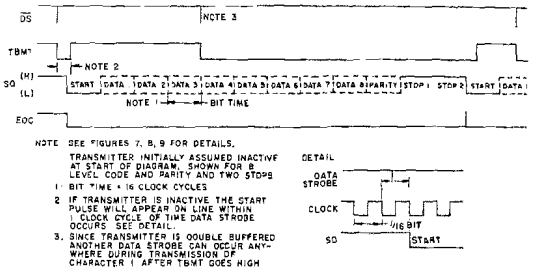
V_{GG} = -12V ±5%
V_{CC} = +5V ±5%
Temperature (T_A) = 0°C to +70°C (AY-5-1013A)
-40 C to +85°C (AY-6-1013 Plastic Package)
-55C to +125°C (AY-6-1013 Ceramic Package)

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					(I_{IL} = -1.6mA max.)
Logic 0	0	--	0.8	Volts	Unit has internal pullup resistors
Logic 1	V_{CC}-1.5	--	V_{CC}+0.3	Volts	
Input Capacitance					
All Inputs	--	--	20	pF	0 volts bias, f= 1MHz
Leakage Currents					
Three State Outputs	--	--	1.0	µA	0 volts
Data Output Levels					
Logic 0	--	--	+0.4	Volts	I_{OL}= 1.6mA (sink)
Logic 1	V_{CC}-1.0	--	--	Volts	I_{OH}= 3mA (source)
Output Capacitance	--	10	15	pF	See Fig.25
Short Ckt. Current	--	--	--	--	
Power Supply Current					AY-5-1013/1013A - See Fig.25
I_{GG}	--	14	16	mA	AY-6-1013 - See Fig.25
I_{CC} } 25°C all inputs -5V	--	17	19	mA	AY-5-1013/1013A - See Fig 26
	--	18	20	mA	AY-6-1013
	--	21	23	mA	
AC CHARACTERISTICS					T_A = 25°C, output load capacitance 50pF max
Clock Frequency	DC	--	640	KHz	AY-5-1013A
	DC	--	360	KHz	AY-6-1013
Baud	0	--	40	Kbaud	AY-5-1013A
	0.	--	22.5	Kbaud	AY-6-1013
Pulse Width					
Clock Pulse	750	--	--	ns	AY-5-1013A - See Fig.9
	1.5	--	--	µs	AY-6-1013-See Fig.9
Control Strobe	300	--	--	ns	AY-5-1013A-See Fig 15
	600	--	--	ns	AY-6-1013
Data Strobe	190	--	--	ns	AY-5-1013A-See Fig 14
	250	--	--	ns	AY-6-1013
External Reset	500	--	--	ns	AY-5-1013A - See Fig. 13
	1.0	--	--	µs	AY-6-1016
Status Word Enable	500	--	--	ns	AY-5-1013A - See Fig. 21
	600	--	--	ns	Ay-6-1013 - See Fig 21
Reset Data Available	250	--	--	ns	Ay-5-1013A - See Fig. 22
	350	--	--	ns	AY-6-1013 - See Fig. 22
Received Data Enable	500	--	--	ns	AY-5-1013A - See Fig. 21
	600	--	--	ns	AY-6-1013 - See Fig. 21
Set Up & Hold Time					
Input Data Bits	0	--	--	ns	See Fig.14
Input Control Bits	0	--	--	ns	See Fig.15
Output Propagation Display					
TPD0	--	--	500	ns	AY-5-1013A - See Fig. 21 & 24
	--	--	650	ns	AY-6-1013 - See Fig. 21 & 24
TPD1	--	--	500	ns	Ay-5-1013A - See Fig. 21 & 24
	--	--	650	ns	AY-6-1013 - See Fig. 21 & 24

**Typical values are at +25° C and nominal voltages

8A

TIMING DIAGRAMS



NOTE SEE FIGURES 7, 8, 9 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM, SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS

1. BIT TIME = 16 CLOCK CYCLES
2. IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE WITHIN 1 CLOCK CYCLE OF TIME DATA STROBE OCCURS. SEE DETAIL.
3. SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISSION OF CHARACTER 1 AFTER TBMT GOES HIGH

Fig.5 UAR/T TRANSMITTER TIMING

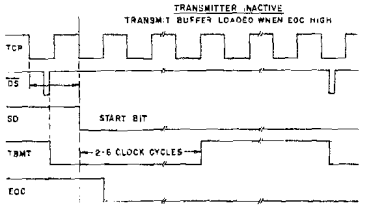


Fig.6 TRANSMITTER AT START BIT

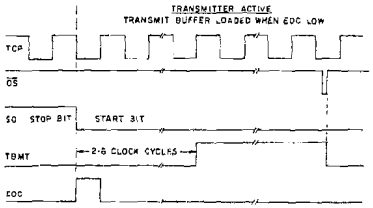
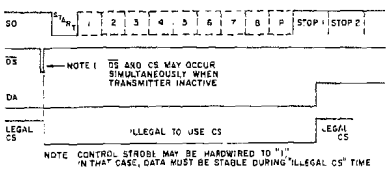
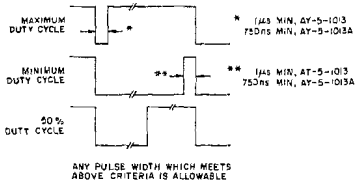


Fig.7 TRANSMITTER AT START BIT



NOTE CONTROL STROBE MAY BE HARDWIRED TO "1". IN THAT CASE, DATA MUST BE STABLE DURING "ILLEGAL CS" TIME

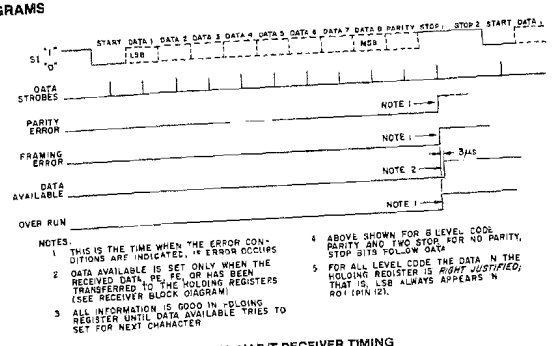
Fig.8 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE

Fig.9 ALLOWABLE TCP, RCP

TIMING DIAGRAMS



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM)
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RO1 (PIN 12).

Fig.10 UAR/T RECEIVER TIMING

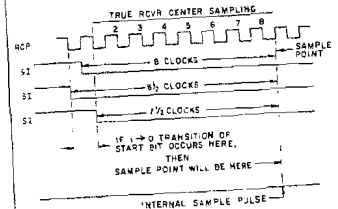


Fig.11

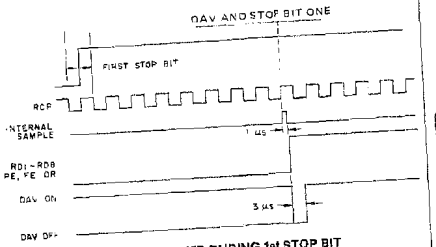
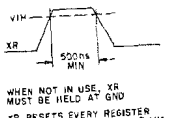


Fig.12 RECEIVER DURING 1st STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND

XR RESETS EVERY REGISTER EXCEPT CONTROL REGISTER AND RECEIVED DATA. SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V

Fig.13 XR PULSE

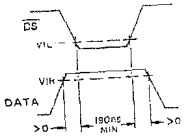
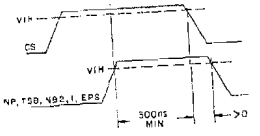
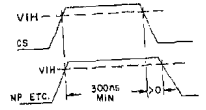


Fig.14 DS



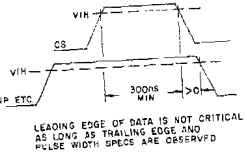
CONTROL BITS MUST BE STABLE FOR LAST 300ns OF CS

Fig.15a CS



CONTROL STROBE AND CONTROL BITS MUST BE 300ns MINIMUM

Fig.15b CS



LEADING EDGE OF DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED

Fig.15c CS

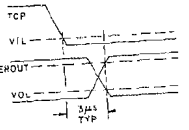


Fig.16

8A

TIMING DIAGRAMS

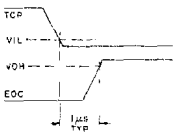


Fig.17 EOC TURN-ON

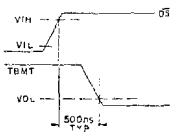


Fig.18 TBMT TURN-OFF

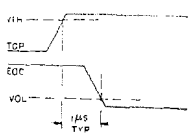


Fig.19 EOC TURN-OFF

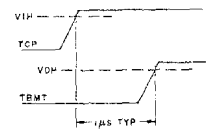


Fig.20 TBMT TURN-ON

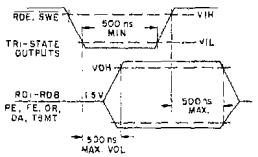


Fig.21 RDE, SWE

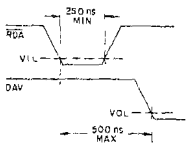


Fig.22 RDAV

TYPICAL CHARACTERISTIC CURVES

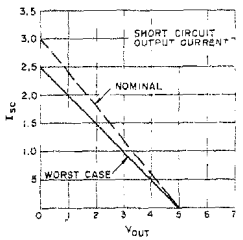


Fig.23 SHORT CIRCUIT OUTPUT CURRENT

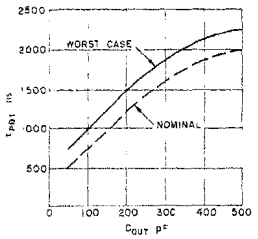


Fig.24 RE1, RD8, PE, FE, OR. TBMT, DAV

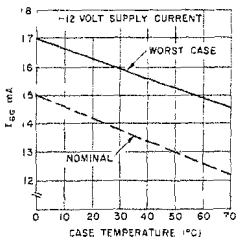


Fig.25 -12 VOLT SUPPLY CURRENT

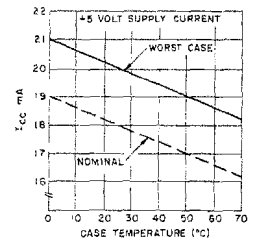


Fig.26 +5 VOLT SUPPLY CURRENT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with respect to V_{GI})	−0.3 to +16V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering 10 sec)	+330°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied —operating ranges are specified below.

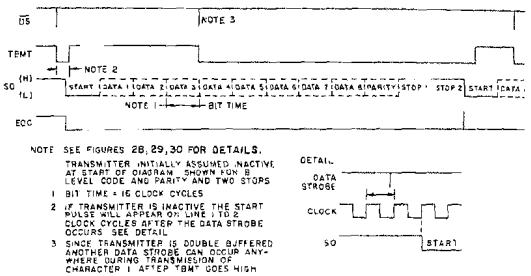
Standard Conditions (unless otherwise noted)

V_{CC} = +4.75 to −14V (AY-3-1014A)
V_{CC} = +4.75V to +5.25V (AY-3-1015)
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels (AY-3-1014A)					
Logic 0	0	—	0.8	Volts	
Logic 1 at V_{CC} = +4.75V	2.0	—	V_{CC} +0.3	Volts	
at V_{CC} = +14V	3.0	—	V_{CC} +0.3	Volts	
Input Logic Levels (AY-3-1015)					
Logic 0	0	—	0.8	Volts	AY-3-1015 has internal pull-up resistors to V_{CC}
Logic 1	2.0	—	V_{CC}+0.3	Volts	0 volts bias, f = 1 MHz
Input Capacitance					
All inputs	—	—	20	pF	
Output Impedance					
Tri-State Outputs	1.0	—	—	MΩ	
Data Output Levels					I_{OL} = 1.6mA (sink)
Logic 0	—	—	+0.4	Volts	I_{OH} = -40µA (source) - at V_{CC} = +5V
Logic 1: AY-3-1014A/1015	2.4	—	—	Volts	I_{OH} = -50µA (source) - at V_{CC} = +14V
AY-3-1014A only	3.5	—	—	Volts	
Output Capacitance	—	10	15	pF	See Fig.45.
Short Ckt. Current	—	—	—	—	
					See Fig 47.
Power Supply Current					
I_{CC} at V_{CC} = +5V (AY-3-1014A)	—	10	15	mA	See Fig.48
I_{CC} at V_{CC} = +14V (AY-3-1014A)	—	14	20	mA	
I_{CC} at V_{CC} = -5V (AY-3-1015)	—	10	15	mA	
A.C. CHARACTERISTICS					T_A = 25°C. Output load capacitance 50 pF max at V_{CC} = +4.75V/+14V at V_{CC} = −4.75V/+14V
Clock Frequency	DC	—	480/400	KHz	
Baud	0	—	30/25	Kbaud	See Fig.31
Pulse Width					
Clock Pulse	3.0	—	—	µs	See Fig.37
Control Strobe	200	—	—	ns	See Fig.36
Data Strobe	200	—	—	ns	See Fig.35
External Reset	500	—	—	ns	See Fig.43
Status Word Enable	500	—	—	ns	See Fig 44
Reset Data Available	200	—	—	ns	See Fig.43
Received Data Enable	500	—	—	ns	
Set Up & Hold Time					See Fig36
Input Data Bits	20	—	—	ns	See Fig.37
Input Control Bits	20	—	—	ns	
Output Propagation Delay					See Fig.43 & 46
TPD0	—	—	500	ns	See Fig.43 & 46
TPD1	—	—	500	ns	

**Typical values are at +25° C and nominal voltages

8A



NOTE SEE FIGURES 28, 29, 30 FOR DETAILS.

TRANSMITTER INITIALLY ASSUMED INACTIVE AT START OF DIAGRAM. SHOWN FOR 8 LEVEL CODE AND PARITY AND TWO STOPS

1. BIT TIME = 16 CLOCK CYCLES
2. IF TRANSMITTER IS INACTIVE THE START PULSE WILL APPEAR ON LINE 1 TO 2 CLOCK CYCLES AFTER THE DATA STROBE OCCURS. SEE DETAIL.
3. SINCE TRANSMITTER IS DOUBLE BUFFERED ANOTHER DATA STROBE CAN OCCUR ANYWHERE DURING TRANSMISION OF CHARACTER 1 AFTER "TBMT" GOES HIGH

Fig.27 UAR/T-TRANSMITTER TIMING

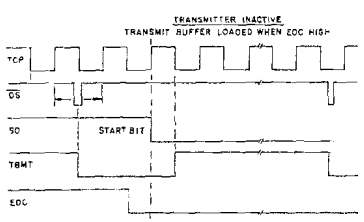


Fig.28 TRANSMITTER AT START BIT

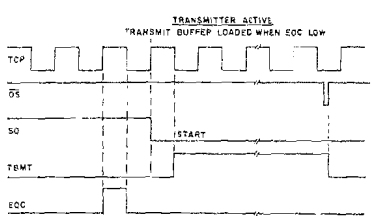
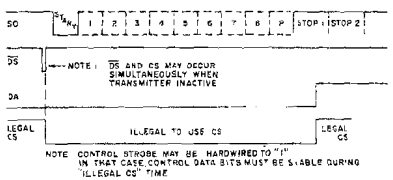
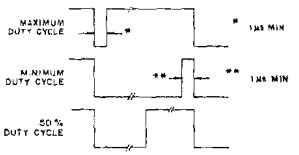


Fig.29 TRANSMITTER AT START BIT



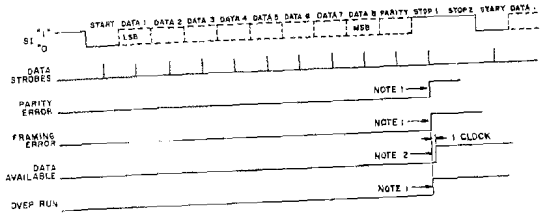
NOTE CONTROL STROBE MAY BE HARDWIRED TO "1" IN THAT CASE CONTROL DATA BITS MUST BE STABLE DURING "ILLEGAL CS" TIME

Fig.30 ALLOWABLE POINTS TO USE CONTROL STROBE



ANY PULSE WIDTH WHICH MEETS ABOVE CRITERIA IS ALLOWABLE

Fig.31 ALLOWABLE TCP, RCP



NOTES:

1. THIS IS THE TIME WHEN THE ERROR CONDITIONS ARE INDICATED, IF ERROR OCCURS
2. DATA AVAILABLE IS SET ONLY WHEN THE RECEIVED DATA, PE, FE, OR HAS BEEN TRANSFERRED TO THE HOLDING REGISTERS (SEE RECEIVER BLOCK DIAGRAM)
3. ALL INFORMATION IS GOOD IN HOLDING REGISTER UNTIL DATA AVAILABLE TRIES TO SET FOR NEXT CHARACTER
4. ABOVE SHOWN FOR 8 LEVEL CODE PARITY AND TWO STOP. FOR NO PARITY, STOP BITS FOLLOW DATA
5. FOR ALL LEVEL CODE THE DATA IN THE HOLDING REGISTER IS *RIGHT JUSTIFIED*; THAT IS, LSB ALWAYS APPEARS IN RO1 (PIN 12)

Fig.32 UAR/T RECEIVER TIMING

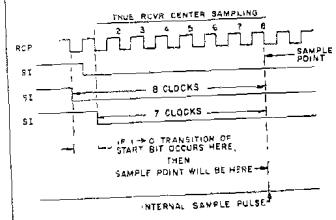


Fig.33

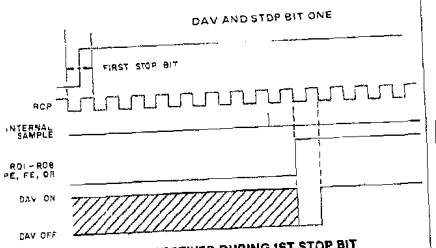
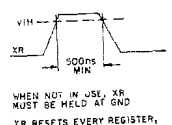


Fig.34 RECEIVER DURING 1ST STOP BIT



WHEN NOT IN USE, XR MUST BE HELD AT GND

XR RESETS EVERY REGISTER, SO, TBMT, EOC ARE RESET TO 5V ALL OTHER OUTPUTS RESET TO 0V.

Fig.35 XR PULSE

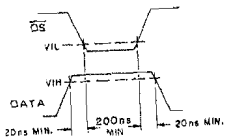
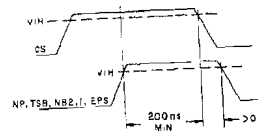
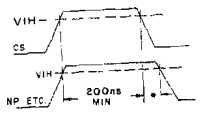


Fig.36 DS



CONTROL BITS MUST BE STABLE FOR LAST 200ns OF CS

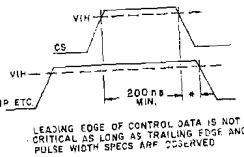
Fig.37a CS



CONTROL STROBE AND CONTROL BITS MUST BE 400ns MINIMUM

* 20ns MIN

Fig.37b



LEADING EDGE OF CONTROL DATA IS NOT CRITICAL AS LONG AS TRAILING EDGE AND PULSE WIDTH SPECS ARE OBSERVED

Fig.37c

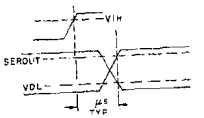


Fig.38 SEROUT

8A

TIMING DIAGRAMS

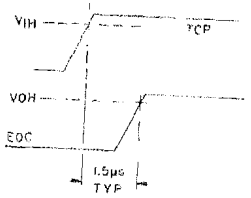


Fig.39 EOC TURN-ON

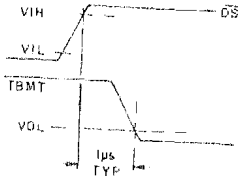


Fig.40 TBMT TURN-OFF

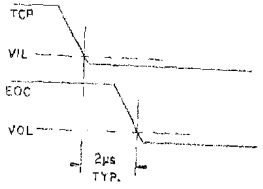


Fig.41 EOC TURN-OFF

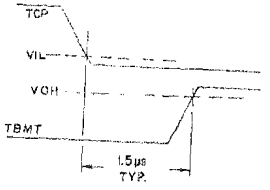


Fig.42 TBMT TURN-ON

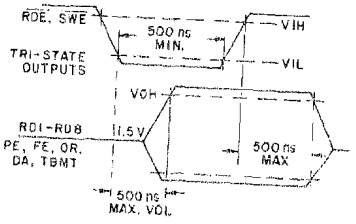


Fig.43 RDE, SWE

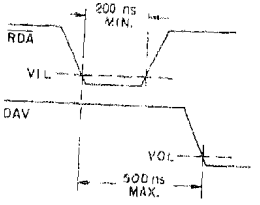


Fig.44 RDAV

TYPICAL CHARACTERISTIC CURVES

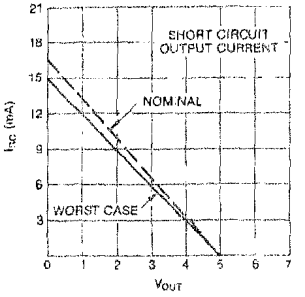


Fig.45 SHORT CIRCUIT OUTPUT CURRENT
(only 1 output may be
shorted at a time)

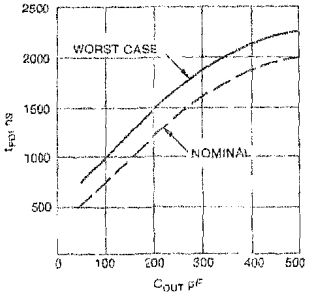


Fig.46 RD1-RD8, PE, FE, OR, TBMT, DAV

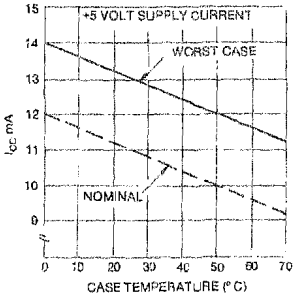


Fig.47 +5 VOLT SUPPLY CURRENT

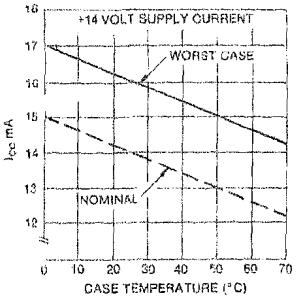


Fig.48 +14 VOLT SUPPLY CURRENT
(AY-3-1014A only)

8A

P/SAR Programmable Synchronous Asynchonous Receiver

FEATURES

- Directly TTL & DTL Compatible — Internal Active Input Pull-Up Devices & Push-Pull Output Buffers.
- Programmable Mode & Clock Rate Selection — Asynchronous & Isochronous — 1X, 16X, 32X or 64X Clock Rate; Synchronous — Internal or External Character Synchronization.
- Programmable Transmission Codes — Character Length of 5, 6, 7 or 8 data bits plus Parity; Parity Inhibit
- DC High Speed Operation — Bit Rate to 100K Bits/Sec with 1X Clock
- Double Buffered Receiver

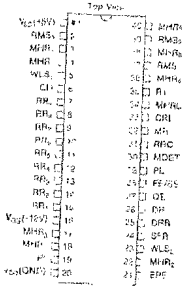
DESCRIPTION

The General Instrument AY-8-1472B P/SAR is a Programmable Receiver that interfaces variable length serial data to a parallel data channel. The receiver converts a serial data stream into parallel characters with a format compatible with all standard Synchronous, Asynchronous, or Isochronous data communications media.

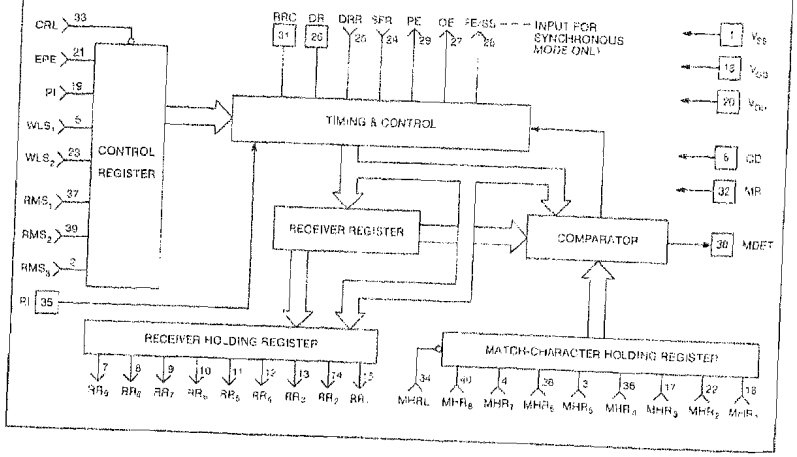
Contiguous synchronous serial characters are compared in a programmable Match-Character Holding Register, character synchronized and assembled. Programming the Asynchronous or Isochronous Mode provides assembly of characters with start and stop bit (s) which are stripped from the data. Four internal registers, in conjunction with Tri-State Output lines provide full-s system versatility

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



p/SAT Programmable Synchronous Asynchronous Transmitter

FEATURES

- Directly TTL & DTL Compatible — Internal Active Input Pull-Up Devices & Push-Pull Output Buffers
- Programmable Mode Selection — Synchronous — Programmable Fill (Idle) Character, Isochronous — Programmable Fill Character with Start & Stop Bit; Asynchronous — Single or Double Stop Bit Generation with 1.5 Stop Bits or 5-level Codes
- Programmable Transmission Codes — Character Length of 5, 6, 7 or 8 data bits plus Parity, Even/Odd Parity Generation, Parity Inhibit
- Programmable Clock Rate — Asynchronous & Isochronous Mose Selectable Divider Ratios for 1X, 16X, 32X or 64X Clock Rate.
- DC to High Speed Operation — Bit Rate to 100K Bits/Sec with 1X Clock
- Double Buffered Transmitter

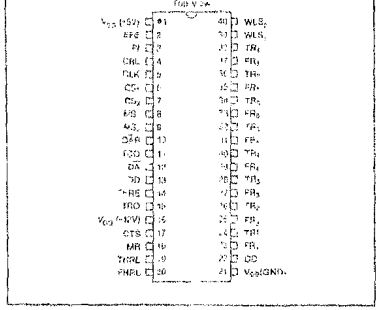
DESCRIPTION

The General Instrument AY-8-1482B P/SAT is a Programmable Transmitter that interfaces variable length parallel input data to a serial channel. The Transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isochronous data communication media.

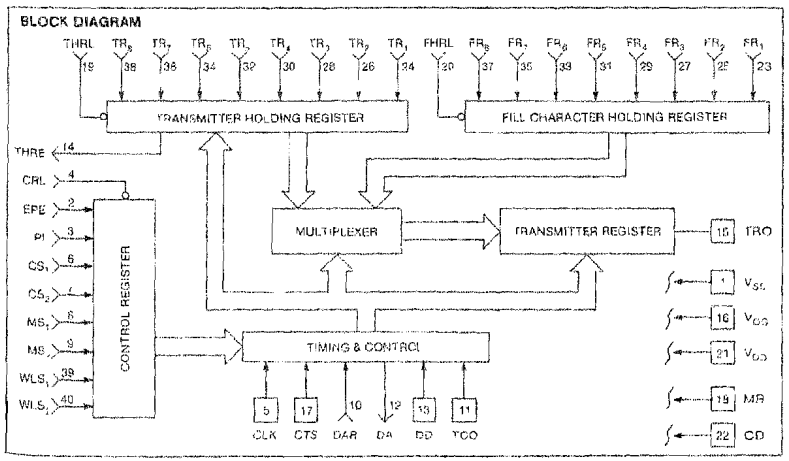
Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous mode provides "Start-Stop" serial data transmission with automatic insertion of Start and Stop Bit(s). Isochronous mode selection provides data transmission with a single Start and Stop Bit with the added capability of programmable Fill (Idle) Character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Tri-State Output Lines, provide full system versatility

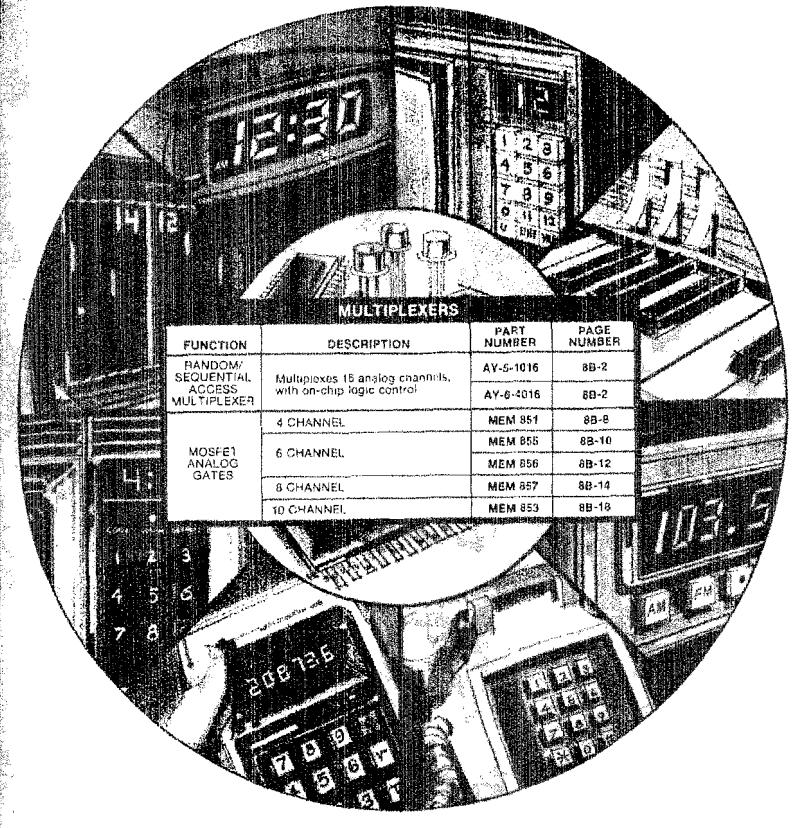
PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM





MULTIPLEXERS

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
RANDOM/ SEQUENTIAL ACCESS MULTIPLEXER	Multiplexes 16 analog channels, with on-chip logic control	AY-5-1016	8B-2
		AY-6-1016	8B-2
MOSFET ANALOG GATES	4 CHANNEL	MEM 851	8B-8
	6 CHANNEL	MEM 855	8B-10
		MEM 856	8B-12
	8 CHANNEL	MEM 857	8B-14
	10 CHANNEL	MEM 853	8B-18

8B

MULTIPLEXERS

MICRO ELECTRONICS

Random/Sequential Access Multiplexers

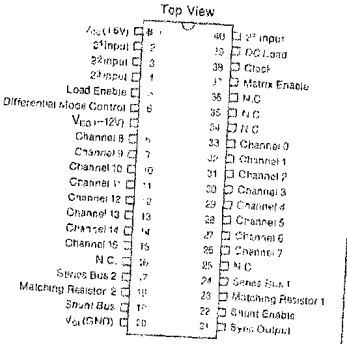
FEATURES

- Directly interfaces with TTL/DTL and MOS.
- Current or voltage modes of operation
- Random or sequential access.
- Single ended or differential operation.
- Expandable in either the sequential or random access modes.
- Programmable length counter for sequential applications
- DC to 2MHz operation.
- Extremely high off-resistance
- Choice of Operating Temperature Ranges:
  AY-5-1016 — 0°C to +70°C
  AY-6-4016 — −55°C to +125°C
- Zener network protection on all input leads

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View

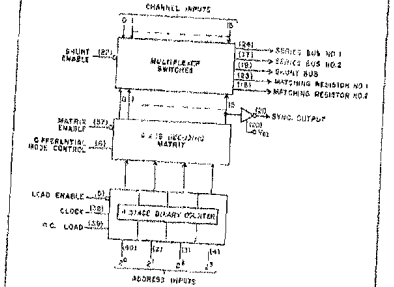


DESCRIPTION

The AY-5-1016 and AY-6-4016 are each a 16 Channel Random/Sequential Access Multiplexer containing a programmable 4 stage binary counter, a 4 × 16 decode matrix, and 16 single-pole double-throw switches.

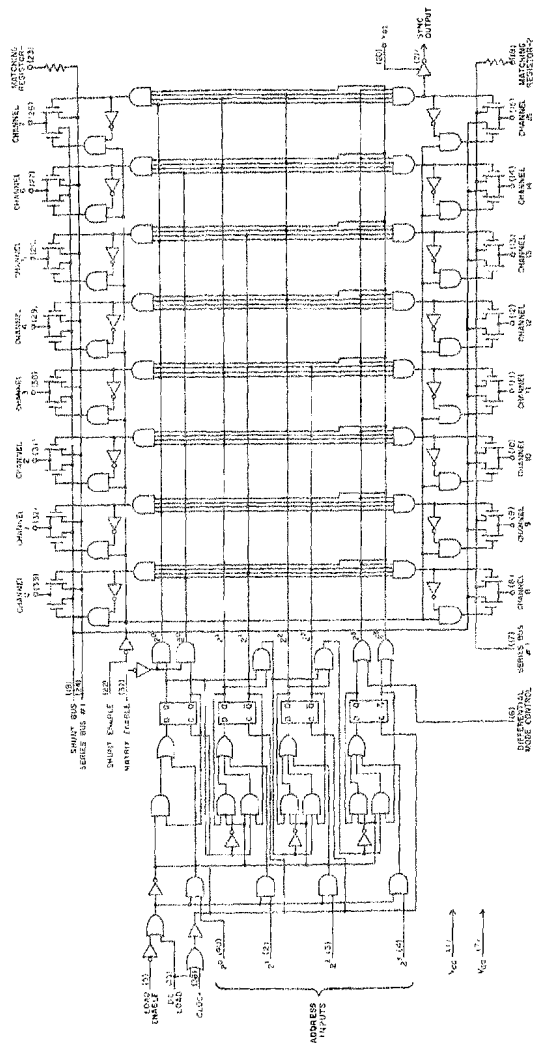
The Shunt Enable control line permits the selection of Current Mode or Voltage Mode operation and in conjunction with the Current Mode, matching resistors are provided to improve accuracy. The Differential Mode Control allows the switches to operate as eight ganged pairs, while the Matrix Inhibit line allows multiple AY-5-1016's (or AY-6-4016's) to be connected to form larger multiplexing arrays. The Load Enable control allows synchronous loading of the 4 address inputs on a low to high transition of the Clock. The DC load control is provided for asynchronous loading of the address inputs independent of the Clock and Load Enable inputs. The Sync Output occurs whenever Channel 15 is selected and is provided to allow expansion in the sequential mode of operation. Also by connecting the Sync Output to the Load Enable input, the counter length can be programmed via the address inputs. Any desired length of from 1 to 16 states can be programmed in this manner.

BLOCK DIAGRAM



LOGIC DIAGRAM

( ) = Pin Numbers



NOTES:
1. Direct Address gated when either DC Load = "1" or Load Enable = "0"
2. DC Load gives permanent high clock
3. Matrix Enable = "1" resets matrix
4. Shunt Enable = "0" connects shunt FETS into circuit
5. Differential Mode Control = "1" connects channels 8-15 ganged to channels 0-7
6. Sync Output = "0" when counter "5" is accessed

ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{BB} and V_{GG} (with respect to V_{CC})	−20V to +0.3V
Clock and Logic Input Voltages (with respect to V_{CC})	−20V to +0.3V
Bus Voltages (Bus 1, Bus 2, and Shunt Bus with respect to V_{CC})	−20V to .3V
Matching Resistor Nodes (with respect to V_{CC})	−20V to .3V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	0°C to +70°C (AY-5-1016)
	−55°C to +125°C (AY-6-4016)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise stated)

V_{CC} = +5 Volts ±0.5 Volts (V_{CC} — Substrate voltage)
V_{BB} = −12 Volts ±1 Volt
V_{GG} = GND

Operating Temperature (T_A) = 0°C to +70°C (AY-5-1016)
−55°C to +125°C (AY-6-4016)

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Inputs (See Fig.1)					
Repetition Rate	DC	—	2.0	MHz	
Clock Pulse Width (ϕ_{PW})	200	—	—	ns	at 2MHz (See NOTE 1)
Clock Pulse Width (ϕ_{PW})	1.0	—	—	µs	at 200Hz
Clock Pulse Delay (ϕ_d)	200	—	—	ns	See NOTE 1
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	12	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = −5V to −5V
Rise & Fall Time (tr, tf)	—	—	1.0	µs	at 100KHz
Rise & Fall Time (tr, tf)	—	—	50	ns	at 2MHz
Noise Immunity	+0.4	—	—	V	
Address Inputs (See Fig.1)					
Clock Lead Time	360	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = −5V to −5V
Noise Immunity	+0.4	—	—	V	
Load Enable Input (See Fig.1)					
Clock Lead Time	300	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
DC Load Input (See Fig.2)					
Pulse Width (90% points)	400	—	—	ns	
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	8	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	−0.4	—	—	V	

**Typical values are at +25°C and nominal voltages
NOTE 1: $\phi_{PW} + \phi_d \geq 500$ns

TIMING DIAGRAMS

Fig.1

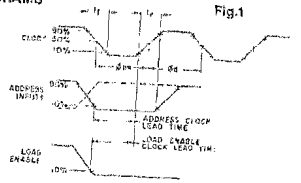
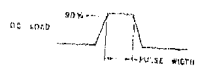


Fig.2



NOTE: Address inputs and the Load Enable Input must be present during the 0 to 1 transition of the Clock.

Characteristic	Min	Typ**	Max	Units	Conditions
Shunt Enable					
Logic Levels					
Logic "0"	—	—	+0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	6	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = +5V to −5V
Noise Immunity	+0.4	—	—	V	
Matrix Enable					
Response Time (See Fig. 3)					
T_{ON}	—	220	—	ns	} at 25°C Output voltage
T_{OFF}	—	120	—	ns	} response with10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	7	—	pF	
Input Impedance	1.0	—	—	MΩ	V_{IN} = −5V to +5V
Noise Immunity	+0.4	—	—	V	
Differential Mode Control					
Response Time (See Fig. 4)					
T_{ON}	—	200	—	ns	} at 25°C Output voltage
T_{OFF}	—	600	—	ns	} response with 10 MΩ, 10 pF load
Logic Levels					
Logic "0"	—	—	0.8	V	
Logic "1"	V_{CC}−1.5	—	—	V	
Input Capacitance	—	5	—	pF	
Input Impedance	1.0	—	—	MΩ	
Noise Immunity	0.4	—	—	V	
Series Switches					
R on (Current Mode)	—	460	750	Ohms	I_{IN} = 100 µA Series Bus 1 - Series Bus 2 = 0V (V_{B1} = 5V) T_A = 25°C V_{CC} = +5V V_{BB} = −12V
R on (Voltage Mode)	—	300	500	Ohms	V_{IN} = +5V, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{BB} = −12V
	—	460	750	Ohms	V_{IN} = 0V, R_L = 300 KΩ T_A = 25°C V_{CC} = +5V V_{BB} = −12V
R off	—	5	—	GΩ	V_{IN} = V_{BB}=10V T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ 10 pF load T_A = 25°C

**Typical values are at 25°C and nominal voltages

TIMING DIAGRAMS

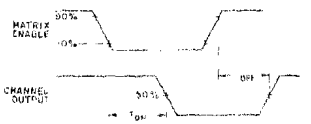


Fig.3

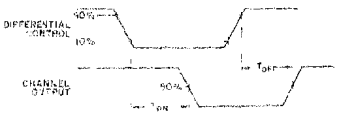


Fig.4

8B

Characteristic	Min	Typ**	Max	Units	Conditions
Sync Output (See Fig.5)					
Logic "0"	—	—	+0.4	V	I_{SINK} = 1.6mA min, I_{OH} = 100 µA min. } Output Load
Logic "1"	V_{CC}−1.0	—	—	V	
Rise Time (tr)	—	110	—	ns	at 25°C
Fall Time (tf)	—	40	—	ns	at 25°C
Response Time					
tpd −	—	200	—	ns	at 25°C
tpd +	—	160	—	ns	at 25°C
Input Leakage					
Channels 0-15 (Per Channel)	—	1.0	10	nA	$V_{IN} = V_{CC}$ −5V at 25°C
Series Bus 1, 2	—	3.0	30	nA	$V_{BUS} = V_{CC}$ −5V at 25°C
Shunt Bus	—	3.0	30	nA	$V_{BUS} = V_{CC}$ −5V at 25°C
Shunt Switches					
R on	—	850	1300	Ohms	I_{IN} = 100 µA, Shunt Bus = 0V, V_{CC} = +5V, V_{EE} = −12V, T_A = 25°C
	—	550	900	Ohms	I_{IN} = 100 µA, Shunt Bus = +5V, V_{CC} = +5V, V_{EE} = −12V, T_A = 25°C
R off	—	5	—	GΩ	$V_{IN} = V_{CC}$ −10V, T_A = 25°C
Turn On Time	—	300	—	ns	Output Voltage Waveform with 10 MΩ, 10 pF load, T_A = 25°C
Matching Resistors	—	460	750	Ohms	I_{IN} = 100 µA, V_{BUS} = 0V
R on	—	300	500	Ohms	I_{IN} = 100 µA, V_{BUS} = +5V
Channel Input Capacitance Channels 0-15 (Per Channel)	—	4	—	pF	
Power Consumption	—	200	—	mW	Series MODE } V_{EE} = −12V
	—	390	—	mW	Shunt MODE } V_{CC} = +5V
Current Drain					
I_{CC}	—	12	—	mA	Series MODE } V_{EE} = −12V
I_{EE}	—	12	—	mA	Series MODE } V_{EE} = −12V
I_{CC}	—	17	—	mA	Shunt MODE } V_{CC} = +5V
I_{EE}	—	17	—	mA	Shunt MODE } V_{CC} = +5V
Power Dissipation (Device)	—	—	600	mW	
Per Channel	—	—	100	mW	

** Typical values are at 25°C and nominal voltages

TIMING DIAGRAMS

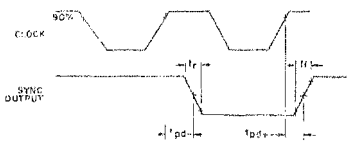
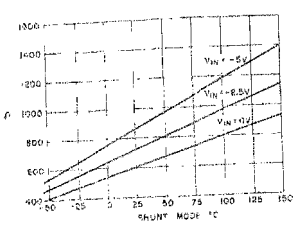
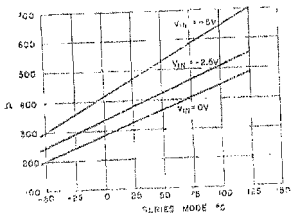
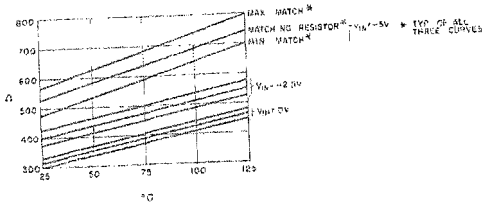


FIG.5

TYPICAL CHARCTERISTIC CURVES







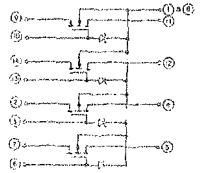
8B

Four Channel MOSFET Analog Gate

FEATURES

- 30 volt peak-peak signal input range
- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- Low "on" Resistance
- Low harmonic distortion

CIRCUIT DIAGRAM



APPLICATIONS

High speed analog multiplexing
Time division multiplexing
Series/shunt chopping
2-quadrant differential switch
Double pole double throw switch
Digital switching

MAXIMUM RATINGS

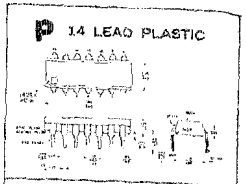
(T_A = 25°C unless otherwise specified — body grounded)

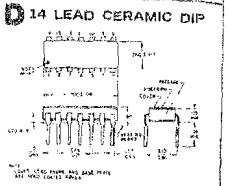
Drain to Source Voltage	35V
Gate to Source Voltage	−35V
Gate to Drain Voltage	−35V
Drain Current	−50 mA
Gate Current (forward direction for zener clamp)	+0.1 mA
Storage Temperature	−65 to 150°C
Operating Junction Temperature (851P)	−65 to 85°C
Operating Junction Temperature (851 D/F)	−65 to 125°C
Total dissipation at 25°C Ambient Temperature	600 mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	150 mW

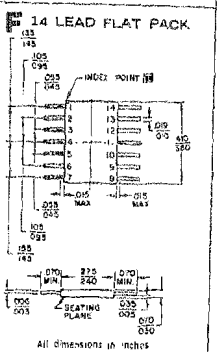
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(off)}$	Gate Source Cutoff Voltage	−1.0	—	−4.0	Volts	V_{DS} = −10V, I_D = −10 μA, V_{DS} = 0V
I_{DSS}	Drain Leakage Current	—	—	−0.3	nA	V_{DS} = −20V, $V_{GS(off)}$ = 0V
I_{GSS}	Source Leakage Current	—	—	−2.0	nA	V_{SD} = −20V, $V_{GS(off)}$ = 0
I_{GSS}	Gate Leakage Current	—	−0.1	−1.0	nA	V_{GS} = −20V, V_{DS} = 0V
$I_{D(on)}$	Drain Current	−5.0	—	—	mA	V_{DS} = V_{GS} = −10V, V_{SS} = 0V
BV_{DSS}	Drain—Source Breakdown	−35	—	—	Volts	I_D = −10 μA, V_{GSS} = 0V
BV_{DSS}	Source—Drain Breakdown	−35	—	—	Volts	I_S = −10 μA, V_{GSS} = 0V
BV_{GSS}	Gate—Source Breakdown	−35	—	−80	Volts	I_G = −10 μA V_{DSS} = 0V
Y_{fs}	Transadmittance	—	1500	—	μmho	1 KHz, V_{DS} = −10V I_D = −5 ma
C_{rss}	Gate To Source Capacitance	—	—	3.0	pF	1 MHz, V_{DS} = V_{SS} = −10V
C_{rss}	Gate To Drain Capacitance	—	—	3.0	pF	1 MHz, V_{DS} = V_{GS} = −10V
C_{ds}	Drain To Source Capacitance	—	0.04	0.10	pF	1 MHz V_{DS} = V_{SS} = −10V
$r_{ds(on)}$	Drain To Source On Resistance	—	—	100	Ohms	V_{GS} = −20V, I_D = −100μA, V_{SS} = 0V
$V_{DS(on)}$	Drain-Source "ON" Voltage	—	—	0.4	Volts	V_{GS} = −10V, I_D = −2mA
t_r	Rise Time	—	—	25	ns	V_{DD} − V_{GS} = −15V
t_f	Fall Time	—	—	130	ns	R_D = R_G = 1.5KΩ





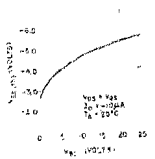


TERMINALS

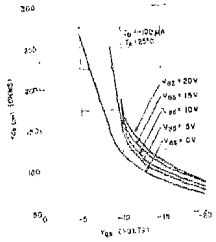
P/N	FUNCTION	P/N	FUNCTION
1	Substrate	8	Substrate
2	Drain 3	9	Drain 1
3	Gate 3	10	Gate 1
4	Source 3	11	Source 1
5	Source 4	12	Source 2
6	Gate 4	13	Gate 2
7	Drain 4	14	Drain 2

TYPICAL CHARACTERISTIC CURVES

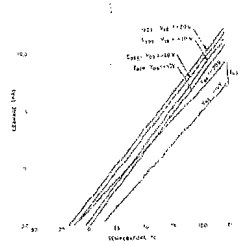
$V_{GS(off)}$ vs. V_{SS}



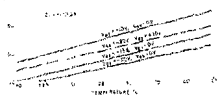
$r_{ds(on)}$ vs. V_{DS}
V_{SS} parameter



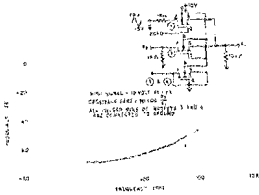
LEAKAGE vs. TEMPERATURE



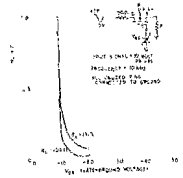
$r_{ds(on)}$ vs. TEMPERATURE
V_{GS}, V_{SS} parameter



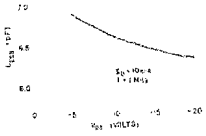
CROSSTALK (dB) vs. FREQUENCY



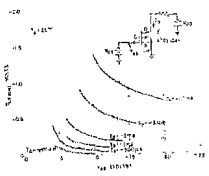
HARMONIC DISTORTION vs. V_{DS}
R_L parameter



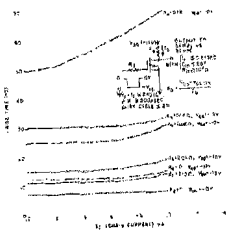
INPUT CAPACITANCE vs. V_{DS}



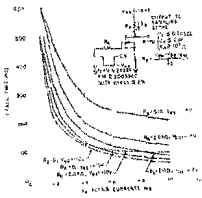
$V_{DS(on)}$ vs. V_{GS}
I_D parameter



RISE TIME vs. DRAIN CURRENT
R_G, V_{DD} parameter



FALL TIME vs. DRAIN CURRENT
R_G, V_{DD} parameter



8B

Six Channel MOSFET Analog Gate

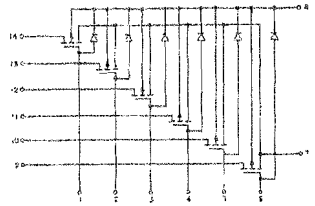
FEATURES

- Low input capacitance
- 40 volt peak-peak signal input range
- 10^{10} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- High Drain, Source and Gate Breakdown Voltages
- Low harmonic distortion

APPLICATIONS

- Analog Multiplexing
- Time division multiplexing
- Chopping
- Serial to parallel & parallel to serial converter

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C, unless otherwise specified — body grounded)

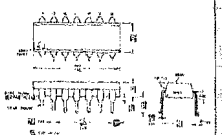
Drain to Source Voltage	−80V
Gate to Source Voltage	−80V
Gate to Drain Voltage	−80V
Drain Current	−20mA
Gate Current (forward direction for zener clamp)	+0.1mA
Storage Temperature	−65 to 150°C
Operating Junction Temperature (856P)	−65 to 85°C
Operating Junction Temperature (856 D/F)	−65 to 125°C
Total dissipation at 25°C Ambient Temperature	300mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	50mW

ELECTRICAL CHARACTERISTICS

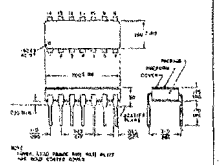
(T_A = 25°C, unless otherwise specified — body grounded)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−3.0	—	−6.0	Volts	V_{DS} = V_{DS}, I_D = −10 μA, V_{BS} = 0V
I_{DS^*}	Drain Leakage Current	—	−.05	−0.5	nA	V_{DS} = −20V, V_{GBS} = 0
I_{DS}	Source Leakage Current (Total for all Units)	—	−0.2	−2.0	nA	V_{DS} = −20V, V_{DBS} = 0
I_{GSS}	Gate Leakage Current	—	−0.1	−0.5	nA	V_{GS} = −20V, V_{DBS} = 0
$I_{D(ON)}$	Drain Current	−1.0	−3.0	—	mA	V_{DS} = V_{DS} = −10V, V_{BS} = 0V
BV_{DSS}	Drain—Source Breakdown	−50	−65	−80	Volts	I_D = −10 μA, V_{GBS} = 0V
BV_{SDS}	Source—Drain Breakdown	−50	−60	−80	Volts	I_S = −10 μA, V_{GBS} = 0V
BV_{GSS}	Gate—Source Breakdown	−50	−70	−80	Volts	I_G = −10 μA, V_{DS} = 0V
Y_m	Transadmittance	—	700	—	μmho	1 kHz, V_{DS} = −20V, I_D = −5mA, V_{BS} = 0V
C_{gs}	Gate To Source Capacitance	—	0.2	0.5	pF	1 MHz, V_{GS} = V_{DS} = −10V
C_{gd}	Gate To Drain Capacitance	—	0.2	0.5	pF	1 MHz, V_{GS} = V_{DS} = −10V
C_{ds}	Drain To Source Capacitance	—	0.04	0.10	pF	1 MHz, V_{GS} = V_{DS} = −10V
$r_{DS(on)}$	Drain To Source On Resistance	—	700	1000	Ohms	V_{GS} = −20V, I_D = −100 μA, V_{BS} = 0V

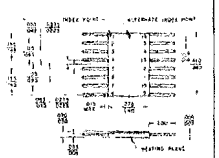
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



F 14 LEAD FLAT PACK



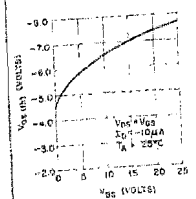
All dimensions in inches

TERMINALS

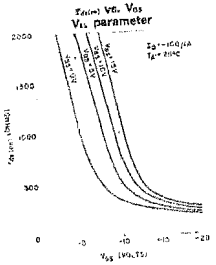
P/N	FUNCTION	P/N	FUNCTION
1	Gate 1	8	Substrate
2	Gate 2	9	Drain 6
3	Gate 3	10	Drain 5
4	Gate 4	11	Drain 4
5	Gate 5	12	Drain 3
6	Gate 6	13	Drain 2
7	Source	14	Drain 1

TYPICAL CHARACTERISTIC CURVES

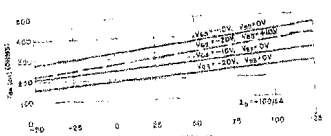
$V_{GS(th)}$ vs. V_{BS}



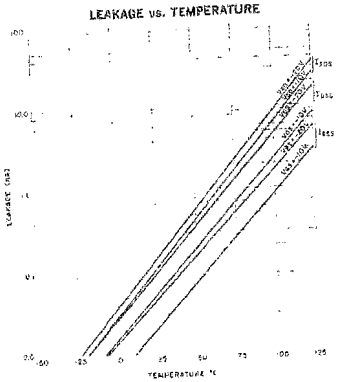
$r_{DS(on)}$ vs. V_{DS} V_{GS} parameter



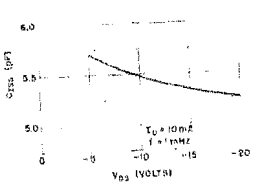
$r_{DS(on)}$ vs. TEMPERATURE V_{GS}, V_{BS} parameter



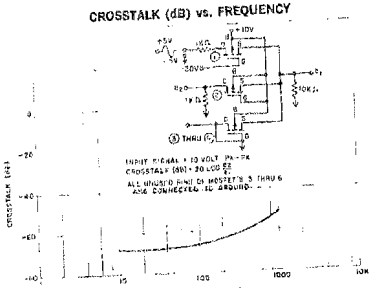
LEAKAGE vs. TEMPERATURE



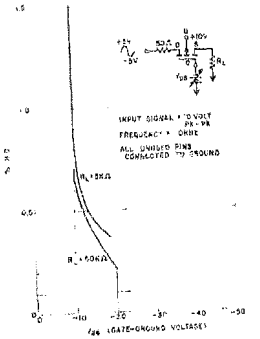
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GG} R_L parameter



Six Channel MOSFET Analog Gate

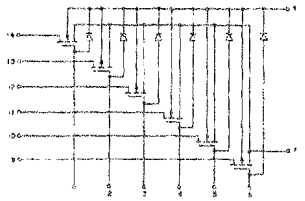
FEATURES

- 25 volt peak-peak signal input range
- 10^{12} ohms input resistance to gate
- Integrated zener clamp protects the gate
- Normally off with zero gate voltage
- Square Law linear transfer characteristics
- Low crosstalk
- Low leakage presented to the summing junction
- Low "on" Resistance
- Low harmonic distortion

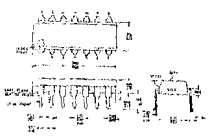
APPLICATIONS

- Analog Multiplexing
- Time division multiplexing
- Chopping
- Serial to parallel & parallel to serial converter

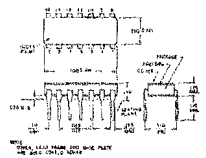
CIRCUIT DIAGRAM



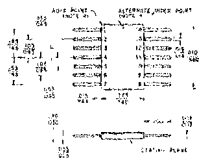
P 14 LEAD PLASTIC



D 14 LEAD CERAMIC DIP



F 14 LEAD FLAT PACK



all dimensions in inches

TERMINALS

P/N	FUNCTION	P/N	FUNCTION
1	Gate 1	8	Substrate
2	Gate 2	9	Drain 6
3	Gate 3	10	Drain 5
4	Gate 4	11	Drain 4
5	Gate 5	12	Drain 3
6	Gate 6	13	Drain 2
7	Source	14	Drain 1

MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

Drain to Source Voltage	−35V
Gate to Source Voltage	−40V
Gate to Drain Voltage	−40V
Drain Current	−50 mA
Gate Current (forward direction for zener clamp)	+0.1 mA
Storage Temperature	−65 to 150°C
Operating Junction Temperature (856P)	−65 to 85°C
Operating Junction Temperature (856 D/F)	−65 to 125°C
Total dissipation at 25°C Ambient Temperature	900 mW
Total dissipation at 25°C Ambient Temperature for each gate circuit	150 mW

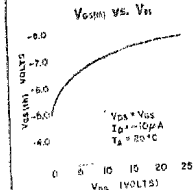
ELECTRICAL CHARACTERISTICS

(T_A = 25°C, unless otherwise specified — body grounded)

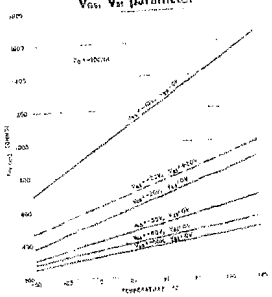
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate Source Cutoff Voltage	−1.5	—	−5.0	Volts	V_{DS} = V_{DS}, I_D = −10 μA, V_{DS} = 0V
I_{DSS}	Drain Leakage Current	—	−.10	−3.0	nA	V_{DS} = −20V V_{GSS} = 0
I_{SDO}	Source Leakage Current (Total for all Units)	—	−0.6	−12	nA	V_{SG} = −20V, V_{DSS} = 0
I_{GSS}	Gate Leakage Current	—	−0.1	−1.0	nA	V_{GS} = −20V, V_{DS} = 0
$I_{D(ON)}$	Drain Current	−3.0	−6.0	—	mA	V_{DS} = V_{SS} = −10V, V_{GS} = 0V
BV_{DSS}	Drain—Source Breakdown	−35	—	—	Volts	I_D = −10 μA, V_{GSS} = 0V
BV_{SDO}	Source—Drain Breakdown	−35	—	—	Volts	I_S = −10 μA, V_{GD} = 0V
BV_{GSS}	Gate—Source Breakdown	−40	—	−80	Volts	I_G = −10 μA, V_{DS} = 0V
Y_{fs}	Transadmittance	—	2500	—	μmho	1 kHz, V_{DS} = V_{SS} = −10V
C_{gs}	Gate To Source Capacitance	—	3.0	6.0	pF	1 MHz, V_{DS} = V_{SS} = −10V
C_{gd}	Gate To Drain Capacitance	—	1.9	3.5	pF	1 MHz, V_{DS} = V_{SS} = −10V
C_{ds}	Drain To Source Capacitance	—	0.04	0.1C	pF	1 MHz, V_{DS} = V_{SS} = −10V
$r_{DS(on)}$	Drain To Source On Resistance	—	150	350	Ohms	V_{GS} = −20V I_D = −100 μA V_{DS} = 0V

TYPICAL CHARACTERISTIC CURVES

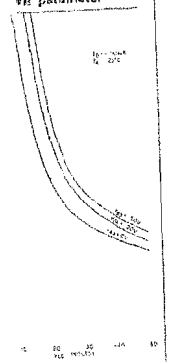
$V_{GS(th)}$ vs. V_{DS}



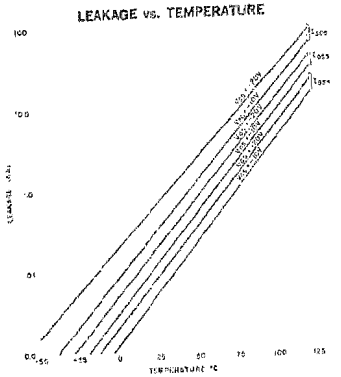
$r_{DS(on)}$ vs. TEMPERATURE
V_{GSS} V_{DS} parameter



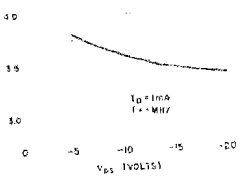
$r_{DS(on)}$ vs. V_{DS}
V_{GS} parameter



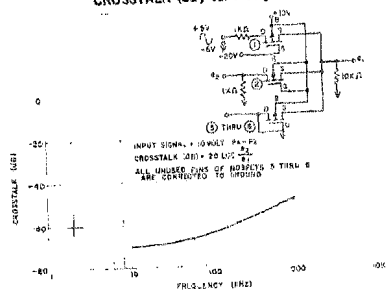
LEAKAGE vs. TEMPERATURE



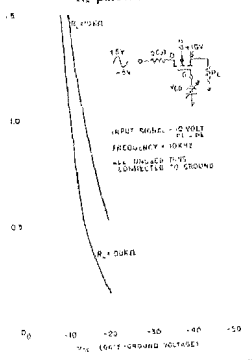
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{DS}
R_L parameter



Eight Channel MOSFET Analog Gate

FEATURES

- 25 Volt Peak-Peak Signal Input Range
- Low Threshold
- 10^{12} Ohms Input Resistance
- Integrated Zener Clamp Protection
- Normally Off with Zero Gate Voltage
- Square Law Linear Transfer Characteristics
- Low Crosstalk
- Low Leakage Presented to the Summing Junction
- Low "ON" Resistance
- Low Harmonic Distortion
- Less Than a 20 Ohm Change of "ON" Resistance from Channel to Channel

APPLICATIONS

Analog Multiplexing
Time Division Multiplexing
Chopper
Serial to Parallel & Parallel to Serial Converter
4-channel Differential Switch

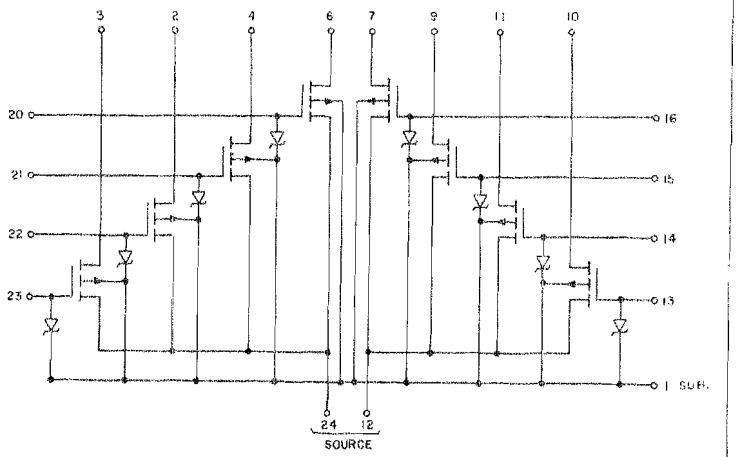
DESCRIPTION

This multiple switch contains 8 nitride passivated insulated gate field effect transistors. The sources are connected in such a way as to afford maximum flexibility for switching applications.

By properly biasing the devices, they can be used either as multiple switches, rotary switches, "AND" gates or "NOR" gates.

The nitride passivation process enables this device to have a low threshold voltage capability

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

Drain to Source Voltage	−30V
Gate to Source Voltage	−30V
Gate to Drain Voltage	−30V
Drain Current	50mA
Gate Current (forward direction for zener clamp)	+0.1mA
Storage Temperature	−65°C to 150°C
Operating Junction Temperature (857P)	−65°C to 85°C
Operating Junction Temperature (857 D/F)	−65°C to 125°C
Total Dissipation at 25°C Ambient Temperature	1.75W
Total Dissipation at 25°C Ambient Temperature for each gate circuit	175mW

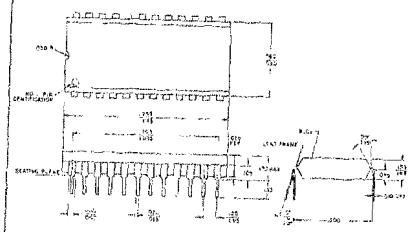
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise specified — body grounded)

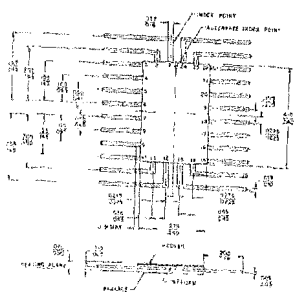
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate-Source Cutoff Voltage	1.5	—	4.5	Volts	V_{DS} = V_{GS}, I_D = −10μA, V_{BS} = 0V
I_{DSS}	Drain Leakage Current	—	—	5	nA	V_{DS} = −20V, V_{GSB} = 0
$I_{S(on)}$ S1-4 / S5-8	Source Leakage Current	—	—	20 / 20	nA	V_{SD} = −20V, V_{GDS} = 0
I_{GSS}	Gate Leakage Current	—	—	1	nA	V_{GS} = −20V, V_{DSB} = 0
$I_{D(on)}$	Drain Current	10	—	—	mA	V_{DS} = V_{GS} = −10V V_{BS} = 0
BV_{DSS}	Drain-Source Breakdown Voltage	30	—	—	Volts	I_{DS} = −10μA, V_{GSB} = 0
BV_{SDS}	Source-Drain Breakdown Voltage	30	—	—	Volts	I_{SD} = −10μA, V_{GDB} = 0
BV_{GSS}	Gate-Source Breakdown Voltage	30	—	—	Volts	I_{GS} = −10μA, V_{DSS} = 0
Y_{fs}	Transadmittance	1500	—	—	μmhos	V_{DS} = −10V, I_D = −5mA, f = 1kHz, V_{BS} = 0
C_{gs}	Gate-Source Capacitance	—	1.5	2.5	pF	V_{GS} = V_{DS} = −10V, f = 1MHz
C_{gd}	Gate-Drain Capacitance	—	1.0	2.0	pF	V_{GS} = V_{DS} = −10V, f = 1MHz
C_{ds}	Drain-Source Capacitance	—	0.04	0.10	pF	V_{GS} = V_{BS} = −10V, f = 1MHz
$r_{DS(on)}$	Drain-Source On Resistance	—	—	150	Ohms	V_{GS} = −20V, I_D = −100μA, V_{BS} = 0

8B

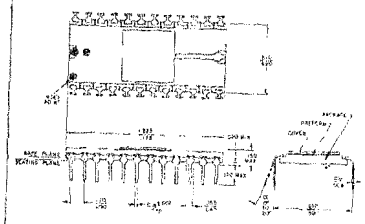
P 24 LEAD PLASTIC



F 24 LEAD FLAT PACK



D 24 LEAD CERAMIC DIP

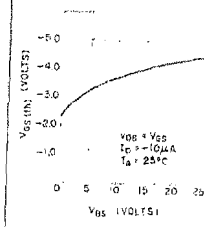


TERMINALS

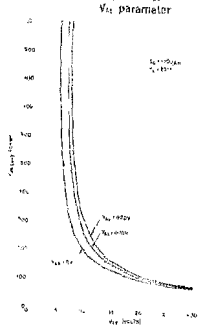
P/N	FUNCTION	P/N	FUNCTION
1	Substrate	13	Gate 10
2	Drain 2	14	Gate 9
3	Drain 1	15	Gate 8
4	Drain 3	16	Gate 7
5	Drain 4	17	Gate 6
6	Drain 5	18	Source 5-6
7	Drain 6	19	Gate 5
8	Drain 7	20	Gate 4
9	Drain 8	21	Gate 3
10	Drain 10	22	Gate 2
11	Drain 9	23	Gate 1
12	Source 7-10	24	Source 1-4

TYPICAL CHARACTERISTIC CURVES

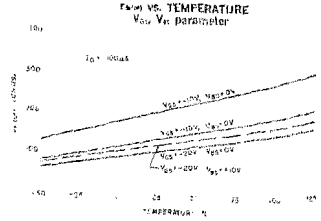
$V_{GS(th)}$ vs. V_{SS}



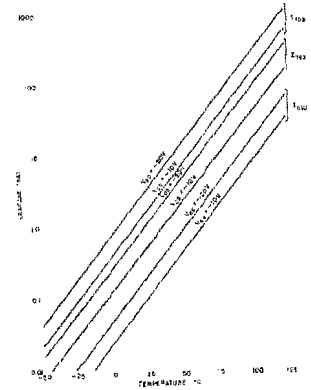
$r_{DS(on)}$ vs. V_{GS}
V_{SS} parameter



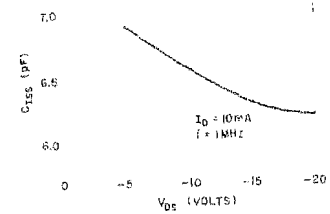
$I_{D(off)}$ vs. TEMPERATURE
V_{DS}, V_{SS} parameter



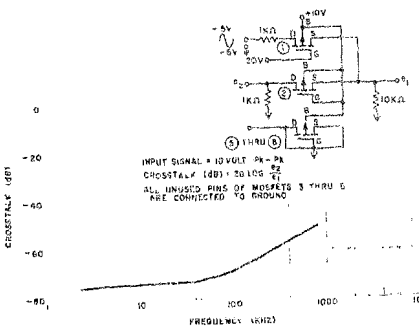
LEAKAGE vs. TEMPERATURE



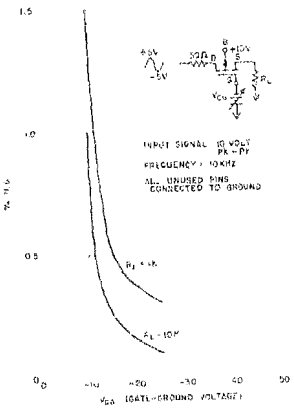
INPUT CAPACITANCE vs. V_{DS}



CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{DD}
R_L parameter



Ten Channel MOSFET Analog Gate

FEATURES

- 25 Volt Peak-Peak Signal Input Range
- Low Threshold
- 10^{12} Ohms Input Resistance
- Integrated Zener Clamp Protection
- Normally Off with Zero Gate Voltage
- Square Law Linear Transfer Characteristics
- Low Crosstalk
- Low Leakage Presented to the Summing Junction
- Low "ON" Resistance
- Low Harmonic Distortion
- Less Than a 20 Ohm Change of "ON" Resistance from Channel to Channel

APPLICATIONS

Analog Multiplexing
Time Division Multiplexing
Chopper
4-channel Differential Switch
Serial to Parallel & Parallel to Serial Converter

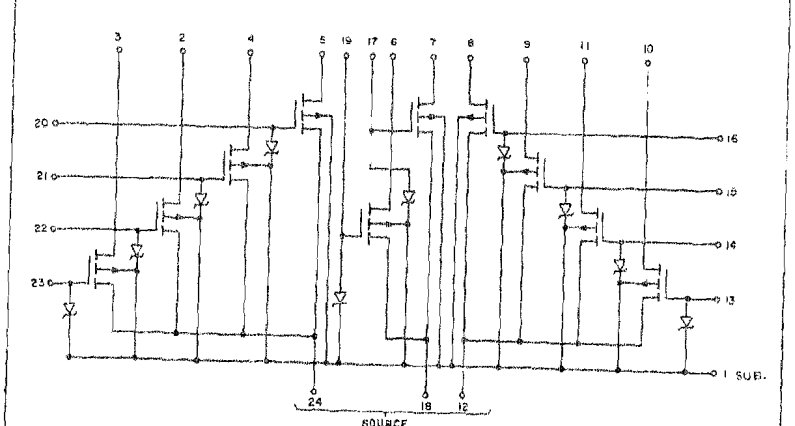
DESCRIPTION

This multiple switch contains 10 nitride passivated insulated gate field effect transistors. The sources are connected in such a way as to afford maximum flexibility for switching applications.

By properly biasing the devices, they can be used either as multiple switches, rotary switches, "AND" gates or "NOR" gates.

The nitride passivation process enables this device to have a low threshold voltage capability.

CIRCUIT DIAGRAM



MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified — body grounded)

Drain to Source Voltage	-30V
Gate to Source Voltage	-30V
Gate to Drain Voltage	-30V
Drain Current	50mA
Gate Current (forward direction for Zener clamp)	-0.1mA
Storage Temperature	-65°C to 150°C
Operating Junction Temperature (853P)	-65°C to 85°C
Operating Junction Temperature (853 D/F)	-65°C to 125°C
Total Dissipation at 25°C Ambient Temperature	1.75W
Total Dissipation at 25°C Ambient Temperature for each gate circuit	175mW

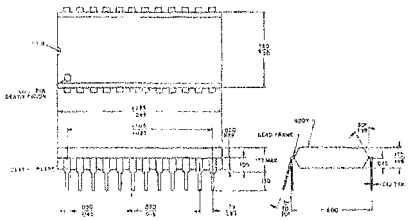
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise specified — body grounded)

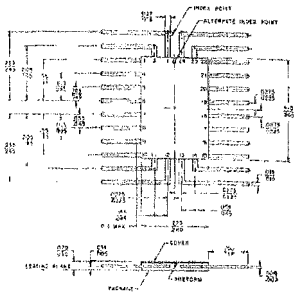
8B

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$V_{GS(th)}$	Gate-Source Cutoff Voltage	1.5	--	4.5	Volts	V_{DS} = V_{GS}, I_D = -10μA, V_{BS} = 0V
I_{DSS}	Drain Leakage Current	--	--	5	nA	V_{DS} = -20V, V_{GSS} = 0
I_{DS} S1-4	Source Leakage Current	--	--	20	nA	V_{SD} = -20V, V_{GDS} = 0
I_{DS} S5-6		--	--	10	nA	
I_{DS} S7-10		--	--	20	nA	
I_{GSS}	Gate Leakage Current	--	--	1.0	nA	V_{GS} = -20V, V_{DSS} = 0
$I_{D(on)}$	Drain Current	10	--	--	mA	V_{DS} = V_{GS} = -10V, V_{BS} = 0
BV_{DSS}	Drain-Source Breakdown Voltage	30	--	--	Volts	I_{DS} = -10μA, V_{BSS} = 0
BV_{SDS}	Source-Drain Breakdown Voltage	30	--	--	Volts	I_{SD} = -10μA, V_{GDS} = 0
BV_{GSS}	Gate-Source Breakdown Voltage	30	--	--	Volts	I_{GS} = -10μA, V_{DSS} = 0
Y_{fs}	Transadmittance	1500	--	--	μmhos	V_{DS} = -10V, I_D = -5mA, f = 1kHz, V_{BS} = 0
C_{gs}	Gate-Source Capacitance	--	1.5	2.5	pF	V_G = V_{DS} = -10V, f = 1MHz
C_{gd}	Gate-Drain Capacitance	--	1.0	2.0	pF	V_{GS} = V_{DS} = -10V, f = 1MHz
C_{ds}	Drain-Source Capacitance	--	0.04	0.10	pF	V_{GS} = V_{DS} = -10V, f = 1MHz
$r_{DS(on)}$	Drain-Source On Resistance	--	--	150	Ohms	V_{GS} = -20V, I_D = -100μA, V_{BS} = 0

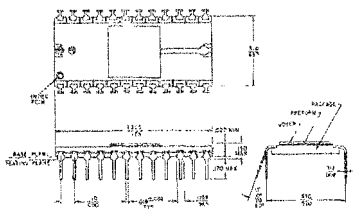
P 24 LEAD PLASTIC



F 24 LEAD FLAT PACK



D 24 LEAD CERAMIC DIP

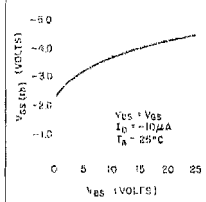


TERMINALS

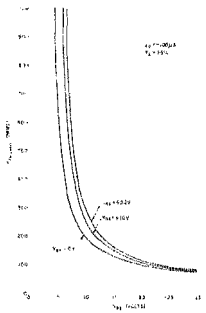
P/N	FUNCTION	P/N	FUNCTION
1	Substrate	13	Gate 8
2	Drain 2	14	Gate 7
3	Drain 1	15	Gate 6
4	Drain 3	16	Gate 5
5	N.C.	17	N.C.
6	Drain 4	18	N.C.
7	Drain 5	19	N.C.
8	N.C.	20	Gate 4
9	Drain 6	21	Gate 3
10	Drain 8	22	Gate 2
11	Drain 7	23	Gate 1
12	Source 5-8	24	Source 1-4

TYPICAL CHARACTERISTIC CURVES

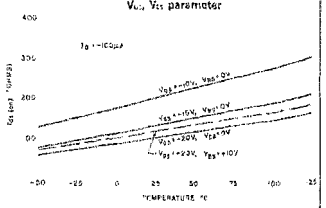
$V_{GS(th)}$ vs. V_{BS}



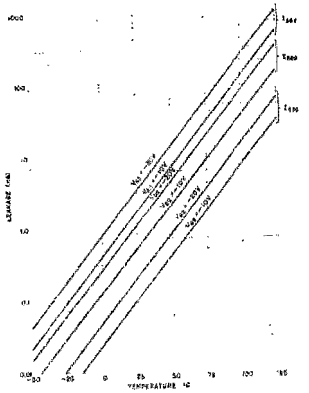
$r_{DS(on)}$ vs. V_{BS}
V_{GS} parameter



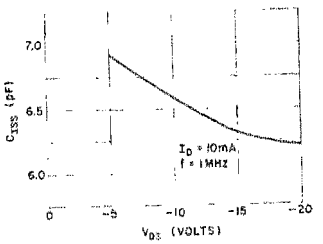
$r_{DS(on)}$ vs. TEMPERATURE
V_{GS}, V_{BS} parameter



LEAKAGE vs. TEMPERATURE

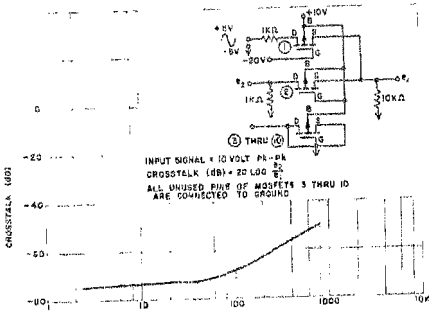


INPUT CAPACITANCE vs. V_{DS}

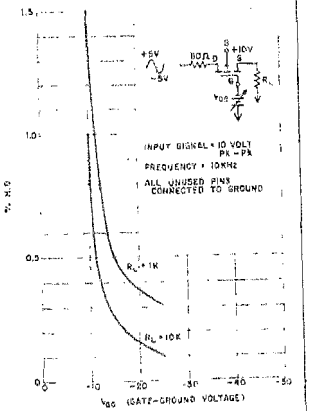


8B

CROSSTALK (dB) vs. FREQUENCY



HARMONIC DISTORTION vs. V_{GS}
R_L parameter



INDUSTRIAL

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
4 DIGIT COUNTER	Counts stores & decodes four decades to BCD outputs	AY-5-4057	9-3
4 DIGIT COUNTER/ DISPLAY DRIVER	Counts (up or down), stores & decodes four decades to 7-segment outputs	AY-5-4007	9-6
		AY-5-4007A	9-6
		AY-5-4007D	9-6
3½ DIGIT DVM	DVM logic incorporating dual ramp integration	AY-5-3507	9-12
		AY-5-3510	9-12
3¾ DIGIT DVM	DVM logic incorporating single ramp integration	AY-5-3500	9-17
4½ DIGIT DVM	DVM logic incorporating dual ramp integration	AY-3-3550	9-22
10 BIT D/A CONVERTER	Laddarless D/A converter	AY-5-5053	9-27
A/D CONVERTER CONTROL	With AY-5-5053 performs A/D transmitter facility	AY-5-5054	9-32
SEQUENTIAL BOOLEAN ANALYZER	A simple, single bit processor which can directly evaluate a set of Boolean equations	SBA	9-36

INDUSTRIAL

MICRO ELECTRONICS

Four Digit Counter

FEATURES

- Fully static operation.
- Maximum clock input 600kHz
- Reset input.
- Multiplexed outputs.
- Final Carry output and two intermediate carry outputs.
- TTL/DTL compatible inputs and outputs

DESCRIPTION

The AY-5-4057 is a fully static four digit counter capable of accepting a count frequency of up to 600kHz. The four counters are connected in series, each having a 4-bit store associated with it. The counters change on the negative going clock transition, and the counter outputs are transferred to the 4-bit stores when the load control is taken to Logic '0'.

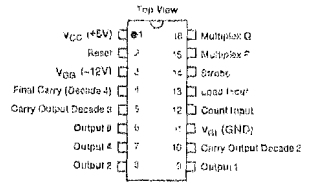
The count held in the four stores is strobed out in sequence by a signal derived from the 'Strobe Input'. The multiplexed BCD outputs are output in sequence and are capable of driving a decoder/driver. The 'Strobe Input' operates on a positive transition (0 to 1), and the multiplex outputs, P and Q are in a 2-bit binary sequence.

In addition to the count outputs, the device has a 'Final Carry Output' (CO 4) and two intermediate carry outputs, CO2 and CO3, from the second and third decades respectively.

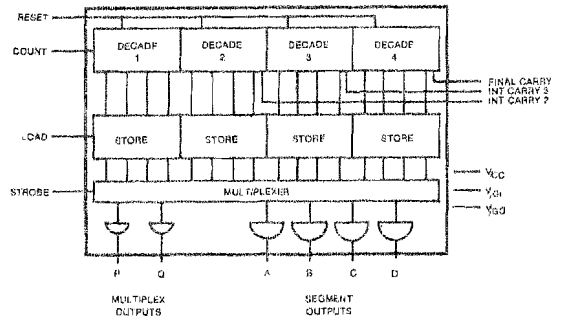
A reset line is provided to reset all four decades to the zero state.

PIN CONFIGURATION

16 LEAD DUAL IN LINE



BLOCK DIAGRAM



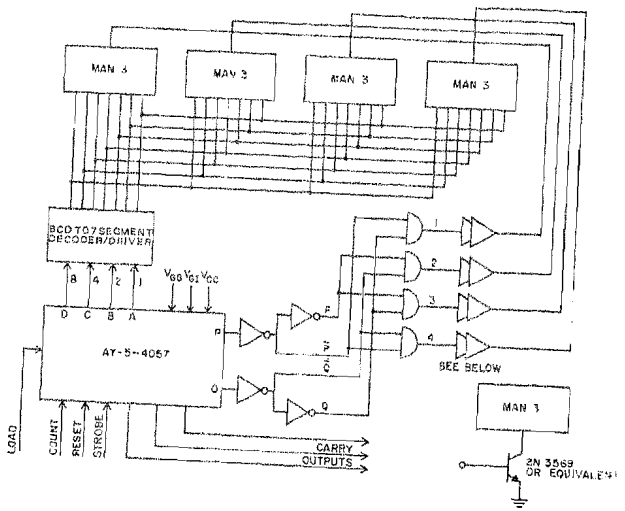
9

PIN FUNCTIONS

Name	Functions
COUNT INPUT	A negative going (1 to 0) signal on this input causes the counter to be incremented by one.
LOAD INPUT	A logic '0' level on this input causes the contents of the four counters to be transferred to the store. To store any one count, the load input must go to logic '0' a minimum of 800 nsec after the count pulse that sets up the count to be stored, (ts1 on timing diagram) and stay at logic '0' for a minimum of 1 μsec.
RESET	A logic '1' level applied to this input will reset all four counters to the all '0's state (Store is *not* reset). A delay of 250 nsec must be allowed (ts2 of timing/diagram) after the reset goes to logic '0' before a count is started.
STROBE	A positive going ('0' to '1') signal on this input clocks the multiplex counter, thereby causing the count to be output in the correct sequence.
P & Q OUTPUTS	The two Multiplex outputs P and Q, identify which decade is being output P Q 1 0 Strobes decade 1 0 1 Strobes decade 2 1 1 Strobes decade 3 0 0 Strobes decade 4
*INTERMEDIATE CARRY (CO2)	This output is generated by the second decade of the counter
*INTERMEDIATE CARRY (CO3)	This output is generated by the third decade of the counter
*FINAL CARRY	This output is generated by the fourth decade of the counter

*All carry outputs go to logic '1' on count 9 and return to logic '0' on count 10.

COUNTER-DISPLAY INTERFACE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Max. voltage between V_{CC} and any pin.	−20V to 0.3V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

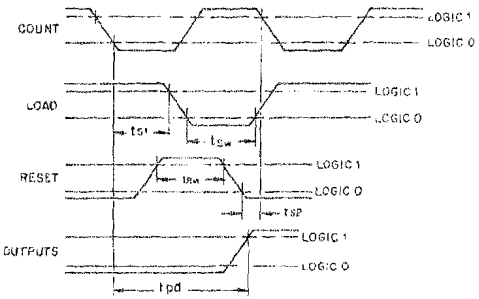
*Exceeding these ratings could cause *permanent damage*. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{BB} = −12V ±1V
V_{CC} = +5.0 ±0.5V
V_{IN} = 0V
Operating Temperature (T_A) = 0°C to +70°C
Output Loading = 1 TTL Load
CL TOTAL = 10 pF

Characteristic	Min	Max	Units	Conditions
Count Input				
Repetition Rate	DC	500	kHz	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5	pF	V_{IN}=V_{CC}
Load Input				
Pulse Width t_{pw}	1.0	—	μs	
Set-up Time ts1	800	—	ns	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	V_{IN}=V_{CC}
Strobe Input				
Repetition Rate	DC	10	kHz	
Pulse Width	10	—	μs	
Rise/Fall Times	—	10	μs	
Logic '0'	—	+0.8	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	5.0	pF	V_{IN}=V_{CC}
***Reset* Input**				
Pulse width t_{pw}	1	—	μs	
Set-up-Time ts2	250	—	ns	
Logic '0'	—	+0.4	V	
Logic '1'	V_{CC}−1.5	—	V	
Input Capacitance	—	10	pF	
Outputs				
Logic '0'	—	+0.4	V	I_{OL} = 1.6mA
Logic '1'	V_{CC}−1.0	—	V	I_{OH} = 100μA
Propagation delay tpd	—	2.0	μs	
Input Leakage	—	5.0	μA	V_{IN}=V_{CC}−10V at 25°C
Power	—	350	mW	

TIMING DIAGRAM



Four Digit Counter / Display Drivers

FEATURES

- Minimum interface required to drive most common types of LED, fluorescent, seven segment displays
- Large output current capability on seven segment outputs, typically 25mA with 1V drop.
- Fully synchronous up/down counting operation.
- Look ahead carry for error free outputs when reversing count direction
- Internal oscillator needing no external components for operating the digit select counter
- Four digit select outputs with inversion control for display driving flexibility.
- Multiplexed BCD outputs and serial output from storage register is available.
- TTL/DTL compatible on inputs and outputs
- Blanking action of Reset input.
- Counting rate up to 600 KHz

DESCRIPTION

The Four Digit Counter Display Driver is an LSI subsystem designed for application in counting display systems such as frequency counters, digital voltmeters, digital timers, event counters using 7 segment numeric displays. It contains a 4 decade up/down synchronous BCD counter, a storage register, multiplexing circuits, internal oscillator for digit selection and 7 segment decoder to count and display up to 9999.

Built-in control circuits provide flexibility of use with a minimum of external components

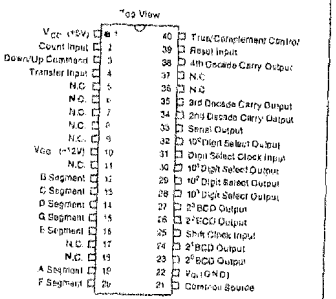
The device is constructed on a single monolithic chip using MTNS P-channel enhancement mode transistors

AY-5-4007A. Available in 40 Lead Dual In Line package, allows for all available functions.

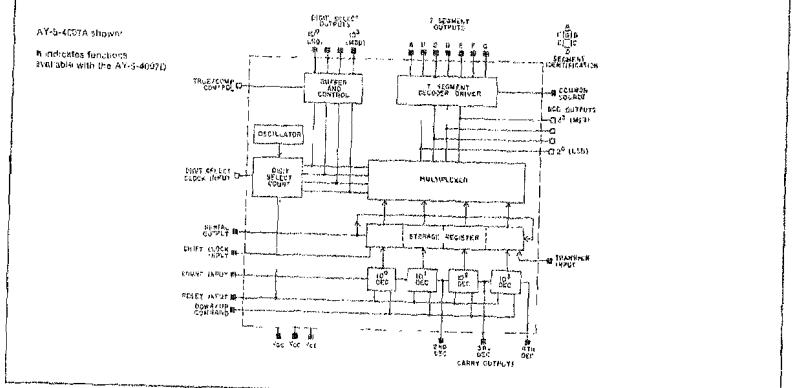
The AY-5-4007 and AY-5-4007D incorporate the most commonly used features in 24 Lead Dual In Line packages.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-4007A

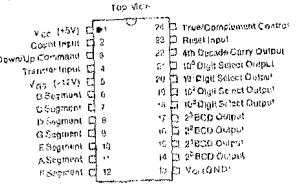


BLOCK DIAGRAM

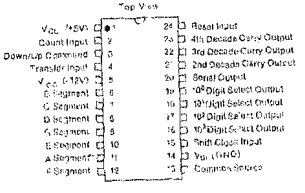


PIN CONFIGURATIONS

24 LEAD DUAL IN LINE
AY-5-4007



24 LEAD DUAL IN LINE
AY-5-4007D



NOTE For AY-5-4007D, True/Complement control is internally connected to logic "0" level

PIN FUNCTIONS

Name	Function
COUNT INPUT	Count Input operates the decade counters synchronously on the positive going edges (logic '0' to '1' transitions)
RESET INPUT	When this input goes to a logic '1' it resets the decade counters to 0000, forces the digit select counter to the MSD position and the Digit Select Outputs to 'not active' logic levels to blank the display. It must be present for a minimum of 10 μsec
DOWN/UP COMMAND	The count direction depends upon the logic level on the DOWN/UP Command input. Logic '0' = Count UP. Logic '1' = Count DOWN
2ND DECADE CARRY OUTPUT 3RD DECADE CARRY OUTPUT 4TH DECADE CARRY OUTPUT	Normally the Carry Outputs are at a logic '0' level. When activated a positive pulse is generated on the output line, which is identical with the Count Input causing the carry
TRANSFER INPUT	Placing the Transfer Input at a logic '1' allows transfer of data from the decade counters to the storage register
SHIFT CLOCK INPUT	This input is used to apply clock pulses to the storage register for serial shift operation. Normally Shift Clock is maintained at a Logic '1' and negative pulses are necessary to perform shift operation. Actual shifting of storage register data is done on the second edge (positive going) of each clock pulse. A Pull-up resistor is internally provided for the Shift Clock Input so that this line, if not used, may be left floating. Since the storage register is quasi-static in serial shift operation the width of negative pulses (at logic '0') has to be limited to 30μsec. During serial shift operation the Transfer Input must be at a 'logic 0'
SERIAL OUTPUT	This is the serial output of the storage register. When serial shift operation is not performed the Serial Output is the least significant bit of the least significant digit of the storage register
10^0 DIGIT SELECT OUTPUT (LSD) 10^1 DIGIT SELECT OUTPUT 10^2 DIGIT SELECT OUTPUT 10^3 DIGIT SELECT OUTPUT (MSD)	These outputs provide sequentially an active logic level (logic '1' if the True/Complement Control is at a logic '1', logic '0' if the True/Comlement Control is at a logic '0'), to specify which of the corresponding digits is selected and displayed, the remaining 3 Outputs being 'not active'. All the Digit Select Outputs are forced to a 'not active' logic level as long as the Reset Input is active
2^0 BCD OUTPUT(LSB) 2^1 BCD OUTPUT 2^2 BCD OUTPUT 2^3 BCD OUTPUT(MSB)	These outputs provide the Binary Coded Decimal representation of the digit being selected and displayed by the multiplexer. The truth table shows BCD Codification of these outputs
"A" TO "G" SEGMENT	These outputs are programmed according to the truth table. Each output terminal is actually connected to the drain of the corresponding output transistor.
COMMON SOURCE	This is the common of the seven segment output transistors. When not externally available the corresponding terminal is internally tied to V_{SS} (0V) line. It may be connected to any voltage between Vss and Vpp according to requirements
TRUE/COMPLEMENT CONTROL	This input controls the polarity of the Digit Select Outputs active logic level. When the TRUE/COMPLEMENT Control is at a logic '1', active level for the Digit Select Outputs is a logic '1', when at a logic '0' active level is a logic '0'
DIGIT SELECT CLOCK INPUT	An external signal applied to this terminal overrides the internal oscillator. When the internal oscillator is used, this terminal must be left floating

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC}	−20 to +0.3V
Storage temperature range	−65°C to +150°C
Ambient operating temperature range	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

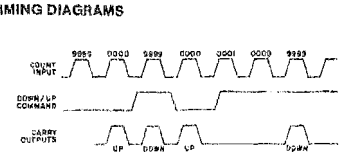
V_{CC} = +5.0 ±0.5V V_{GG} = −12V ±1V OR −7.0V ±0.5V
V_{GR} = 0V Operating Temperature (T_A) 0°C to +70°C

	V_{GG} = −12V ±1V			V_{GG} = −7V ±0.5V				
Characteristic	**Min**	**Typ****	**Max**	**Min**	**Typ****	**Max**	**Units**	**Conditions**
Inputs								
Logic '0'	V_{GG}	-	+0.8	V_{GR}	-	+0.8	Volts	See Fig. 4
Logic '1'	V_{CC} −1.5	-	V_{CC} +0.3	V_{CC} −1.5	-	V_{CC} +0.3	Volts	
Capacitance	-	-	10.0	-	-	10.0	pF	V_{IN} = V_{CC} f = 1MHz
Leakage	-	-	5.0	-	-	5.0	µA	V_{IN} − V_{CC} = −10V at 25°C
Repetition Rate	D.C	-	800	D.C	-	350	kHz	Square Wave
Pulse Width	0.7	-	-	1.0	-	-	µsec	Pulse either high or low
Tr & Tf	-	-	100			100	µsec	
True/Complement/ Control Input								
Input Current	10	40	100	10	-	50	µA	V_{IN} = V_{CC}
	10	25	50	10	-	25	µA	V_{IN} = V_{GR} See Fig. 5
Digit Select Clock								
Input Current	10	60	150	5	25	75	µA	V_{IN} = V_{CC} (Sink)
	50	250	1600	50	150	1000	µA	V_{IN} = V_{GI} (Source) See Fig. 3
Internal Freq.	1.0	2.0	4.0	1.0	2.0	4.0	kHz	
External Freq.—Data only	D.C.	-	100	D.C	-	50	kHz	
Display	D.C	-	15	D.C.	-	7	kHz	Display Duty Cycle 25%
Shift Clock								
Frequency	D.C	-	1	D.C	-	0.8	MHz	
Pulse Width	0.4	-	1000	0.5	-	1000	µsec	See functional description
Input Current	20	100	400	10	30	200	µA	V_{IN} = V_{GI} (See Fig. 6)
Outputs—7 Segment (See Note 2)								
Leakage Current	-	-	10	-	-	10	µA	V_{OUT} − V_{CC} = −10V at 25°C
Device on Current	15	25	45	12	20	35	mA	V_{CS} − V_{OUT} = +1.0V at 25°C, V_{CS} = V_{CC}
Device on Current	12	18	27	7	11	17	mA	V_{CC} − V_{OUT} = −1.0V at 25°C. V_{CS} = V_{GI}
Power Dissipation (per segment at 25°C)	-	-	200	-	-	200	mW	See Note 1 & Fig. 1
Other Outputs								
Logic '0'	-	0.2	0.4	-	0.3	0.4	Volts	I_{OL} = 1.6mA with 10pF load
Logic '1'	V_{GI} −1.0	V_{CC} −0.65	-	V_{CC} −1.0	V_{CC} −0.65	-	Volts	I_{OH} = 50µA
Propagation Delay	-	-	1.0	-	-	1.5	µsec	Carry Output } See Fig. 2
			1.5	-	-	2.0	µsec	Serial Output }
Tr, Tf								
Rise, Fall Times	-	0.15	0.3	-	0.3	0.6	µsec	
Power								
I_{GG}	-	25	35	-	13	20	mA	(V_{CC} to V_{GG})

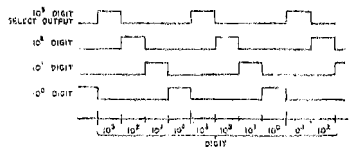
**Typical values are at +25°C and nominal voltages.

NOTES
1. Derate Power Linearly to 100mW at 70°C
2. See also Typical 7-Segment Output Curves, Figs.9, 11, & 13 (−12V ±1V)
   See also Typical 7-Segment Output Curves, Figs.10, 12 & 14 (−7V ±0.5V)

TIMING DIAGRAMS



CARRY OPERATION



DIGIT SELECT OPERATION
(True/Complement Control is at logic "1" level)

OPERATION

Decade Counters

The four decade counters are synchronously operated on the positive going edges of the Count Input. A single DOWN/UP Command controls the direction of counting. The edge-triggered structure of the master-slave flip-flops allows the count direction to be changed between count pulses at either Count input level. A Reset input resets decade counters to 0000.

Carry outputs are provided at the 2nd, 3rd and 4th decade; these outputs are activated when an overflow (in counting up) or an underflow (in counting down) condition exists in the corresponding decade counter. The carry output pulse is the same as the Count input pulse causing the carry.

The look ahead design of the carry stages gives error free outputs when reversing the count direction.

Storage Register

Data in the decade counters is transferred to the storage register under control of the Transfer Input signal. The Transfer Input may be connected to a logic "1" for a continuous transfer and display operation.

The Storage register may also be operated as a parallel-in serial-out shift register. In this case clock pulses are to be provided to Shift Clock Input, the serial content of storage register is available on the Serial Output line, and recirculated back to the first stage input. A train of 16 clock pulses is needed to extract the full content of the register least significant bit of least significant digit first. When operating the storage register serially, Transfer Input is to be kept at a logic '0'.

Digit Select Counter and Multiplexer

The digit select counter is driven by a built in oscillator which requires no external components. The internal oscillator can be overridden by applying an external signal to the Digit Select Clock Input.

The digit select counter controls the multiplexer to route information from storage register to the 7 segment decoder drivers and to the BCD Outputs.

The counter scans from MSD (10³ digit) to LSD (10⁰ digit). Each of the four Digit Select Outputs is sequentially activated when the corresponding digit is selected and displayed.

The Digit Select counter is forced to MSD position and Digit Select Outputs are forced to 'not active' logic levels as long as Reset Input is active. This feature blanks the display when the device is being reset. The True/Complement Control inverts the Digit Select Outputs active logic level for flexibility of output interface circuitry.

Internal delay logic ensures that both 7 segment outputs and BCD outputs are valid before activation of the corresponding Digit Select Output to avoid "ghost images".

7 Segment Decoder Driver

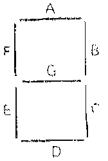
The 7 segment decoder drivers consist of very low impedance output transistors (typically 40 ohms) to minimize external interface components when driving 7 segment displays such as LEDs, fluorescents, incandescents, etc.

The 7 Segment Outputs are the drains of the corresponding output transistors, these outputs are programmed according to the truth table below. A Common Source terminal is also available to increase flexibility of use.

DIGIT	7 SEGMENT OUTPUT TRANSISTOR							BCD OUTPUT			
	A	B	C	D	E	F	G	MSB 2^3	2^2	2^1	LSB 2^0
0	*	*	*	*	*	*	–	0	0	0	0
1	–	*	*	–	–	–	–	0	0	0	1
2	*	*	–	*	*	–	*	0	0	1	0
3	*	*	*	*	–	–	*	0	0	1	1
4	–	*	*	–	–	*	*	0	1	0	0
5	*	–	*	*	*	*	*	0	1	0	1
6	*	–	*	*	*	*	*	0	1	1	0
7	*	*	*	–	–	–	–	0	1	1	1
8	*	*	*	*	*	*	*	1	0	0	0
9	*	*	*	*	–	*	*	1	0	0	1

LEGEND
* output transistor ON
– output transistor OFF
0 logic '0'
1 logic '1'

SEGMENT IDENTIFICATION



7 SEGMENT AND BCD OUTPUTS TRUTH TABLE

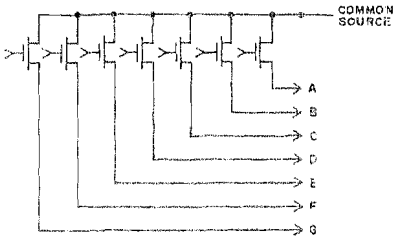


Fig.1 7-SEGMENT OUTPUTS

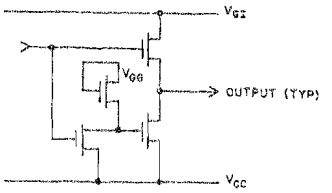


Fig.2 ALL OTHER OUTPUTS

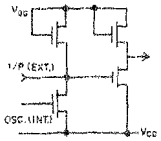


Fig.3 DIGIT SELECT CLOCK INPUT

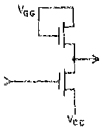


Fig.4 TYPICAL INPUT

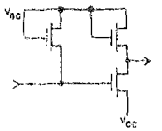


Fig.5 TRUE/COMPLEMENT INPUT

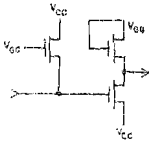


Fig.6 SHIFT CLOCK INPUT

CIRCUIT DIAGRAMS

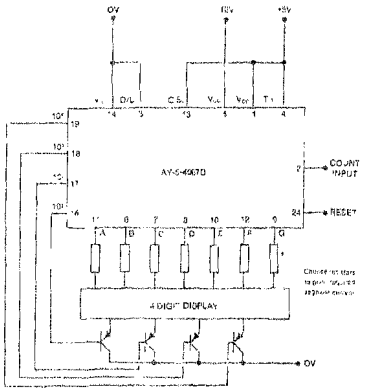


Fig.7 COMMON CATHODE LED DISPLAY

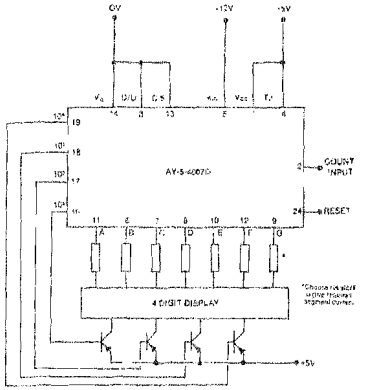
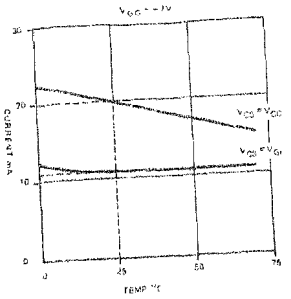


Fig.8 COMMON ANODE LED DISPLAY

TYPICAL CHARACTERISTIC CURVES



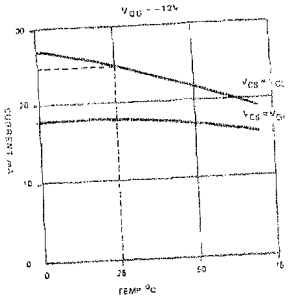


Fig.9 Fig.10

TYPICAL CURVES OF SEGMENT CURRENT VS. TEMPERATURE AT 1V ACROSS OUTPUT DEVICE

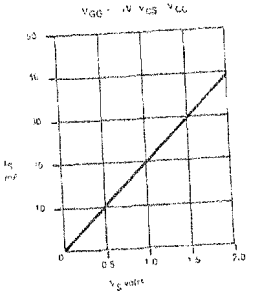


Fig.11

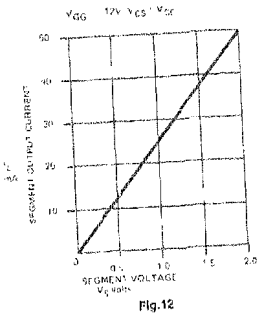


Fig.12

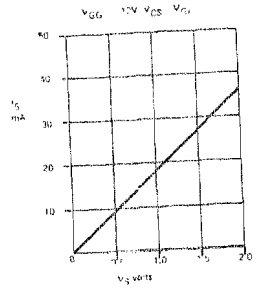


Fig.13

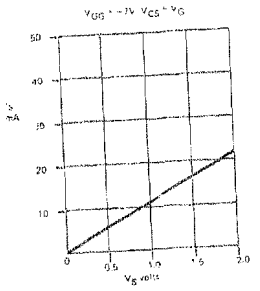


Fig.14

TYPICAL SEGMENT OUTPUT CURRENT V- OUTPUT VOLTAGE AT +25°C

9

3½ Digit DVM

FEATURES

- 3½ Decade Display (±1999 max. reading)
- Automatic Polarity Detection
- Overrange Indication

AY-5-3507

- Direct LED 7-Segment Drive
- Up to 5 readings per second

AY-3-3510

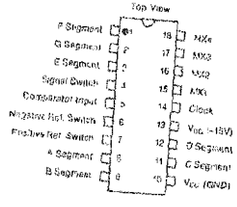
- BCD Outputs
- Up to 50 readings per second
- Chopper Output provided for oscillator synchronization or underrange indication

DESCRIPTION

The AY-5-3507 and the AY-5-3510 are MOS LSI circuits containing all the logic necessary for a 3½ Decade Digital Voltmeter utilizing Dual Ramp Integration. Automatic polarity detection is incorporated as is automatic overrange indication. For the AY-5-3507, the outputs are multiplexed onto a 7-segment bus allowing easy interface to LED and similar displays. For the AY-5-3510 the outputs are multiplexed onto a BCD bus allowing easy interface to a wide variety of displays.

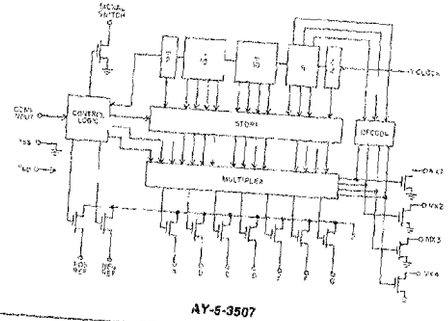
PIN CONFIGURATION

16 LEAD DUAL IN LINE
AY-5-3507

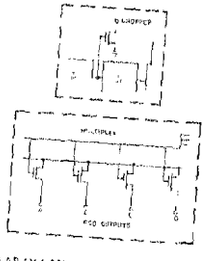


16 LEAD DUAL IN LINE
AY-5-3510

BLOCK DIAGRAM



AY-5-3507



SAME AS AY-5-3507 EXCEPT AS MARKED ABOVE.

AY-5-3510

PIN FUNCTIONS

Name	Functions
COMPARATOR INPUT	A logic '0' level corresponds to a negative input signal. A logic '1' level corresponds to a positive input signal.
CLOCK INPUT	This signal should be supplied from an external oscillator giving a square wave signal.
REFERENCE SWITCH OUTPUTS	These outputs drive analog switches which connect the Reference Voltages to the Integrator. A logic '0' at the Comparator Input will be followed by a logic '1' at the Positive Reference Switch Output. A logic '1' at the Comparator Input will be followed by a logic '1' at the Negative Reference Switch Output.
SIGNAL SWITCH OUTPUT	This output will be at logic '1' during the time that the signal is connected to the integrator.
DISPLAY MULTIPLEX OUTPUTS	Each output will be at logic '1' for 2 clock periods to display (see Fig. 1). The outputs selected will be as follows:– MX1 O/I, ±, Over-range MX3 Decade 2 (10^2) MX2 Decade 3 (10^3) MX4 Decade 1 (10^0)
AY-5-3507 SEGMENT OUTPUTS	The outputs of the 3 decade counters are presented sequentially on the outputs A, B, C, D, E, F, G. (In the first multiplex position 1 is indicated by segments B and C.–is indicated by segment G, overrange by the flashing of segments A and D. 0, ± and underrange are not indicated.
AY-5-3510 CHOPPER OUTPUT	This output is a square wave at 1/100 the clock input frequency. It can be used either to phase lock the clock oscillator to the mains or to provide a 5% FSD under-range signal.
AY-5-3510 DISPLAY OUTPUTS	The outputs of the 3 decade counters are presented on the outputs A, B C, D in BCD complement code. A=2^0, B=2^1, C=2^2, D=2^3. At MX1 time, the most significant digit is output on A with its complement on D, sign is output on B and over-range on C.

OPERATION

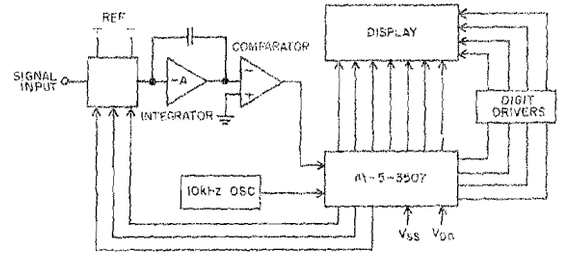
The operation of the circuit is as follows.

Initially the signal, and reference outputs are in the logic '0' state. The counter counts continuously and at the 1999 to 0000 transition a ÷ 2 is toggled driving the signal switch output to logic '1' turning on the signal switch. The integrator generates a ramp, the amplitude and polarity of which depend on the amplitude and polarity of the input signal. After a further 2000 clock pulses the ÷2 is toggled again. This stores the state of the comparator output in a D type flip flop (this signal represents the sign of the input signal). The appropriate reference switch is then energized to cause the integrator output to ramp back to zero. When the comparator output subsequently changes state the reference is switched off and the number in the counter is transferred to the store together with polarity information.

Should the input signal be so large that zero is not reached during one counter cycle, an overange flip flop will be set and will remain set until the next 1999 to 0000 transition of the counter. During overrange the main display will be set to 0000 and the overrange indicator will flash.

To minimize pin requirements, a time shared output is used. The display store output (including ±, 0/1 and overrange) is gated sequentially, a decade at a time, onto a common 7 line (AY-5-3507) or 4 line (AY-5-3510) output bus.

3½ DECADE DIGITAL VOLTMETER



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Maximum voltage between any pin and V_{SS} pin	−0.3 to −20 V
Operating temperature range	0° C to +70° C
Storage temperature range	-65° C to +150° C
Maximum power dissipation	500mW (total), 50mW (per output)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

	AY-5-3507	AY-5-3510
V_{CC}	GND	-
V_{SS}	-	GND
V_{DD}	12 to −18V	−18 to −24V
Operating Temperature (T_A)	0° C to +70° C	0° C to +70° C

Characteristic	Min	Typ**	Max	Units	Conditions
AY-5-3507					
DC CHARACTERISTICS					
Clock & Comparator Inputs					
Logic '0' Level	−5	—	−18	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Leakage	—	—	10	µA	V_{IN} = −18V, T_A = −25° C
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	1.2	2	3.2	mA	V_{OUT} = −2V, T_A = −25° C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	µA	V_{OUT} = −18V, T_A = +25° C
Switch Outputs (Note 1)					
Logic '1' sink current	0.5	0.8	1.25	mA	V_{OUT} = −2V, T_A = +25° C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	µA	V_{OUT} = −18V, T_A = +25° C
Segment Outputs (Note 1)					
Logic '1' sink current	4.25	7	11	mA	V_{OUT} = −2V, T_A = +25° C, V_{GG} = −12V
Logic '0' leakage current	—	—	10	µA	V_{OUT} = −18V, T_A = +25° C
Supply Current	—	1.5	2.2	mA	V_{DD} = −12V, T_A = +25° C
	—	3.6	5.25	mA	V_{DD} = −18V, T_A = +25° C
AC CHARACTERISTICS					
Clock & Comparator Inputs					
Input Capacitance	—	—	10	pF	V_N = 0V, f = 1MHz
Clock Frequency	DC	—	20	kHz	V_{DD} = −18V
	DC	—	10	kHz	V_{DD} = −12V
Clock Pulse Width	10	—	—	µs	Note 2
Display Multiplex Outputs					
Propagation delay	—	—	4	µs	from Clock positive edge
Segment Outputs					
Propagation delay	—	—	10	µs	from Multiplex output positive edge
AY-5-3510					
Clock & Comparator Inputs					
Logic '0' Level	−8	—	−24	Volts	
Logic '1' Level	+0.3	—	−1	Volts	
Input Capacitance	—	—	5	pf	V_{IN} = 0V
Input Leakage	—	—	10	µA	V_{IN} = −24V
Clock Frequency	DC	—	200	kHz	
Display Multiplex Outputs (Note 1)					
Logic '1' sink current	2	—	—	mA	V_{OUT} = −6V
Logic '0' leakage current	—	—	10	µA	V_{OUT} = −24V
Display & Switch Outputs (Note 1)					
Logic '1' sink current	0.7	—	—	mA	V_{OUT} = −4V
Logic '0' leakage current	—	—	10	µA	V_{OUT} = −24V
Supply Current	—	—	10.5	mA	V_{DD} = −24V

**Typical values are at +25° C and nominal voltages.

NOTE
1. All outputs are single-ended ("open-drain"). External pull-down resistors are required
2. A square waveform is preferred

TIMING DIAGRAMS

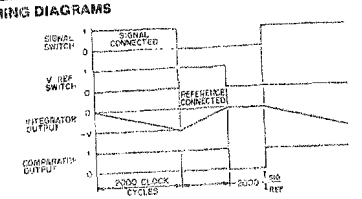


Fig.1

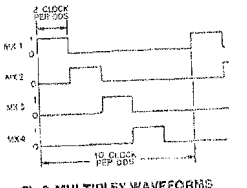


Fig.2 MULTIPLEX WAVEFORMS

TRUTH TABLES

AY-5-3507

7 SEGMENT OUTPUT TRUTH TABLE (MX2-MX4)

Digit	Segment Output A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

MX1 OUTPUT TRUTH TABLE

Display	Segment Output A	B	C	D	E	F	G
0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0
2	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0
UR	0	0	0	0	0	0	0
OR	1	0	0	1	0	0	0

Flashing

AY-5-3510

BCD OUTPUT TRUTH TABLE (MX2-MX4)

Digit	Digit Output A	B	C	D
0	1	1	1	1
1	0	1	1	0
2	1	0	1	1
3	1	1	1	0
4	0	1	1	0
5	1	0	1	1
6	1	0	1	1
7	1	1	1	0
8	1	1	1	1
9	1	1	1	0

MX1 OUTPUT TRUTH TABLE

A	B	C	D	U/D	Polarity	Overrange
1	X	X	0	0		
0	X	X	1			
X	1	X	X			
X	0	X	X			
X	X	1	X			
X	X	0	X			

OR

ANALOG CIRCUIT DIAGRAMS

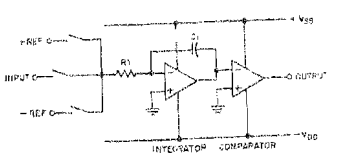


Fig.1 BASIC ANALOG CIRCUIT-AY-5-3507

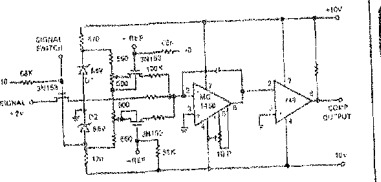


Fig.2 TYPICAL ANALOG CIRCUITRY-AY-5-3510

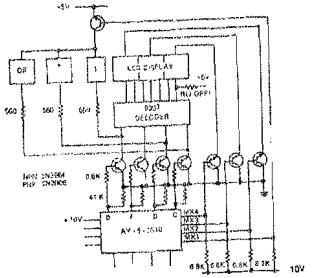


Fig.3 DISPLAY INTERFACE For AY-5-3510

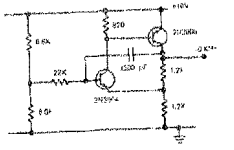
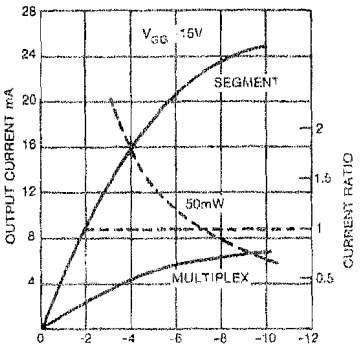
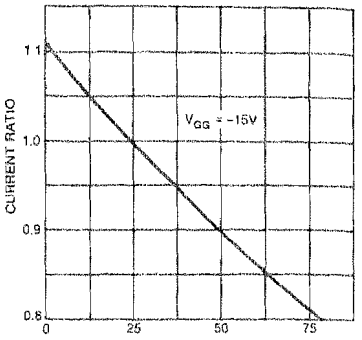


Fig.4 CLOCK OSCILLATOR-AY-5-3510

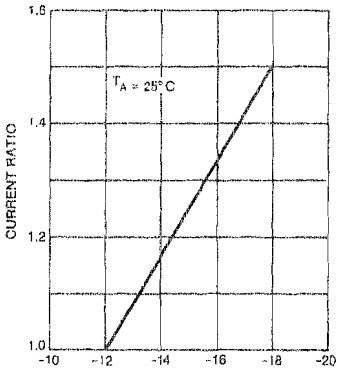
TYPICAL CHARACTERISTIC CURVES



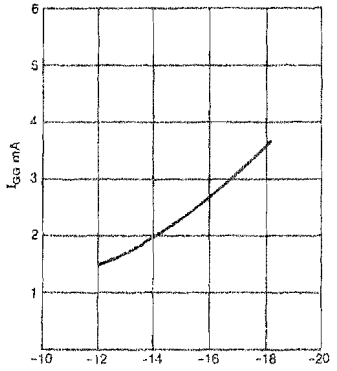
OUTPUT CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT CURRENT vs TEMPERATURE



NORMALIZED OUTPUT CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

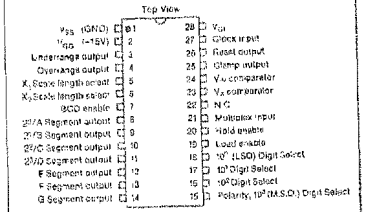
3¾ Digit DVM

FEATURES

- Single Ramp Integration
- Three measurement ranges 999, 1999, 2999
- Dual Polarity.
- Reading Rate up to 70 measurements per second
- Overrange Indication, 2 most significant digits flash
- Separate overrange output available on 1999 and 2999 ranges.
- Underrange output
- Operating voltage 13V to 17V.
- Power consumption 30mW typical.
- 7 segment or BCD output
- Controllable display brightness.
- Load enable freezes display.
- Hold input halts measurement

PIN CONFIGURATION

28 LEAD DUAL IN LINE



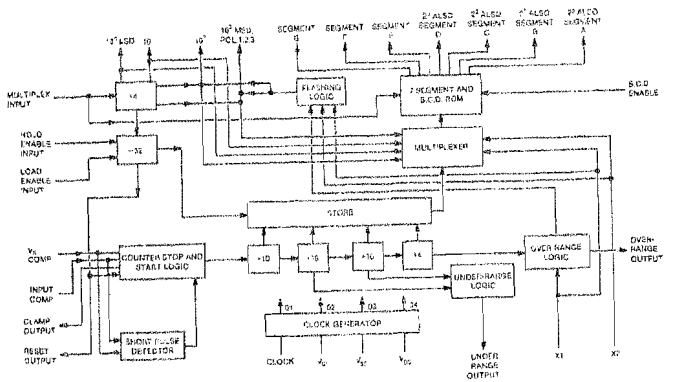
See next page for details of Pin Functions.

DESCRIPTION

The AY-5-3500 is a single ramp, dual polarity digital voltmeter chip having a selectable scale length of 999, 1999, 2999

It is manufactured using the MTNS low voltage p-channel nitride technology. Low power dissipation achieved by the use of 4-phase logic with an "on chip" clock generator.

BLOCK DIAGRAM



PIN FUNCTIONS

OVERRANGE OUTPUT
This output goes to logic '1' as soon as an overrange count has been detected. It returns as logic '0' at the end of the measurement cycle.

It operates at 2000 on the 1999 range.
It operates at 3000 on the 2999 range.

MEASUREMENT CYCLE
The measurement cycle lasts 128 Multiplex clock periods. Data is transferred to the display store from clocks 113 to 120. The counters are reset from 121 to 128.

UNDERRANGE OUTPUT
The underrange output is a pulse from clock 105 to 112 if the reading is less than 250.

SCALE LENGTH SELECT

X1	X2	Scale
0	1	999
1	0	1999
0	0	2999

OVERRANGING

Range	Count	Display	Overrange Output
999	0XXX	XXX	0
	1XXX	1XXX First	0
	2XXX	XXX Two Digits	0
	3XXX	3XXX Flash	0
1999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	1XXX First Two	1
	3XXX	3XXX Digits Flash	1
2999	0XXX	XXX	0
	1XXX	1XXX	0
	2XXX	2XXX	0
	3XXX	3XXX First Two Digits Flash	1

CLAMP OUTPUT
The clamp output goes to a logic '1' after 3 Counter clock periods following the input from the V_{IR} comparator. This output is used to switch off the V_{IR} comparator thus reducing the average input current by a factor of approx. 70. Fig.2 shows input waveforms without use of clamp output and Fig.3 shows waveforms with use of clamp output and timing for Clamp output.

BCD ENABLE
Logic '0' = BCD
Logic '1' = 7 segment

BCD OUTPUTS
The BCD outputs appear on the 7 segment output lines (Logic '1' is the Active Level): E, F, G are blanked to logic '0'.
A = 2^0
B = 2^1
C = 2^2
D = 2^3

LOAD ENABLE
Logic '0' = Normal Operation
Logic '1' = Freeze Display

HOLD ENABLE
Logic '0' = Halts measurement cycle in reset state
Logic '1' = Normal Operation

RESET OUTPUT
Logic '1' resets ramp generator

NEGATIVE SIGN OUTPUT
Displayed on segment G output on 999 and 1999 ranges. Inhibited on 2999 range.

OPERATION

A linear stable ramp is generated and compared to zero volts and the input voltage in two comparators. The time between the changing of the comparator outputs is proportional to the magnitude of the input voltage, and the sequence of switching gives the polarity.

TIMING DIAGRAMS

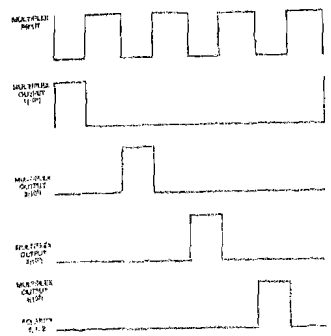


Fig.1 MULTIPLEX INPUT AND OUTPUT

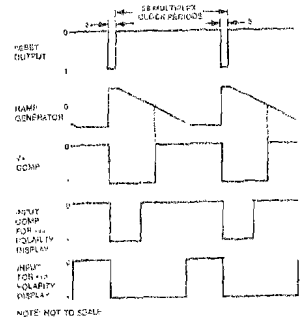


Fig.2 INPUT AND RESET OUTPUT

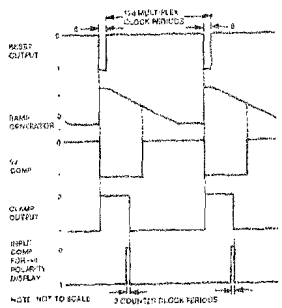


Fig.3 INPUT AND RESET OUTPUT TIMING DIAGRAM SHOWING CLAMP OUTPUT

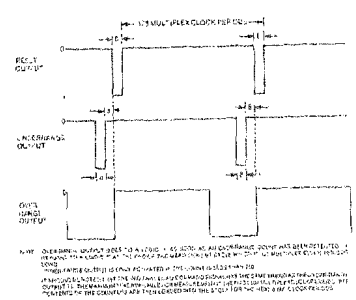


Fig.4 UNDER-RANGE AND OVER-RANGE OUTPUT

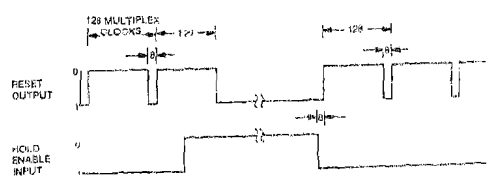


Fig.5 RESET OUTPUT WITH RESPECT TO HOLD ENABLE INPUT

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin	+20V to −0.3V
Storage temperature range	−65°C to +150°C
Ambient operating temperature range	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

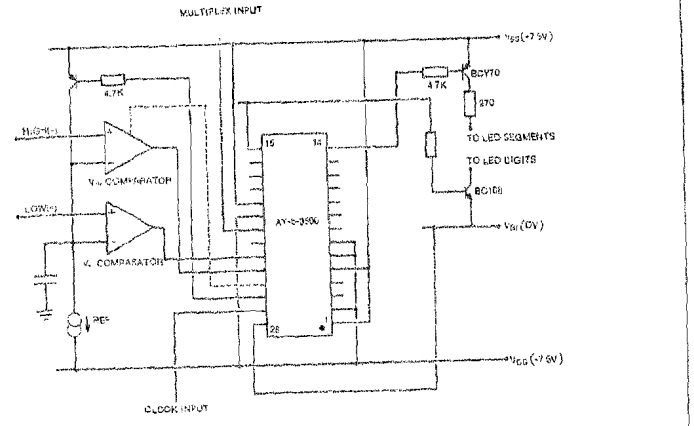
Standard Conditions (unless otherwise noted)

$V_{SS} = 0V$
$V_{GG} = -15 \pm 2V$
$V_{DI} = V_{LOG}/2$ (Note 8)
Temperature (T_A) = 0°C to +70°C

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Input					
Frequency	—	200	—	kHz	
Pulse width	1.5	—	—	µs	At logic '0' and '1' levels
Rise and Fall time	—	—	1	µs	
Logic '0' level	+0.3	—	+1	V	
Logic '1' level	−9	—	−17	V	
Multiplex Input					
Frequency	0.5	1.6	10	kHz	(See Note 1)
Pulse width	15	—	—	µs	
Logic '0' level	+0.3	—	+1	V	At logic '0' and '1' levels (Note 2)
Logic '1' level	−4	—	−17	V	
Control Inputs					
Logic '0' level	+0.3	—	+1	V	
Logic '1' level	−4	—	−17	V	
Leakage (all inputs)	—	—	1	µA	$V_{IN} = -10V$ at 25°C
Segment,Overrange, Underrange Outputs					
Logic '0'	—	—	30	kΩ	$V_{OUT} = +0.3V$ (Note 3)
Logic '1'	—	—	2	kΩ	$V_{OUT} = V_{DI} + 1V$ (Note 4)
Digit Select Outputs					
Logic '0'	—	—	1	kΩ	$V_{OUT} = -1V$ (Note 5)
Logic '1'	—	—	15	kΩ	$V_{OUT} = V_{DI} + 0.3V$ (Note 6)
Clamp and Reset Outputs					
Logic '0'	—	—	20	kΩ	$V_{OUT} = -0.2V$ (Note 3)
Logic '1'	—	—	5	kΩ	$V_{OUT} = V_{DI} + 1V$ (Note 7)
Supply Current	—	2	—	mA	$V_{GG} = -15V$ excluding output current

**Typical values are at +25°C and nominal voltages.

NOTE:
1. This gives a reading rate of typically 12 per second.
On the 2999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 64.
On the 1999 range, the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 42.
On the 999 range the maximum Multiplex clock frequency must be less than the Counter clock frequency divided by 21.
2. In 7 segment mode, outputs are energised when Multiplex Input is at Logic '1'.
The display brilliance is therefore controlled by the input Mark-Space ratio.
3. Output device connected to V_{SS}.
4. Output device connected to V_{DI} segment energised.
5. Output device connected to V_{SS} digit selected.
6. Output device connected to V_{DI}.
7. Output device connected to V_{DI} Reset condition.
8. V_{DI} is only applied to the output drivers, thus its absolute value is not critical.



AY-5-3500 D.V.M. -FSD 999 COMMON CATHODE LED DISPLAY

4¾ Digit Multi-Meter / Counter

FEATURES

- 4¾ digit display (± 29,999 max reading)
- 6 range autoranging
- Autozero, auto polarity
- Direct LED 7 segment drive
- Leading zero blanking/overrange blinking
- Multiplexed BCD output
- Single power supply
- On chip clock
- 20,000, 29,999 or freerun counter modes

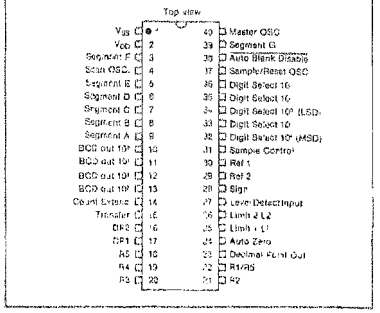
DESCRIPTION

The AY-3-3550 contains all the logic for a 4¾ digit DMM (±29,999 maximum reading) incorporating dual ramp integration. Outstanding features of this "state-of-the-art" DMM chip include 6 range autoranging, autozero, auto polarity, direct 7-segment LED drive, and multiplexed BCD outputs. An on-chip oscillator controls the sampling rate, digit select multiplexing and BCD counting.

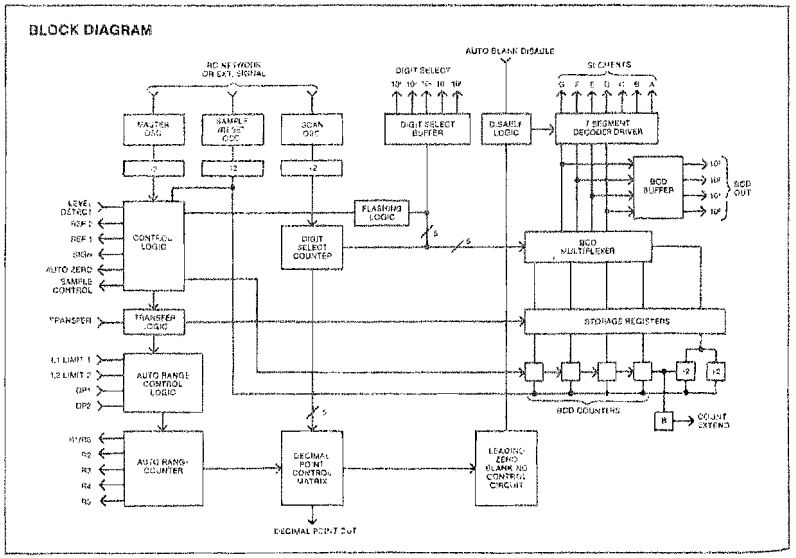
Fabricated in GI's advanced N-channel Ion Implant process to enable operation from a single power supply (+4.5V to +11V), the AY-3-3550 typically draws only 12mA when operating at +5V.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



Functional Description

Operation

(Refer to Figs. 1 and 2 and the Block Diagram) An input on the Sample/Reset OSC Input triggers the internal reset signal which in turn resets the internal BCD synchronous counters, synchronizes the master clock with the control signals and simultaneously activates the 10¹ Multiplex output. At the first master clock following the trailing edge of the internal reset, the 'Sample Control' signal is activated. This signal opens the switch in the analog section to integrate the unknown input voltage. After 10,000 internal clocks, the "Sample Control" signal is deactivated and either Ref SW1 or Ref SW2 activates depending upon the comparator logic level. This in turn switches the integrator to the opposite polarity source. Compared to the unknown input voltage, the integrator capacitor is discharged until the output voltage reaches the comparator threshold value. This variable time is proportional to the unknown voltage. The Comparator input voltage change at this time stops the internal counter and internally produces a transfer pulse to store the measured count. The storage registers are fed to the BCD multiplexer which is controlled by a digit select counter. According to the multiplexing sequence, the seven segment information and BCD data are made available at the Seven Segment and BCD Output pins. Note that the Autozero signal is deactivated during the counting cycle. Also, the correct polarity signal Sign Output is available when either of the reference switches are activated.

Transfer Logic and Timing

BCD data in the decade counter is transferred to the storage registers by means of an active Comparator Input. BCD data can also be transferred to the latches under the control of the Transfer input signal.

The Transfer signal at its active (high) state causes a continuous transfer and display mode or it can be pulsed to transfer on command. The Transfer signal in its active state also triggers the auto-range up-down counter whose function is determined by its control logic. The internal transfer pulse is superseded by an external signal applied at the Transfer Input. The Transfer signal in its active state also blanks the Decimal Point Output.

Scan OSC. Logic and Timing

The digit select counter and decoder is edge-triggered from either a signal applied at the Scan OSC. Input or from the output of the internal scan oscillator. The frequency of the internal oscillator is controlled by an RC network tied at this input. The digit select counter is set to the MSD position by a reset signal. Each of the five digit select line outputs is sequentially activated (low) when the corresponding digit is selected. The internal synchronization logic is incorporated to ensure that both the seven segment and BCD data from the selected latch are valid prior to enabling the corresponding Digit Select Output.

Sample/Reset OSC.

An input pulse on this pin activates an internal one-shot which resets the BCD decade counter and forces the digit select counter to the MSD position. This reset pulse also synchronizes the master oscillator frequency to control the logic outputs and BCD counters. An RC network tied to this input causes the internal oscillator to function at the frequency selected.

Leading Zero Blanking and Decimal Point Control

At the start of each MSD to LSD scan cycle, a blanking of leading zeros occurs until the decimal point active state is clocked. Any number following a decimal point is displayed. Leading zero blanking does not affect the BCD outputs and the 10¹ and 10² digits in the display. This feature allows the chip to work as a 3½ DMM. Leading zero blanking is inhibited whenever the Auto Blank Disable is tied to an active (low) level.

Autoranging

The autorange up-down counter is edge triggered by a transfer pulse (internal or external) in conjunction with the associated control logic. The autorange counter is decoded into one of the five output signals through buffers R¹ thru R5. Range R1 acts as R6 when the DP2 control signal is zero.

Down Ranging

If the display count is less than 1800, the autorange counter is downranging, except in the resistance range (Function 2). When in this mode, the counter is upranging. Between count 1800 and 20,000, no autorange movement occurs. At 20,000 or above the counter upranges. Depending upon the state of the Limit 1 and Limit 2 control signals, the scale length could be 20,000, 29,999 or free run.

Flashing Logic

The MSD digit flashes when the count is above 20,000 and the chip is in scale length 29,999 (L2=1,L1=0). If leading zero blanking is not disabled in this mode, all digits except MSD are blanked out and the MSD flashes indicating an overrange situation in the highest possible range. This feature prevents current drain through the segments in an overflow condition.

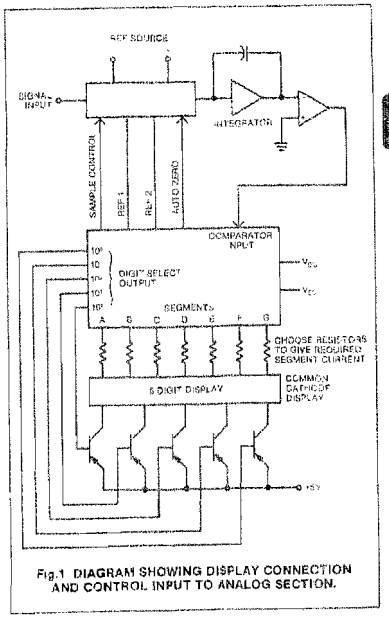
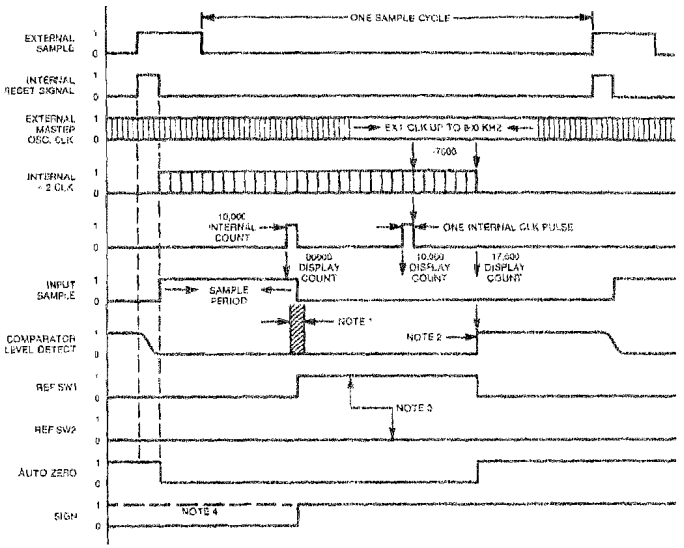


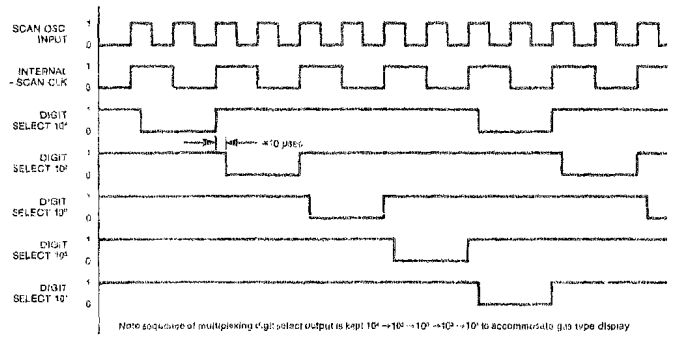
Fig.1 DIAGRAM SHOWING DISPLAY CONNECTION AND CONTROL INPUT TO ANALOG SECTION.

TIMING DIAGRAMS



NOTE
1) During the shaded area, the comparator level DETECT INPUT should be well defined and no noise should be allowed at the input
2) The comparator change is determined by the EXTERNAL CIRCUIT at this point. The count in the counters is proportional to the input measuring voltage
3) The waveform of REF1 and REF2 would be reversed if the comparator level is in the opposite state
4) Polarity would be reversed if the comparator input is reversed

Fig.2 TIMING DIAGRAM OF CONTROL SIGNAL FOR ONE SAMPLE CYCLE



Note sequence of multiplexing digit select output is kept $10^4 \rightarrow 10^3 \rightarrow 10^2 \rightarrow 10^1 \rightarrow 10^0$ to accommodate gas type display

Fig.3 SCAN CLOCK INPUT AND MULTIPLEXING DIGIT SELECT OUTPUT

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... +20 to -0.3V
Storage Temperature ..... -55°C to 150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

Operating Temperature (T_A) = 25°C
V_{SS} = 0.0V
V_{DD} = +4.5V to +11V

Parameters	Min	Typ	Max	Units	Conditions
Clocks input voltage low	0.0	—	0.7	V	
Clocks input voltage high					
Pin No. 4,40	V_{DD}-1.0	—	V_{DD}	V	
Pin No. 37	V_{DD}+1.0	—	V_{DD}	V	
Master Clk Freq	DC	(Internal)	400	kHz	From 0°C to 70°C
Scan Clk Freq.	DC	(Internal)	10	kHz	From 0°C to 70°C
Sample Clk Freq.	DC	(Internal)	100	Hz	From 0°C to 70°C
Comparator input voltage HI	3.0	2.8	V_{DD}	V	At V_{DD} = 5V
Comparator input voltage LO	V_{SS}	2.0	2.5	V	At V_{DD} = 5V
Group A					
Input Logic Level HI	V_{DD}-1.0	—	V_{DD}	V	Input Resistance = 100KΩ
Input Logic Level LO	V_{SS}	—	V_{SS}+0.7	V	
Group 2 & 3					
Output Logic Level HI	V_{DD}-1.2	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS}+0.5	V	At 2.0mA
Group 4					
Output Logic Level HI	V_{DD}-1.0	—	V_{DD}	V	At 40μA (V_{DD} = 5V)
Output Logic Level LO	V_{SS}	—	V_{SS}+0.4	V	At 100μA
Group 1					
Output Logic Level HI	V_{DD}-1.2	—	V_{DD}	V	V_{DD} = 5V
Output Logic Level LO	V_{SS}	—	V_{SS}+1.2	V	V_{DD} = 5V @ 1mA
For REF1, REF2, Sample Control, Autozero & Clk Extend					
Output Rise Time	—	—	5.0	μs	V_{DD} = 5V
Output Fall Time	—	—	5.0	μs	
Supply Current	—	—	12	mA	@ V_{DD} = 4V, V_{SS} = 0V, Input Freq = 300 KHz

Pin Numbers

Group A = 15, 16, 17, 25, 26, 38
Group 1 = 3, 5, 6, 7, 8, 9, 23, 28, 29
Group 2 & 3 = 10, 11, 12, 13, 14, 32, 33, 34, 35, 36
Group 4 = 16, 19, 20, 21, 22, 24, 27, 30, 31

Fig.4 TRUTH TABLE FOR DECIMAL POINT AND AUTORANGE FUNCTIONS

Auto Range	Function 1 (ACV, DCV.)		Function 2 (Resistance)		Function 3 (Current)		Function 4	
	DP1	DP2	DP1	DP2	DP1	DP2	DP1	DP2
	0	1	1	0	0	0	1	1
R1	A		*		*		D	
R2	B		C		*		B	
R3	C		E		B		C	
R4	D		D		C		D	
R5	E		C		D		E	
R6	*		B		E		*	

NOTES.
1) *denotes illegal states
2) RANGE 1 (R1) output = R1 when DP2 = 1, RANGE 1 OUTPUT acts as RANGE 6 OUTPUT when DP2 = 0
3) When decimal point A is "ON", no blanking occurs
4) DECIMAL POINT POSITION is shown in Fig.5 below.

MSD				LSD
DIGIT SELECT				
10^4	10^3	10^2	10^1	10^0
2 / B	9 / C	9 / D	9 / E	9 / A

POSITION OF DECIMAL POINT ON DISPLAY

Fig.5

Scale Length	Condition		Leading Zero Blanking	Blinking MSD on Overrange
	L2	L1		
20,000	0	1	YES	NO
20,000	0	0	YES	NO
29,999	1	0	YES	YES, OVER 20,000 COUNTS
FREE RUN COULD BE USED AS FREQ CTR	1	1	NO	NO

Fig.6 SCALE LENGTH SELECT AND OVERFLOW CONDITION TABLE

DECIMAL	7-SEGMENT							BCD			
	A	B	C	D	E	F	G	2^0	2^1	2^2	2^3
0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	1	1	1	1	1	0	0	0
2	0	0	1	0	0	1	0	0	1	0	0
3	0	0	0	0	1	1	0	1	1	0	0
4	1	0	0	1	1	0	0	0	0	1	0
5	0	1	0	0	1	0	0	1	0	1	0
6	0	1	0	0	0	0	0	0	1	1	0
7	0	0	0	1	1	1	1	1	1	1	0
8	0	0	0	0	0	0	0	0	0	0	1
9	0	0	0	0	1	0	0	1	0	0	1

NOTE
Logic "0" = Low Segment "ON"
Logic "1" = High Segment "OFF"

Fig.7 Seven segment and BCD output truth table.

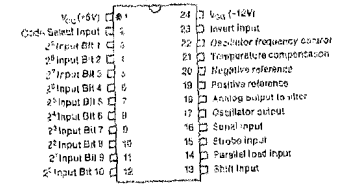
10 Bit D/A Converter

FEATURES

- 10 Bit resolution
- 8 Bit accuracy (linearity).
- Parallel or serial input.
- Simple external circuitry.
- Binary or 2's complement coding
- Output inversion
- TTL/CMOS compatible inputs.
- Monotonic output
- 8.5 ms settling time for 10 bits with 2nd order filter.
- 1.23 ms settling time for 8 bits with 2nd order filter.

PIN CONFIGURATION

24 LEAD DUAL IN LINE

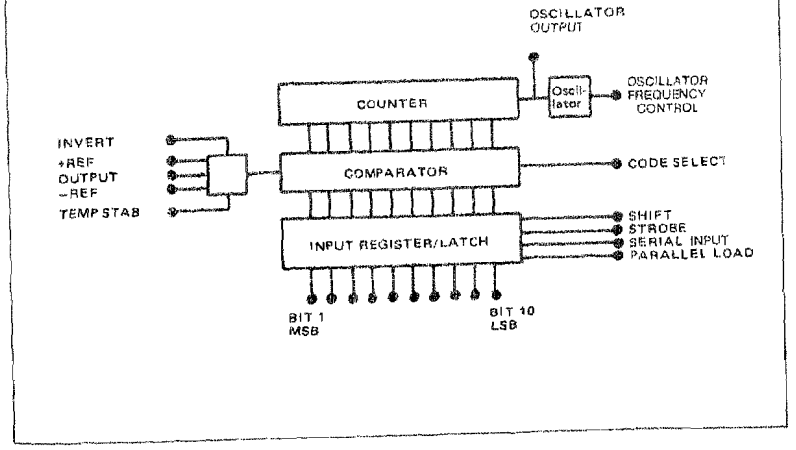


See next page for details of Pin Functions

DESCRIPTION

The AY-5-5053 is a 10 bit D/A converter employing the stochastic conversion technique, requiring no precision components other than a voltage reference.
The input can be either serial or parallel with Binary or 2's complement coding

BLOCK DIAGRAM



Maximum Ratings*

Voltage on any pin with respect to V_{cc} pin	−20 to +0.3 Volts
Ambient operating temperature range	0°C to +70°C
Storage temperature range	−65°C to +150°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{cc} = +5V ± 0.5V
V_{DD} = −12V ± 0.5V
Positive reference = +4.5V
Negative reference = 0V
Clock Frequency = 800KHz
R_T (temp comp) = 12K Ω 5%
R_L (linearity) = 270 Ω nom
R_O (osc. frequency) = 10K Ω nom

Characteristic	Min	Typ**	Max	Units	Conditions
Clock Frequency	100	800	1000	kHz	
Voltage Stability	—	5	—	%/V	
Temp. Stability	—	0.2	—	%/°C	
Output Logic '0'	—	—	0.4	Volt	R_L = 6.8K to V_{cc} I sink = 1.6mA
Output Logic '1'	V_{cc}−1	—	—	Volt	R_L = 6.8K to V_{DD} I source = 100μA
Inputs					
Logic '0' Level	—	—	+0.8	Volts	
Logic '1' Level	V_{cc}−1.5	—	—	Volts	
Leakage Current	—	—	10	μA	V_{IN} = V_{cc} −5V
Capacitance	—	—	10	pF	
Shift Clock Frequency	10	—	1000	kHz	
Resolution	—	10	—	Bits	
Differential Linearity	—	—	¼	LSB	
Linearity	—	0.5	2	LSB	After trimming at 0.5 FSD
Temperature Co-efficient	—	50	—	PPM/C°	Excluding reference and filter drift
Supply current	—	—	20	mA	(140mW)
Reference Current	—	—	100	μA	Max at ½FSD

**Typical values are at +25°C and nominal voltages.

TABLE 1 INPUT CODING

BINARY	2's COMPLEMENT	ANALOG OUTPUT
0000000000	1000000000	0
0000000001	1000000001	+LSB
0111111111	1111111111	½V ref−LSB
1000000000	0000000000	½V ref
1000000001	0000000001	½V ref+LSB
1111111111	0111111111	V ref−LSB

SETTLING TIME AND BANDWIDTH D/A CONVERTER

NO. OF BITS	10		8		6	
Filter Type	1st Order	2nd Order	1st Order	2nd Order	1st Order	2nd Order
Filter time constant mSec	5.3	0.66	1.1	0.16	0.2	0.06
Settling time to ± ½ LSBmSec	45	6.8	7.7	1.23	0.8	0.32
Bandwidth Hz — 0.1%	1.35	14.8				
— 0.4%			13	116		
—1%					112	618
— 10B	13.5	135	65	597	400	1784

PIN FUNCTIONS

Pin No.	Name	Function
1	V_{cc}	Positive power supply +5V
2	Code Select Input	Logic '0' gives Binary coding. Logic '1' gives 2's complement coding. (See table 1).
3-12	Bits 1-10 Input	Parallel data inputs. Bit 1 is MSB.
13	Shift Input	Clock input for serial mode. Data is shifted in on the '0' to '1' logic transition. In the parallel mode this input must be at logic '1'
14	Parallel Load Input	In the parallel mode data is loaded into the data register when this input is at logic '1'. This input should be at logic '0' in parallel mode operation.
15	Strobe Input	A logic '1' on this input loads serial data into the data register. The data is latched when the input returns to logic '0'. This input should be at logic '0' in parallel mode operation
16	Serial Input	Serial data input bit 1 first.
17	Oscillation Output	TTL compatible oscillator output signal.
18	Analog Output	Analog output to low pass filter. This output is a stochastic pulse waveform having a mean amplitude equal to the required DC output level.
19	Positive Reference	+4.5V nominal reference of voltage.
20	Negative Reference	0V reference, connected to 0V via a 500 ohm variable resistance used to adjust the error at half scale to zero.
21	Temperature Compensation	This pin is connected to V_{cc} via a 12K ohm 5% resistor to achieve the stated temperature stability. The temperature stability can be improved by a factor of 4 by using an 18K Ω resistor in parallel with a DPGC49−39K Ω thermistor instead of the 12K Ω resistor.
22	Oscillator Frequency Control	This pin is connected to V_{cc} via a 50 K Ω variable resistor used to adjust the oscillator frequency to the required value.
23	Invert Input	A logic '1' on this input inverts the output
24	V_{DD}	Negative power supply −12V.

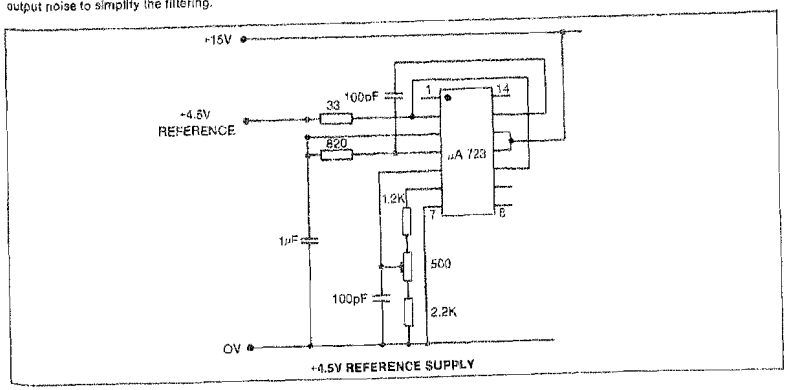
OPERATION

The binary word contained in the input register is compared with the output of a continuously cycling counter. The output of the comparator is high whenever the binary input is greater than the counter, this results in an output waveform which has a mean value equal to the desired analog output. This output is passed through a low pass filter to recover the DC level.

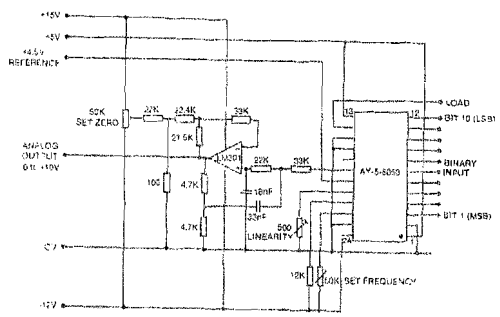
The counting sequence of the binary counter has been chosen to optimise the conversion characteristics and the frequency of the output noise to simplify the filtering.

MULTIPLIER OPERATION

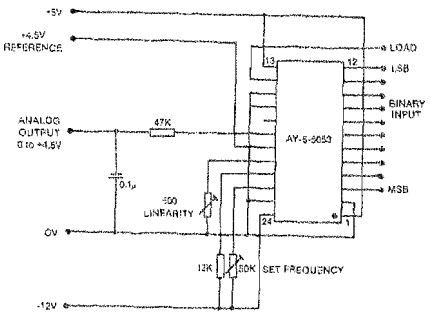
The AY-5-5053 may be used as a Digital—Analog multiplier by replacing the positive reference with the Analog multiplier input voltages in the range 0 to +4.5 Volts may be used. The accuracy is of the order of 0.1% and the settling time is as for normal operation



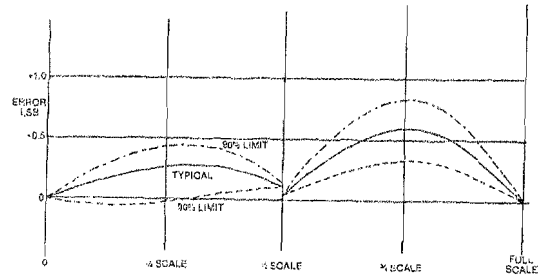
+4.5V REFERENCE SUPPLY



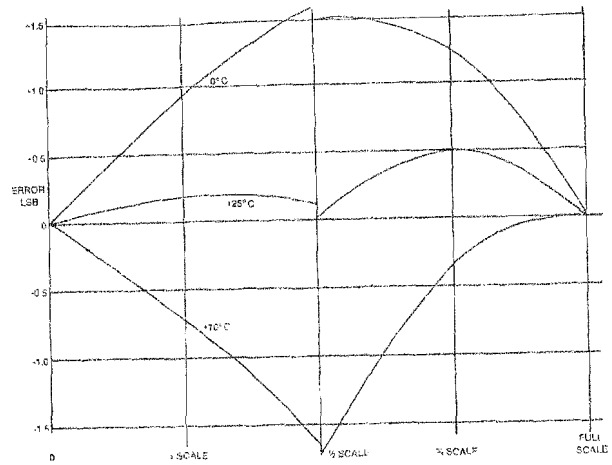
10 BIT D/A CONVERTOR PARALLEL INPUT SECOND ORDER FILTER 0 to +10V OUTPUT



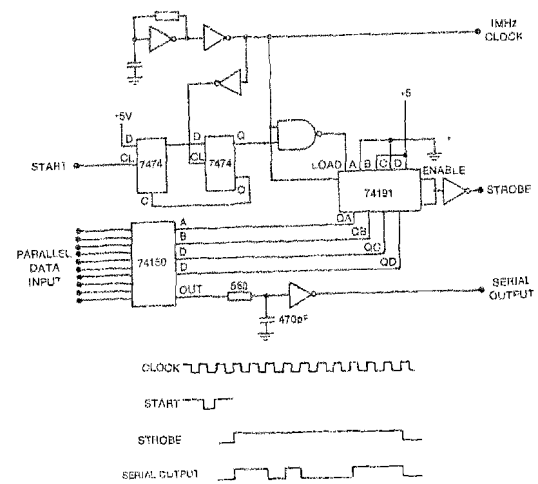
10 BIT D/A CONVERTOR FIRST ORDER FILTER



D/A CONVERTOR LINEARITY



D/A CONVERTOR TYPICAL TEMPERATURE STABILITY



SERIAL DATA TRANSMITTER FOR AY-5-5053 D/A CONVERTOR

10 Bit A/D Converter Control

FEATURES

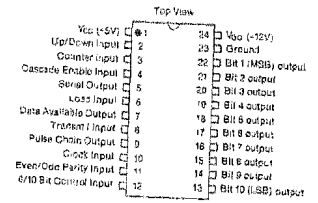
- 10 Bit Resolution
- 200 ns settling time to ½ LSB
- Integral serial data transmitter 8/10 Bits with parity
- Parallel outputs
- TTL/MOS compatible inputs and outputs

DESCRIPTION

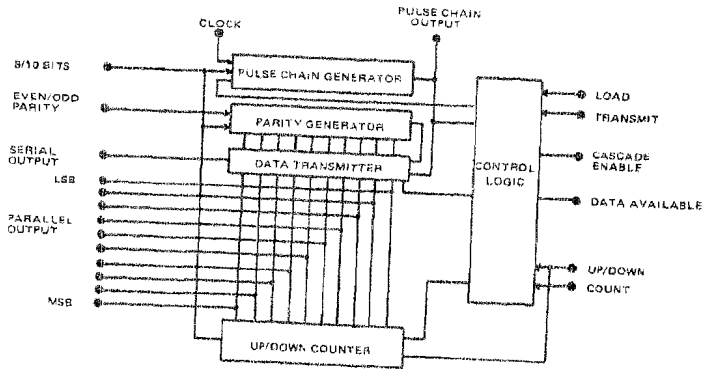
The AY-5-5054 is designed to work in conjunction with the AY-5-5063 to form a 10 Bit A/D converter. It consists of a 10 bit up/down counter, control logic and a serial data transmitter.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Pin No.	Name	Function
1	V_{CC}	Positive Power supply (+5V)
2	UP/DOWN	Controls direction of counting, at logic '1' for UP
3	Counter Input	Clock input for UP/DOWN counter. Control logic inhibits the clock during UP/DOWN transition, during loading of the transmitter and when the counter has reached all '0's or all '1's
4	Cascade Enable Output	This output goes to logic '1' at the end of data transmission for one clock cycle. It can be connected to the Transmit input of a second AY-5-5054, enabling a series of convertors to be interrogated sequentially using only one line
5	Serial Output	Serial data output from transmitter, 8 or 10 bits plus parity. MSB first.
6	Load Input	A pulse to logic '1' on this input loads data into the transmitter. If data is being transmitted the command is stored until the transmission is complete.
7	Data Available Output	This output goes to logic '1' when valid data has been loaded into the transmitter. It returns to 'logic 0' when the transmission has been completed
8	Transmit Input	A pulse to logic '1' on this input causes transmission to commence. The pulse must last at least one but no more than 8 clock periods
9	Pulse Chain Output	A chain of 9 or 11 pulses is output on this line during data transmission. It would be used to clock data into the receiver
10	Clock Input	Clock for the data transmitter 1MHz max
11	Even/Odd Parity Input	Logic '1' gives even parity
12	8/10 Bit Control Input	Logic '1' gives 8 bit data transmission
13-22	Parallel Data Outputs	Connect to Parallel inputs of AY-5-5063
23	Ground	
24	V_{DD}	Negative power supply (-12V).

A/D CONVERTOR RESPONSE TIME

1 SIMPLE TYPE - 1ST ORDER FILTER

NO. OF BITS	10	8	6
Filter time constant	4.5msec	1.2msec	0.3msec
Clock frequency	10kHz	40kHz	160kHz
Settling time to ½LSB	200msec	50msec	12.5msec

2 VARIABLE CLOCK FREQUENCY TYPE

If the counter clock frequency is arranged to be proportional to the difference between the input voltage and the actual convertor output, the response speed can be considerably improved. In this case the system becomes a linear one and a 2nd order filter can be used without danger of oscillation.

NO. OF BITS	10	8
Filter time constant	0.66msec	0.104msec
Settling time to ½LSB	1.5msec	3msec
Max. clock frequency	450kHz	1MHz

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} pin −20 to +0.3 Volts
Ambient Operating Temperature range 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these condition is not implied—operating ranges are specified below.

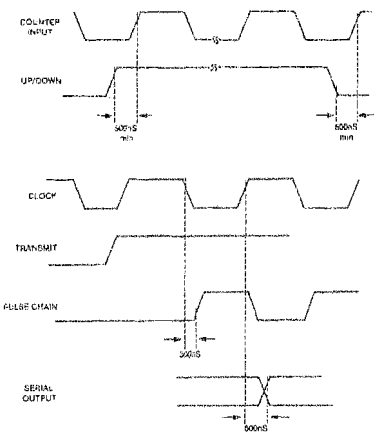
Standard Conditions (unless otherwise noted)

V_{CC} = +5 ±0.5V
V_{GG} = −12 ±0.5V
Operating Temperature (T_A) = 0°C to +70°C

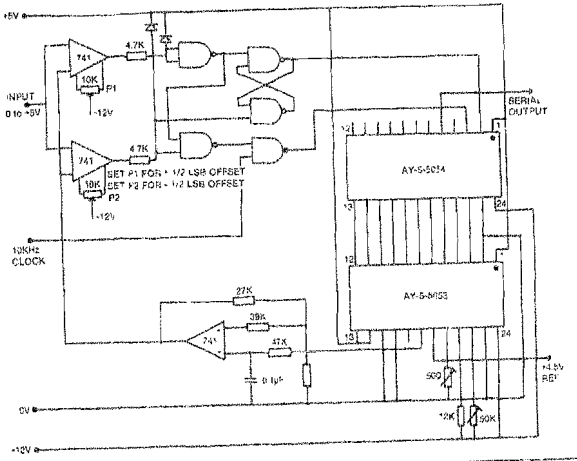
Characteristic	Min	Typ**	Max	Units	Conditions
Clock and Clock Inputs					
Logic '0' level	—	—	+0.8	Volts	
Logic '1' level	V_{CC}−1.5	—	V_{CC}+0.3	Volts	
Frequency	DC	—	1	MHz	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	$V_{IN}=V_{CC}-10V$
Logic Inputs					
Logic '0' level	—	—	+0.8	Volts	
Logic '1' level	V_{CC}−1.5	—	V_{CC}+0.3	Volts	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	$V_{IN}=V_{CC}-10V$
Output					
Logic '0' level	—	—	+0.4	Volts	I_{OL}=1.6mA
Logic '1' level	V_{CC}−1	—	—	Volts	I_{OH}=100µA
Power	—	240	—	mW	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



SIMPLE 10 BIT A/D CONVERTER



PRELIMINARY INFORMATION

Sequential Boolean Analyzer

FEATURES

- 1023 words of program
- 30 programmable inputs, outputs, or multiplexed input/outputs
- 16 element stack and 120 element Read/Write memory
- AND, OR, XOR, COMPARE, INVERT basic logic functions
- Serial processing of inputs and stored information provides very easy programming in Boolean logic
- Versatile clock generation scheme
- TTL compatible inputs and outputs
- Simulator and software program compiling facilities available

DESCRIPTION

The SBA is a microprogrammable Sequential Boolean Analyzer which forms the basic controlling element for many systems requiring timing and control functions. The SBA is fabricated in GI's low voltage Ion Implant N-channel process resulting in high speed operation and low power dissipation

APPLICATIONS

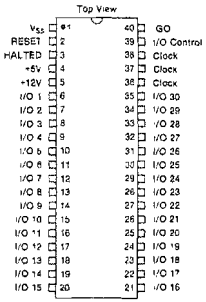
The SBA is suitable for a very wide spectrum of applications such as:

TELECOMS: Simple PAX controllers, Relay circuit control, Answering machine controllers, Line seeker/monitor.

INDUSTRIAL: Complex sequential timers, Small machine controllers, Special purpose digital clocks, Alarm monitor.

CONSUMER: Gaming machines White goods timers, Combination locks, Pinball machine/one arm bandit.

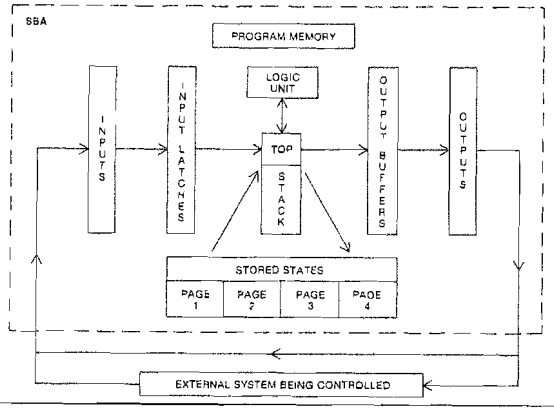
PIN CONFIGURATION
40 LEAD DUAL IN LINE



MICROPROCESSORS: As a slave processor for BCD/binary conversion Binary/BCD conversion, Alarm condition monitor/interrupt generator, Peripheral controller.

In general the SBA is best suited to applications where a control response is required in milliseconds rather than microseconds.

BLOCK DIAGRAM AND DATA PATHS



PIN FUNCTIONS

RESET Input	When taken to a logic '0', this input will reset the program to the start position.
GO Input	When taken to a logic '0', this input will halt the program at the end of the program cycle and will activate the HALTED output When taken to a logic '1', the program will cycle continuously
HALTED Output	A logic '1' on this output indicates that the program has stopped cycling
INPUTS/OUTPUTS	There are 30 input/outputs on the circuit which can be mask programmed as inputs, outputs, or inputs/outputs
I/O Control	When this output is at logic '0', the circuit will output information When it is at logic '1', it will read input data

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -0.3V to +15V
Storage Temperature Range ..... -55°C to +150°C
Operating Ambient Temperature Range ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{CC} = +12V ± 10%
V_{DD} = +5V ± 15%

Characteristic	Min.	Typ.	Max.	Units	Conditions
Clock	10	—	800	kHz	Note 1
Inputs					
Logic '0' level	+0.3	—	+0.4	V	
Logic '1' level	+2.4	—	+12	V	
Current	—	—	10	µA	V_{IN} = +12V
Timing	—	—	—	—	Note 2
Outputs					
Logic '0'	—	100	—	Ohms	0.7V at 7mA
Sink Current	—	7	20	mA	Max total power 150mW
Logic '1'	1.2	—	—	MOhms	open drain
Leakage current	—	—	10	µA	V_{OUT} = +12V
Timing	—	—	—	—	Note 2

NOTES:
1. Clock frequency controlled by external R/C network
2. The timing of inputs depends on the clock frequency and the program length Refer to the detailed descriptions

PART I General Information

A. INTRODUCTION

The Sequential Boolean Analyzer (SBA) is a very simple single bit processor which can directly evaluate a set of Boolean equations.

The use of Boolean Equations as a 'programming language' has a number of unique advantages.

1. It is concise
2. It is standarized worldwide
3. engineers already use it and *understand it*
4. universities teach it now and have done so for many years.
5. it serves the dual purpose of both program and documentation
6. *it* has stood the test of time.

The equations define the logic that controls the system to which the SBA inputs and outputs are connected

In addition to Boolean logic, most systems require that some events have to be 'remembered', this being the reason for the use of flip flops in TTL type logic implementations. In the SBA a number of internal storage elements are provided for such purposes

A memory is used to hold an encoded version of the Boolean equations that define the desired function of the SBA and there is a one to one correspondence between the data in this memory and the Boolean Equations as written by an engineer.

B. PRINCIPLE OF OPERATION

A block diagram of the SBA showing the program memory, inputs, logic unit, stack, stored states and outputs is shown in Fig. 1.

The SBA functions as follows:

1. The new inputs are read in from the system being controlled and are latched into the input latches
2. The SBA now reads the Boolean equations out of the memory and, using the logic unit and the stack, it processes the input data and stored states one Boolean term at a time to produce results which are either 'remembered' as stored states or placed in the output buffer.
3. The Boolean equations are taken from the memory term by term and when all the equations have been evaluated the results are transferred from the output buffers to the outputs and thus to the system being controlled. The program address counter is then reset and the cycle begins again.

C. COMBINATIONAL LOGIC

If the SBA is used to emulate combinational logic, then the Boolean equation which defines the logical function will only contain input terms and output terms. For example·

A = B.C.-D+E.F. (X + -X.G)
L = T + E.F. (X + -X.G)

where . signifies logical AND
+ signifies logical OR
- signifies negate (-D read not D)
A and L are outputs
all other letters are inputs.

The number of program steps required to evaluate the above Boolean equations can be reduced by using a stored state to save the value of E.F. (X + -X.G) after it has been evaluated the first time This partial result can then be used in the second equations. Now we have.

a. stored state = E.F. (X + -X.G)
b. A = B.C. + stored state
c. L = T + stored state

This example serves to illustrate how the equations can sometimes be optimized by trading off stored state memory against program memory.

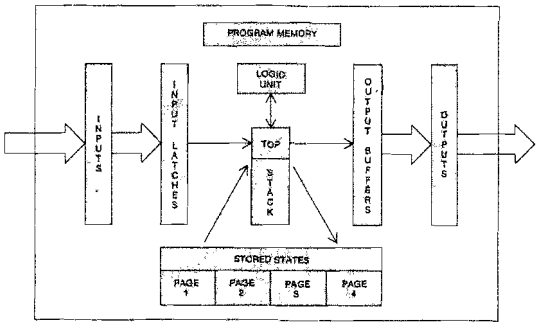


Fig. 1 BLOCK DIAGRAM

D. SEQUENTIAL LOGIC

Although some problems are combinational in nature, the vast majority of practical problems are sequential

A sequential system is one in which the response to a given set of input conditions is dependent on the previous history of the system. An example might be a digital clock where normally the seconds digits are incremented except when they are at 59 when they are reset to 00. In other words the next response of the counter depends on its current value and there may be different responses depending on different current values.

All sequential systems can be described by a combinational network in which some of the results of the Boolean equations are stored in a memory. It is this memory that remembers the history or 'state' of the sequential system.

Thus the stored state memory of the SBA has its main use in remembering the 'state' of the system being implemented. Each time the SBA evaluates the complete set of Boolean equations describing a sequential system, it uses the stored states as part of the equations. As the evaluation proceeds, the stored states may be changed if the Boolean equations demand it

A simple example is shown by a Vending Machine where there are two major states —1. not enough money to buy anything.
2 enough money, so supply the goods.

In this example some of the stored states would be used to keep count of the money that has been fed into the machine. The Boolean equations controlling the dispensing of the goods would all contain a term involving the stored state that could never be logically true if there were not enough money to buy the goods. As soon as goods were bought and supplied the stored states holding the 'amount' of money would be altered to reflect that the goods had been supplied thus switching the system back to state 1.

E. SYSTEM DESCRIPTION

The Sequential Boolean Analyzer consists of the following major components (refer to Fig. 1)·

1. **A Program Memory which holds the set of Boolean equations defining the system operations. In the single chip version of the SBA this is contained in an on-chip mask programmable ROM. There will be another version in which the program memory is off the chip and it can then be ROM. RAM or PROM as required.** The Boolean equations which define the logical relationships between the SBA inputs, stored states, and outputs are stored in the memory as 8 bit words in an encoded form. An exact definition of the code is given in the next section
2. A set of up to 30 input buffers which are latched at the start of the evaluation of Boolean equations. This is done so the input values are consistent during the whole period of time it takes to evaluate all the Boolean equations once
3. A number of pages of 30 stored-state flip flops which can be grouped to emulate counters and shift registers, or used singly as 'flags' to remember the state of the machine, or in logic equation reduction. The SBA addressing structure only allows for 30 addresses, but the number of stored states is increased to 120 by having typically 4 pages of 30 each Two instructions control a 'page counter'. One steps the counter and so changes the page, and the other sets it back to the first or 'home page'. Thus an infinite number of pages is theoretically possible, the SBA stepping through them in sequence as required with the option to return to the start at any time
4. A logic unit which can perform all the possible logic functions of two variables, namely AND, OR, EXCLUSIVE OR and COMPARE, and also negate (invert). The truth tables of the functions are shown in Fig. 2. Any logic system can be described by a set of Boolean equations written with these operators

   The logic unit always has two inputs and produces one output and there are two types of action.

   (a) One input comes from an input latch or stored state; the second input comes from the top of the stack, and the result is placed on the top of the stack.
   (b) One input comes from the top of the stack; the second input comes from the next location of the stack; and the result is left on the top of the stack.

   The exact operation of the various Boolean equation evaluation codes is defined in the next section
5. The stack is always involved in logical evaluations, as the top of the stack is always one of the operands to the logic unit The stack is just a pile of Boolean values and can be imagined as a vertical shift register in which data is always put into or taken from the top. When data is added to the stack, it is said to be 'pushed' onto the stack. The new data becomes the top of the stack and all the previous data is pushed down the stack by one place. If the opposite is performed, the data in the stack is moved up by one place and the stack is said to be 'popped'. The top of the stack will be lost and the data previously just below the top will become the new top of the stack

   The data stack in the SBA is normally used as workspace or accumulator and the top of the stack is used in most of the instructions together. sometimes, with the next location down. However, the stack can also be used to store temporary Boolean variables and helps greatly in the evaluation of Boolean equations containing brackets. For example a function such as:

   A. (B.C. + (D.E + F.G).(H.I + J.K))

   would be evaluated in the following way:

Operation	Result
(a) evaluate D.E	D.E
(b) push into the stack	
(c) evaluate F.G	
(d) OR	D.E+F.G
(e) push into the stack	
(f) evaluate H.I + J.K as in (a)-(d)	
(g) AND	
(h) push into stack	(D.E+F.G).(H.I+J.K)

AND			OR			EXCLUSIVE OR			COMPARE		
A	B	RESULT	A	B	RESULT	A	B	RESULT	A	B	RESULT
0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	1	1	0	1	0
1	0	0	1	0	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1	0	1	1	1
Output true only if both inputs true.			Output true if either input true.			Output true when inputs differ			Output true when inputs compare		

Fig. 2 LOGIC FUNCTIONS

Operation	Result
(i) evaluate B.C	
(j) OR	B.C+(D.E+F G).(H.I+J.K)
(k) AND the stack with A	Final result.

Naturally this is not the only way the stack can be used, the variation being limited only by the imagination.

6. A set of up to 30 output buffers which have their new values stored in them as the Boolean equations are evaluated. When all the equations are complete, at the end of a program cycle, the data on the output buffers is relatched into the output drivers connected to the system being controlled. In this way the external outputs of the SBA are updated once per cycle and remain unchanged until the end of the next complete evaluation of the Boolean equations.

F. INPUT/OUTPUT

It has been noted that there can be up to 30 inputs and up to 30 outputs available in an SBA. However, because of the physical limitation of an actual device, if there are more than a *total* of 30 inputs and outputs then inputs and outputs are multiplexed onto the same pins. So the device will be available with 30 pins mask programmable to be inputs, outputs or multiplexed input/outputs

G. CONTROL LOGIC

As well as the major functional blocks described above, the SBA contains some simple control logic which operates transparently to the user. At the end of a complete program cycle, i.e. at the Restart instruction, the following actions are performed:

(a) the contents of the output buffers are relatched into the outputs
(b) the top of the stack is set to a logic 1
(c) the page counter is set to the home page
(d) new inputs are latched
(e) the program address counter is set to point at the first term of the first Boolean equation.

Once the SBA has started a program cycle, the program address counter is simply incremented every SBA clock cycle, the instruction read out and acted upon.

H. SBA RESPONSE TIME

It is implicit in the description of the operation that the speed of response of the SBA to an external system being controlled is determined by the length of time it takes to evaluate the complete set of Boolean equations once. This is because the inputs and outputs are only latched once per program cycle of the SBA's operation.

The SBA is designed in such a way that all its logical operations and data transfers take the same time to execute (in fact, one of the SBA's internal clock cycles) and so the response time of the output of the SBA to new inputs from the system being controlled by the SBA is directly proportional to the number of Boolean operations required to define the control function. This response time will typically be of the order of a few milliseconds.

I. DATA PATHS

The data paths available in the SBA are illustrated in Fig. 3. The focal point as far as data is concerned is the top of the stack since all data transfer go to or come from the top of the stack. The stack is loaded from an input or stored state. The logic unit can perform any logical function on it and the result can then be stored on any output buffer or a stored state.

Note that it is not possible for Boolean equations to use terms involving data on the output buffers. If such a facility is absolutely necessary, then a copy of the output buffer state must be made in a stored state so that the data path to the top of the stack is made available. The outputs of the SBA can be connected back to inputs either directly or via some piece of circuitry. A direct connection forms a stored state that can be accessed from outside the SBA. This can also be a limited source of extra stored states. External logic can be connected between outputs and inputs or even keys and switches. This latter possibility is useful in, say, scanning a matrix switch or selecting a code switch, and reduces external circuitry

However, in general, the outputs of the SBA are connected to the parts of the external system that controls its actions and the inputs of the SBA are connected to parts of the system that monitor its current state.

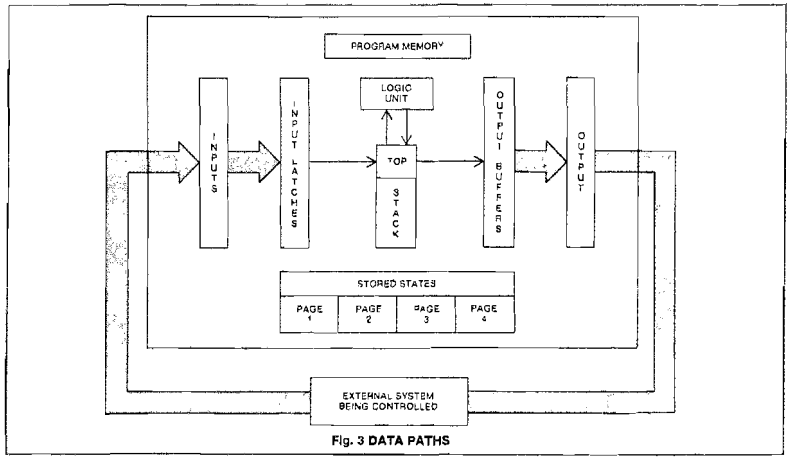


Fig. 3 DATA PATHS

J. BOOLEAN EQUATIONS IN THE PROGRAM MEMORY

In order to make the best use of the space available for memory, the codes representing the Boolean operations should be as efficient as possible. It has been determined that about 20 instructions would provide a good compromize between the number and efficiency of the instructions. Given also that about 30 inputs and outputs were suitable for the requirements of the type of system likely to be controlled by an SBA, the following scheme is used.

An 8 bit word is used for each instruction code. 5 bits provide an address for the inputs, outputs or stored states and, if two of the 32 available addresses are reserved for addressless instructions, the remaining 3 bits of the code enables a total of 24 instructions to be made available.

The 8 bit binary word is conveniently represented by 3 octal (redix 8) digits ranging from 0 to 377 (00 000 000 to 11 111 111 binary). The least significant 3 binary digits are treated as the instruction, and the 5 most significant bits as the address. Addresses 1 to 36 (octal) represent the 30 addresses required throughout the SBA (1-30 in decimal). Addresses 0 and 37 (all 0's and all 1's in binary) are reserved for instructions as shown in Fig. 4

Memory Code in OCTAL		MNEMONIC	Functional Description of Code
01 to 36	0	ANDIN	This input specified by the address is ANDed with the top of the stack.
01 to 36	1	NANDIN	The logical inverse of the input specified by the address is ANDed with the top of the stack.
01 to 36	2	ANDSS	The stored state specified by the address* is ANDed with the top of the stack.
01 to 36	3	NANDSS	The logical inverse of the stored state specified by the address* is ANDed with the top of the stack
01 to 36	4	ASPI	The stored state specified by the address* is ANDed with the top of the stack. then a 1 is pushed onto stack
01 to 36	6	NASPI	The inverse of the stored state specified by the address* is ANDed with the top of the stack then a 1 is pushed onto stack.
01 to 36	5	STORE	The value on top of the stack is stored in the etored state specified by the address* and a logical 1 left on the stack
01 to 36	7	OUTPUT	The value on top of the stack is stored in the output buffer specified by the address and a 1 left on the stack.

Memory Code in OCTAL	MNEMONIC	Functional Description of Code
000	RESTART	Restart evaluation of equations
001	INVERT	Invert top of stack
002	PAGE	Change Page
003	HOME	Back to Home Page
004	PUSH 0	Push logic 0 onto stack
005	PUSH 1	Push logic 1 onto stack
006	PUSH C	Push and copy top of stack
007	POP	Pop the stack
370	AND	Perform the function on the top two locations of the stack. Store result on top of stack
371	OR	
372	EXOR	
373	COMP	
374	PAND	Perform the function on the top two locations of the stack. Push result into stack leaving logic 1 on top
375	POR	
376	PEXOR	
377	PCOMP	

*The address of a stored state defines 1 of 30 on the currently enabled pege

Fig. 4 BOOLEAN EQUATION CODES

Description of Codes.

The codes used for defining the Boolean equations fall into four categories:

(a) single operand instructions which affect the stack
(b) logical operations taking inputs from the stack and storing the result on the stack
(c) data transfer instructions for inputs, atored states, and outputs
(d) program control instructions.

Category (a) — stack manipulation (See Fig. 5):

1. Invert top of stack. The Boolean value is taken from the top of the stack and replaced by its logical inverse; a 1 becomes a 0, and a 0 becomes a 1. The stack is neither pushed or popped.
2. Push 0 onto stack. All data values on the stack are pushed down one place and a logic 0 entered on top of the stack
3. Push 1 onto stack. All items in the stack are pushed down one place and a logic 1 put on the top.
4. Push and Copy top of stack. Data is moved down the stack and the previous top of stack (now the next position down) is copied to the top.
5. Pop the stack. All data values are moved up the stack one place. The old top of stack is lost.

Category (b) — logical operations (See Fig. 6):
There are two types here, a logical function (AND, OR, EXOR. COMP) and the function followed by PUSH:

1. AND, OR EXOR, COMP. The top two elements of the stack are propped into the logic unit, the logical function is performed on them, and the result pushed back onto the stack.
2. AND-PUSH, etc. The top two values on the stack are popped into the logic unit, the appropriate function is performed on them, the result is pushed onto the stack, and this is followed by a logical 1. This form of logical operation is used when the result is to be saved in the stack for subsequent processing. The 1 is put onto the stack to make it ready for further evaluations

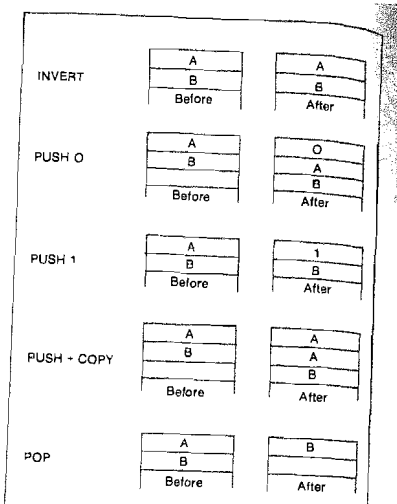


Fig. 5 STACK MANIPULATION

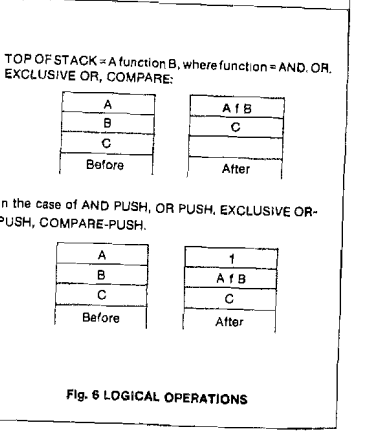


Fig. 6 LOGICAL OPERATIONS

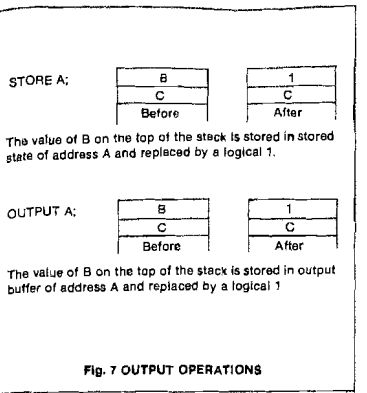


Fig. 7 OUTPUT OPERATIONS

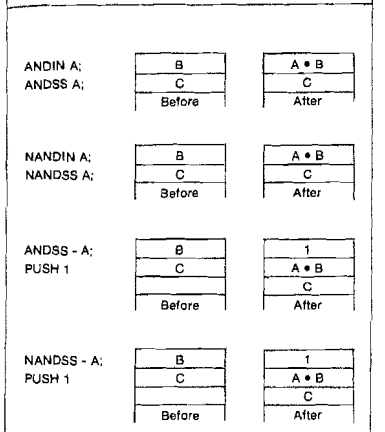


Fig. 8 INPUT OPERTIONS

Category (c) — input/output operations (See Figs. 7 and 8): These instructions have two parts, the command and the address. The command defines the data path (input-stack, stored state-stack, stack-stored state or stack-output) and the logical operation to be performed, if any. The address defines which of the 30 pieces of data is to be manipulated

STORE and OUTPUT take the logic value from the top of the stack and transfer it to the appropriate stored state or output buffer, the top of the stack being replaced by a logical 1 ready for the next evaluation

ANDIN takes the value of the addressed input end ANDs it with the top of the stack.

NANDIN takes the logical inverse of the addressed inputs and ANDs it with the top of the stack.

ANDSS takes the value of the addressed stored state and ANDs it with the top of the stack.

NANDSS takes the logical inverse of the addressed stored state and ANDs it with the top of the stack.

In the above four operations, the stack is neither pushed nor popped

ASP1 takes the value of the addressed stored state, ANDs it with the top of the stack, and pushes 1 onto the stack.

NASP1 takes the logical inverse of the addressed stored state, ANDs it with the top of the stack, and pushes 1 onto the stack

Category (d) — control:

PAGE. There are typically 4 pages of stored states in the SBA, and the instructions reading and writing to and from the stored states only provide an address within the currently enabled page. The PAGE instruction steps the page counter and enables the next page.

HOME. If it is required to enable a page of stored states that has been passed, the HOME instruction causes the page counter to go back to enable the home page.

As an example, if the pege counter is currently enabling page 3 and it is required to update a stored state on page 4, the PAGE instruction would be used. If now a stored state on page 2 is required, a HOME instruction will switch back to page 1 and a PAGE instruction will step to page 2

RESTART. This code is always the last code in the program memory (note that its value is conveniently all zeros) and when seen by the control logic the following is performed:

1. the contents of the output buffers are relatched to the outputs.
2. a new set of inputs are latched
3. the top of the stack is set to logical 1
4. the page counter is reset to the home page
5. the program address counter is reset to restart the evaluation of Boolean equations.

PART II Using the SBA

A. INPUT/OUTPUTS

The addressing capability of the SBA allows for 30 inputs and 30 outputs. There are 30 pins available as Input/Outputs and so if more than 30 total inputs and outputs are used they must be multiplexed.

There is a mask programmable option on each of the 30 pins to allow them to be inputs, outputs or multiplexed input/outputs. Regardless of the option, the internal addressing of the pins remains the same and so, for example, if an application requres only one input and the board layout requires it to be the last pin the program must use address 30.

Input

When programmed as an INPUT, nothing will be able to be output from the pin even if the program loads something in the respective output buffer.

Output

When programmed as an OUTPUT, the input data path is still connected and the value on the pin will be latched with all the other inputs at the appropriate time. This fact can be utilized as follows:

(a) It is sometimes required that the value of an output is used in the processing during the following cycle and would normally have to be copied into a Stored State. Feeding an output back as an input in this way avoids this problem and can also be used as a limited supply of extra stored states, if spare pins are available, that can also be read outside the chip.

(b) As well as reading the value of the output directly, the output can be modified by making use of the open drain construction of the output driver. The value of the output can be modified by an externally connected active pull-down device and the result read into the input. Something like a manual override would be a simple use of this facility while more complex logic functions can also be easily performed.

Multiplexed Input/Output

For complete separation of inputs and outputs the MULTIPLEXED facility must be used although external logic must be used for demultiplexing.

Output Drive Capability

The Output drivers have an impedance of 100 Ohms and are nominally rated at a sink current of 7mA. Thus each output can drive 4 TTL loads plus a 10 KOhm pull-up resistor to +5V.

The nominal current rating is determined by the total allowable power dissipation in the output circuits, which is a maximum of 150mW. The 7mA rating has been determined assuming all 30 outputs are being used. If less than the maximum are in use, the current rating for each can be increased up to the maximum rating of 20mA, keeping within the 150mW power restriction. Fig. 9 gives a guide to the current capacity for different numbers of outputs in use.

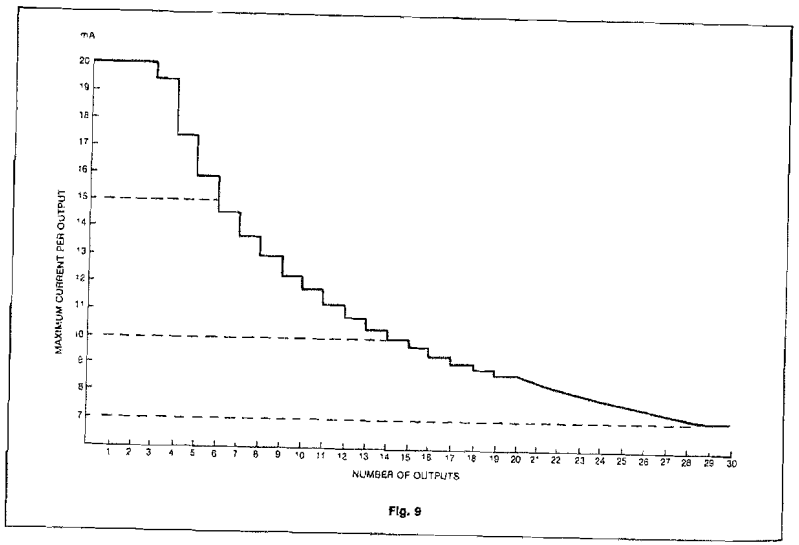


Fig. 9

B. DEVICE TIMING

The clock can be generated internally with the help of an external R/C network connected to the three 'clock' pins, or an external clock can be applied to the clock input.

The SBA will perform the instructions in the ROM, one per clock cycle, until the RESTART instruction is reached. At this point a special sequence is performed that is shown in Fig. 10.

The possible variations are due to separate or multiplexed inputs/outputs and the use of HALTED and GO.

Input Timing

Inputs are strobed into the device once per program cycle, as shown in Fig. 10, whether they are exclusive inputs or multiplexed.

Output Timing

If a pin is dedicated to the output function, then the logic level remains constant throughout the program and is updated at the end of each cycle as shown in Fig. 10.

In a multiplexed I/O the output data is present for two clock cycles at the end of each program cycle, the I/O control providing a strobe so the data can be stored in an external device (on the negative edge).

Modes of Operation

1. If the SBA is required to cycle continuously the GO input will be true. In this case there will be one clock cycle between I/O control disappearing and the SPA strobing the inputs. This is the more common mode of operation.

2. If GO is not present after the I/O control goes high, the HALTED output will appear and the SBA will stop. When GO becomes true, HALTED will be removed and the SBA will continue by latching a new set of inputs. Although this mode can be useful it is usually better to put the control into the program itself and run continuously.

Cycle Times

Since all instructions have been arranged to take the same time, the total time taken for a complete program cycle is the time for 1 clock cycle multiplied by the total number of instructions in the program (including RESTART) plus 8 (for the end of cycle sequence). If the cycle is stopped by removing GO, the time can be up to 1 clock cycle less. Thus the maximum possible cycle time is:

Clock period x (1023 + 6) = 1.28625ms at 800KHz
= 10.29ms at 100KHz

In general we have:

$$\frac{\text{no. of instructions} + 6}{\text{clock frequency in KHz}} = \text{program cycle time in ms}$$

C. BASIC PROGRAMMING

The internal operation of the SBA is of no concern to the user, the device simply being thought of as a variable array of logic. It can be treated as abstract logic or as the logic family most familiar to the engineer, although speed and response time must be considered separately as it is somewhat unique in the SBA.

The logic representing the function to be performed by the SBA is described by a set of Boolean Equations. These can be of any length and are composed of the four logical functions, AND, OR, EXCLUSIVE OR and COMPARE, together with invert or negate and as many levels of brackets as are required. Rules and restrictions are minimal.

Stored States — Basic Storage

The Stored States can be used to store the state of some input or logical combinations from one program cycle to the next. For example, if it were required to produce an output whenever an input changed state, the value of the input must be stored and compared with the new input in the next cycle. The equations might be:

output = input * store; (where * represents exclusive OR)
store = input;

Thus, when the input is different from the stored value, i.e. the state of the input last time, the output is produced.

It should be noted here that because of the sequential nature of the SBA the equations are performed one at a time. So the 'store' equation must come after the 'output' equation otherwise the

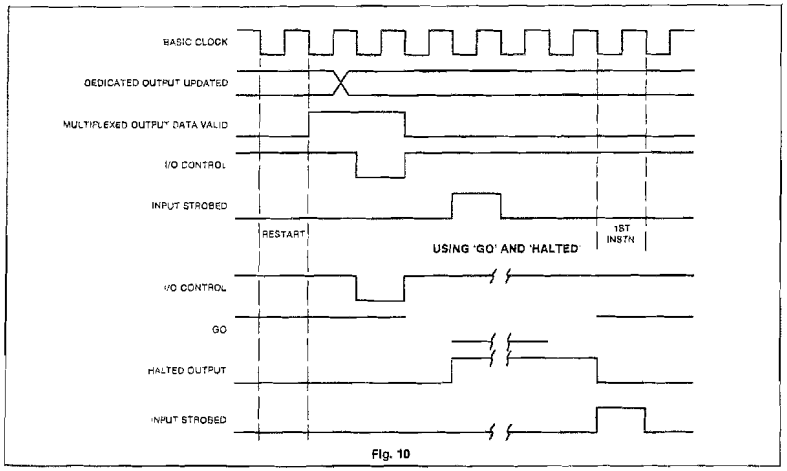


Fig. 10

store would contain the same value as the input of the current program cycle.

The Stored States can also be considered in groups for storing numbers, machine states, etc., and also for counters and sequence generators. Again the equations can either be generated purely logically from a truth table of the required sequence or by considering an appropriate hardwre solution.

Stored State — Temporary Storage

Stored States do not necessarily have to be used as stores from one cycle to the next. It is often convenient to use these as temporary stores within a program cycle. A typical example is when a calculated value is to be used in several equations. Rather than calculate the value each time, it can be calculated once and stored and then read directly from the store as required. Such 'temporary stores' may be updated as many times as required in a program cycle and it is often convenient to reserve a couple of stored states on each page for this purpose. An example might be the Stored State 'temp' being used as a reset for a store and then later as an enable for an output.

```
temp = reset logic;
store A = (store A logic).-temp;
store B = (store B logic).-temp;
etc., then later in the program
temp = enable logic;
output A = (output A logic).temp;
output B = (output B logic).temp;
etc.
```

If the SBA compiler is used, the name for the temporary store must be the same (as 'temp' above) to define the same bit and it can be seen that there might be confusion in knowing the function of the store in a particular part of the program. The problem can be solved by knowing that SBACOMP only takes the first 4 characters of the name. So as long as these remain constant, the same bit of storage will be used and the name can be extended to indicate the current use of that particular store. In the above example the names could have been 'tempreset' and 'tempenable'.

Order of Equations

The most important rule in SBA programming has already been mentioned and that is the order of the equations. While the timing as seen external to the device is clearly defined, it must always be remembered that the equations within a program cycle are performed in sequence and care must be taken to ensure that stores are updated at the right time.

The first example illustrates the overall construction of a program and is demonstrated by considering the store defining the current state of the machine. The state will be output to the system being controlled and the inputs read back from the system. These, together with the present state, will define the next state to be output to the system. When the state number is used in the SBA equations, the position of that equation in relation to the equations updating the state will obviously define which state is being referred to. The state number before updating will refer to the state output to the system last time and will therefore be associated with the current inputs since these are a direct result of that state. The state number after updating will refer to the next state and will be used in determining the outputs.

Another important time to watch the updating of stores is when using such things as counters. A 3 bit binary counter stepped by 'step' might be written:

```
A = A*step;
B = B*(step.A);
C = C*(step.A.B);
```

where the least significant bit changes whenever 'step' is true and the subsequent bits only when all previous bits are true AND 'step' is true. It can be seen that the equations cannot be written as shown because the values on the right hand side refer to the present value of the counter and those on the left hand side the next value. After the first equation, A has been updated and so in the next equation the wrong value will be read. (Note that a hardware solution would update all bits in parallel.) In this case the stack can be utilized to advantage by storing the new values as they are calculated and only when all bits are completed are the stored states updated from the stack. The example would actually be written:

```
stak = A*step;
stak = B*(step.A);
stak = C*(step.A.B);
C = save.
B = save;
A = save,
```

Equations 3 and 4 can be combined but, if written like this for clarity, they will, in fact, be combined by the compiler.

The Pages of Stored States

The order of equations and the variables within the equations can also be important (as far as economy of instructions are concerned) when the different pages of Stored States are used. Equations using variables from more than one page can, in extreme circumstances, use more page change instructions than actual processing!

For this reason, those bits commonly used together (e.g. counters) should be grouped on a single page. It is better to leave a page partly unused in order to do this. Thus four 15 bit counters would certainly be better put one counter per page with the odd associated bits (like resets) kept on their respective pages, rather than squeezing onto two pages and having to put resets etc., on a different page.

If possible, processing should be performed in the order of pages. Thus page 1 processing would be done first, then page 2 and so on to avoid unnecessary page changes. It is easiest to write the program first and then allocate the stores to pages to get the flow right. Data transferring from one page to another can often be stacked first as demonstrated in the following.

Bits on page 1 labelled 1A, 1B, 1C to be moved to page 2, bits labelled 2A, 2B, 2C, and if written:

```
2A = 1A;
2B = 1B,
2C = 1C;
```

will use 11 instructions while:

```
stak = 1A:
stak = 1B;
stak = 1C,
2C = save;
2B = save;
2A = save;
```

uses only 9. If the pages were 1 and 4, the number of instructions would be 17 and 11, if moving page 3 to page 2 we would have 14 against 10. Obsessive page instruction saving is, however, not usually required and is only important when using the ROM to its maximum capacity. It is generally best to write the equations initially using the simple basic rules and to resort to more clever reduction techniques if the ROM is filled.

D. PROGRAMMING EXAMPLES

Combinational Logic

Little needs to be said here since any boolean equations is valid and can include AND, OR, EXOR, COMPARE and INVERT operators and as many variables and brackets as are required.

For greatest economy of instructions the equation should be minimized as far as possible, using EXOR and COMP if appropriate, and in general sums of minterms are most efficient.

If required, even further reductions can be made by considering the instruction set. Inversion of single terms costs nothing, while inversions of multiple terms costs one instruction. The AND operator with a single term is implicit with the reading function, while all other operators and the AND with a multiple term all cost an extra instruction.

A good rule is to use as few OR, EXOR and COMP operators as possible (also AND and INVERT outside brackets). The difference in the number of instructions taken by two versions of the same equations is approximately the difference in the numbers of these 'bad' operators (shown underlined).

Examples:

(a) -A.-B ± -C.-D ± -E.-F instead of (A ± B).(C ± D).(E ± F) saves 3 (2 versus 5)

(b) -(-A.-B.-C.-D) instead of A ± B ± C ± D saves 2

Latches

The straightforward storing, temporarily or otherwise, of input data or logical combinations has been discussed and needs no further comment.

However, it is often required that a piece of data be latched into a store, and in hardware solutions devices such as S-R, J-K and D type latches are available for this function. The stored states in the SBA together with a bit of logic can be made to act as latches, the type being limited only by the imagination. A few examples are as follows:

(a) Simple S-R latch that is set by the variable 'set' and reset by 'reset': Q = set + Q.-reset

(b) In (a) the 'set' will override if both inputs appear together. If 'reset' is to override Q = (set + Q).-reset

(c) Clocked latches have greater variety, a simple D type being: Q = data.clock + -clock.Q

(d) A clocked set - reset:
Q = (set.clock) + Q.-(reset.clock)

(e) Clocked set, asynchronous reset, set override.
Q = (set.clock) + Q.-reset

(f) Clocked set, asynchronous overriding reset:
Q = ((set.clock) + Q).-reset

(g) Full J-K latches
Q = J.clock.-Q + Q.-(K.clock)

It is usually best to design the latch to fit the particular requirement since, in general, the more features required the more instructions are needed. If a latch is required to change on a particular edge of a clock, another store is required and we have, for example:

```
clock = inclock.-storaclock,
storeclock = inclock;
```

to detect the 0-1 transition. Either or both edges can be detected in this way. It can be noted here that once an input clock has been monitored for a transition then anything in the whole of that program cycle can be clocked by the same edge.

Counters and Sequence Generators

There are several ways in which counters can be programmed, but a good general purpose method is described here.

The counter will have an input to tell it when to count and let this be called COUNT.

Consider each bit of the counter in turn, from the least to most significant bits, and determine the conditions that require that bit to change. This condition, ANDed with COUNT, can be made to change the bit using the exclusive OR instruction. So for the Rth bit, if the change condition is CR we have:

```
R = R*(COUNT.CR);
```

Care must, of course, be taken to ensure that bits are not used after they have been updated. They can be stored conveniently on the stack. In a binary counter each bit changes when all bits of lower significance are true, and we have, for a 4 bit counter as an example.

```
stak = A*COUNT;
stak = B*(COUNT.A);
stak = C*(COUNT.A.B),
stack = D*(COUNT.A.B.C);
D = save:
C = save;
B = save;
A = save;
```

If the counter is to step each program cycle (for a switch scanner or a counter using the cycle for its timing, for example), COUNT can be removed and the first equation changed to stak = -A;

The binary case is very regular and an alternative approach, which is more economical for large (over 4 bits) counters, uses temporary stores to build up the change conditions progressively:

```
T1 = COUNT.A
A = A*COUNT
T2 = T1.B
B = B*T1
T1 = T2.C
C = C*T2
T2 = T1.D
D = D*T1
etc.
```

Note that this time stacking has been avoided since the change condition is built up progressively. It can also be seen that only two temporary stores are required.

The technique is further illustrated by considering the following 'random' sequence:

State	DCBA
1	0000
2	0111
3	1110
4	0001
5	1011
6	0011
7	0100
8	1001
9	0000;

Examining each bit we see that:

A changes after states 1, 2, 3, 6, 7, 8
B changes after states 1, 3, 4, 6
C changes after states 1, 3, 6, 7
D changes after states 2, 3, 4, 5, 7, 8

Assuming the non-valid states cannot occur, and using standard reduction techniques, the change conditions reduce to:

```
CA = -A + B.-D + -B.D
CB = -C.-D + C.D
CC = -A + B.-C.-D
CD = C + D + A.-B
```

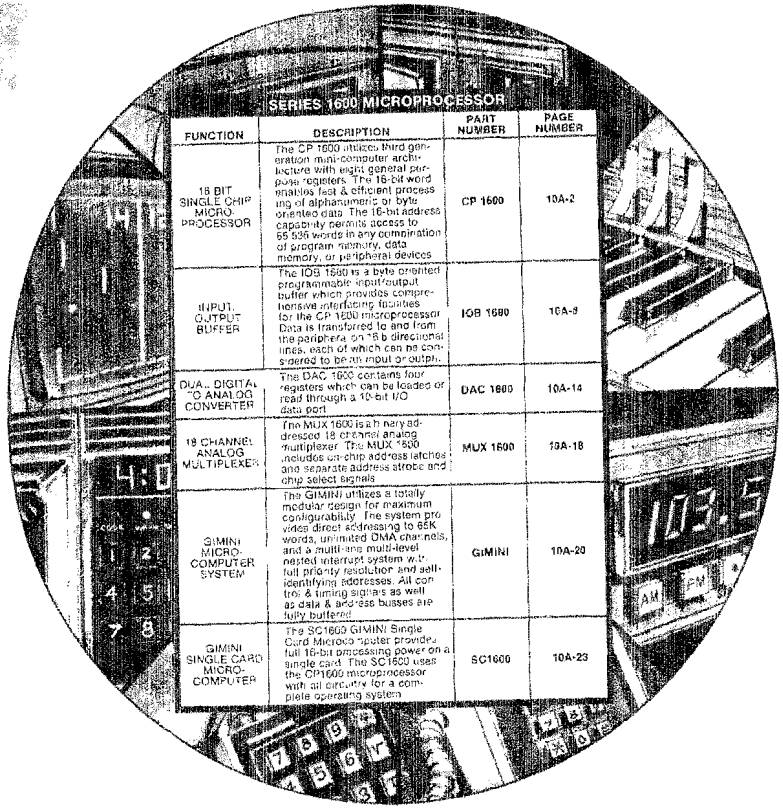
Now including STEP, and reducing still further for the SBA using exclusive OR(*) and compare (#), we have finally

```
stak = A * STEP.(-A + (B*D)),
stak = B * STEP.(C#D),
stak = C * STEP.(-A + B.-C -C).
stak = D* STEP (C + D + A.-B);
D = save,
C = save;
B = save,
A = save;
```

And, for completeness, the carry output is given by A.-B -C.D, reducing to

```
COUT = -B.D;
```

which should go at the beginning, before the states are updated.



SERIES 1600 MICROPROCESSOR

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
16 BIT SINGLE CHIP MICRO-PROCESSOR	The CP 1600 utilizes third generation mini-computer architecture with eight general purpose registers. The 16-bit word enables fast & efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices.	CP 1600	10A-2
INPUT, OUTPUT BUFFER	The IOB 1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the CP 1600 microprocessor. Data is transferred to and from the peripheral on 16 bi directional lines, each of which can be considered to be an input or output.	IOB 1680	10A-9
DUAL DIGITAL TO ANALOG CONVERTER	The DAC 1600 contains four registers which can be loaded or read through a 16-bit I/O data port.	DAC 1600	10A-14
16 CHANNEL ANALOG MULTIPLEXER	The MUX 1600 is a binary addressed 16 channel analog multiplexer. The MUX 1600 includes on-chip address latches and separate address strobe and chip select signals.	MUX 1600	10A-18
GIMINI MICRO-COMPUTER SYSTEM	The GIMINI utilizes a totally modular design for maximum configurability. The system provides direct addressing to 65K words, unlimited DMA channels, and a multi-line multi-level nested interrupt system with full priority resolution and self-identifying addresses. All control & timing signals as well as data & address busses are fully buffered.	GIMINI	10A-20
GIMINI SINGLE CARD MICRO-COMPUTER	The SC1600 GIMINI Single Card Microcomputer provides full 16-bit processing power on a single card. The SC1600 uses the CP1600 microprocessor with all circuitry for a complete operating system.	SC1600	10A-23

10A

SERIES 1600 MICROPROCESSOR

MICRO ELECTRONICS

16-Bit Single-Chip Microprocessor

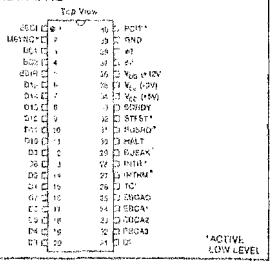
FEATURES

- 8 program accessible 16-bit general purpose registers
- 67 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit 2's complement arithmetic & logic
- Status word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64k memory using single address
- TTL compatible/simple bus structure
- 600ns cycle time 3.3 MHz 2-phase clock

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



*ACTIVE LOW LEVEL

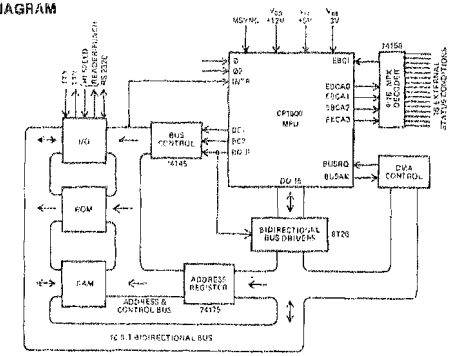
DESCRIPTION

The CP1600 Microprocessor is a compatible member of the Series 1600 Microprocessor products family. The CP1600 is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with General Instrument's N-Channel Ion-Implant GIANT II process, insuring high performance with proven reliability and production history. All members of the Series 1600 family, including Programmable Interface Controllers, Read Only Memories and Random Access Read/Write Memories are fully compatible with the CP1600.

The CP1600 Microprocessor has been designed for high speed data processing and real time applications. Using a 3.3MHz two phase clock, the CP1600 completes a microcycle in 600 nanoseconds. Typical applications include programmable calculator systems,peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications. The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard, cassette tape, floppy disk, and RS-232C data communication lines.

The CP1600 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alpha-numeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set and microprogrammable Peripheral Interface devices, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1600 SYSTEM DIAGRAM



PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROLS

STPST
Input
STop-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

MSYNC
Input
Master SYNC: Active low input synchronizes the microprocessor to the ϕ1, ϕ2 clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL SIGNALS

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

BUSRQ*
Input

BUSAK*
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

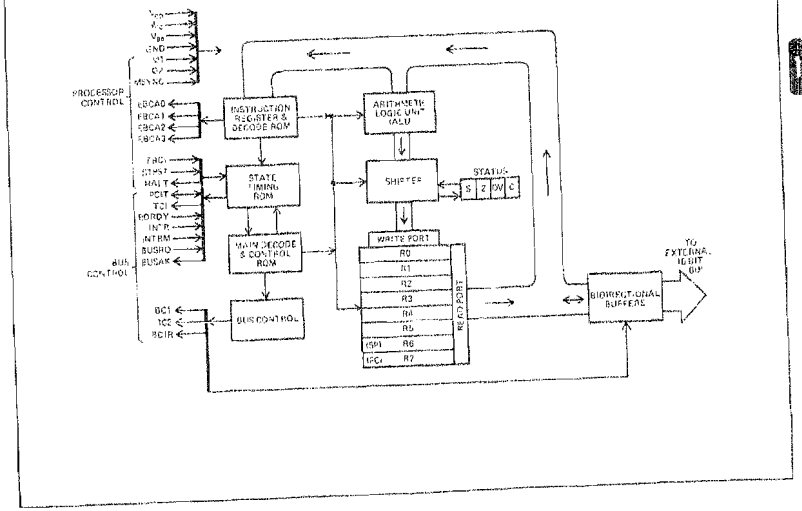
BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

INTR*, INTRM*
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

TCI
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.

PCIT
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1600 INTERNAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other input/output voltages with respect to V_{BB} ..... −0.3V to +16.0V
Storage Temperature ..... −55°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause *permanent damage to these devices*. Functional operation at these conditions is not implied—operating conditions are *specified below*

Standard Conditions: (unless otherwise noted)

V_{DD}=+12V±5%, 70mA(typ) , 110mA(max.) V_{BB} = −3V±10%, 0.2mA(typ) , 2mA(max.)
V_{CC}=+5V±5%, 12mA(typ) , 25mA(max.) Operating Temperature (T_A)=0°C to +70°C

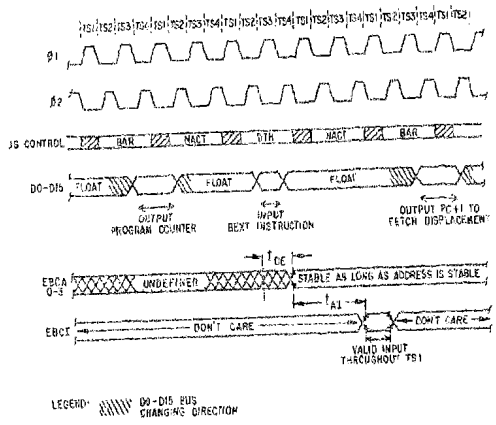
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	$V_{\phi H}$	10.4		V_{DD}	V	
Low	$V_{\phi L}$	0	--	0.6	V	
Logic Inputs						
Low	V_{IL}	0	--	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	--	V_{CC}	V	
High (Bus Data Ready Line See Note 1)	V_{IHR}	3.0	-	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}		V	I_{OH} = 100μA
Low (Data Bus Lines D0-D15)	V_{OL}	--	--	0.5	V	I_{OL} = 1.8mA
Low (Bus Control Lines BC1,BC2,BDIR)	V_{OL}	--	--	0.45	V	I_{OL} = 2.0mA
Low (All Others)	V_{OL}	-	--	0.45	V	I_{OL} = 1.8mA
AC CHARACTERISTICS						
Clock Pulse Inputs, φ1 or φ2						
Pulse Width	$t_{\phi 2}$, $t_{\phi 2}$	120	--	--	ns	
Skew (φ1, φ2 delay)	t_{12}, t_{21}	0	--	--	ns	
Clock Period	t_{CY}	0.3	-	2.0	us	
Rise & Fall Times	tr, tf	--	--	15	ns	
Master SYNC:						
Delay from φ	tms	--	-	30	ns	
D0-D15 Bus Signals						
Output delay from φ1 (float to output)	t_{BC}	-	-	120	ns	1 TTL Load & 25 pF
Output delay from φ2 (output to float)	t_{BF}	--	60	-	ns	
Input setup time before φ1	t_{B1}	0	-	--	ns	
Input hold time after φ*	t_{B2}	10	--	--	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from φ1	t_{DC}	-	-	120	ns	
BUSAK Output delay from φ1	t_{BD}	--	150	-	ns	
TCI Output delay from φ1	t_{TD}	--	200	-	ns	
TCI Pulse Width	t_{TW}	--	300	-	ns	
EBCA output delay from BEXT input	t_{DE}	--	-	150	ns	
EBCA wait time for EBCI input	t_{AI}	--	-	400	ns	
CAPACITANCE						TA = +25°C, V_{DD} = +12V; V_{CC} = +5V, V_{BB} = −3V f φ1 = φ2 = 120ns
φ1, φ2 Clock Input capacitance	Cφ1, Cφ2	--	20	30	pF	
Input Capacitance						
D0-D15	CIN	--	6	12	pF	
All Other	--	--	5	10	pF	
Output Capacitance						
D0-D15 in high impedance state	C_L	--	6	15	pF	

**Typical values are at +25° C and nominal voltages

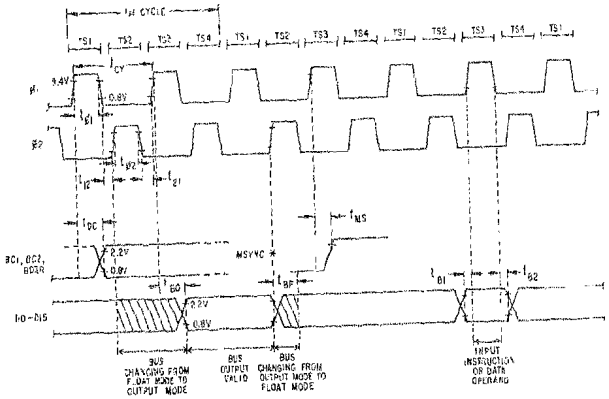
NOTE:

1. The Bus Data ReaDY(BDRDY) *line is sampled during time period* TS1 after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns *minimum*. BDRDY *may go high* asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration

BUS TIMING DIAGRAM



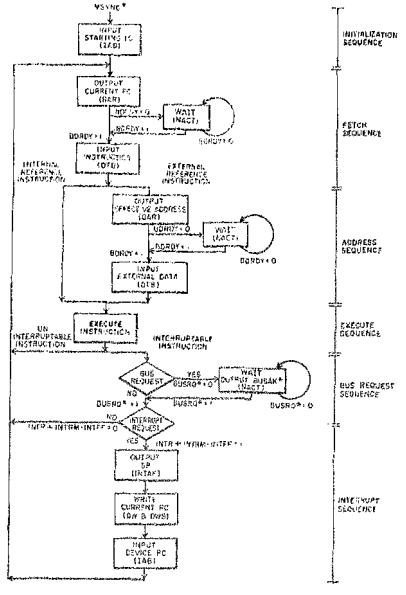
TYPICAL INSTRUCTION SEQUENCE



BRANCH ON EXTERNAL CONDITION INSTRUCTION

10A

SIMPLIFIED STATE FLOW DIAGRAM



BUS CONTROL SIGNALS

BDIR	BC1	BC2	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	0	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	1	DTB	Data to Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DWS	Data Write Strobe
1	1	0	DW	Data Write
1	1	1	INTAK	INTerrupt AcKnowledge

INSTRUCTION SET SUMMARY

		Mnemonics	Operation	Microcycles Dir.	Indr.	Imm.	Stack	Comments
External Reference Instructions	Arithmetic & Logic	ADD	ADD	10	8	8	11	Result not saved
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	
	I/O	MVO	MoVe In	10	8	8	11	
		MVI	MoVe In	10	8	8	11	
Internal Register Instructions	Register to Register	ADDR	ADD contents of Registers	6				Add one cycle if Register 6 or 7, except*. Result not saved
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		MOVR	MOVe Register	6				
	Single Register	CLRR	CLeaR Register	6				XORR with itself
		TSTR	TeST Register	6				
		JR	Jump to address in Register	7*				PC←(RRR)
		INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				Two Words
		SIN	Software INterrupt	6				Pulse to PCIT pin
		RSWD	Return Status WorD	6				
		PULR	PULl from stack to Register	11*				PULR=MVI @ R6
		PSHR	PuSH Register to stack	9*				PSHR=MVO @ R6
	Register Shift	SLL	Shift Logical Left	6				one or two position shift capability. Add two cycles for 2-position shift
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
		SWAP	SWAP 8-bit bytes	6				2-position=SWAP twice
Control Instructions		HLT	HaLT	4				Must precede external reference to double byte data
		SDBD	Set Double Byte Data	4				
		EIS	Enable Interrupt System	4				Not interruptible
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
Jump Instructions		J	Jump	12				Return Address saved in R4, 5 or 6
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable Interrupt	12				
Conditional Branch Instructions		B	unconditional Branch	7				Displacement in PC+1 PC←PC±Displacement Add 2 cycles if test condition is true.
		BC, BLGE	Branch on Carry, C=1	7				
		BNC, BLLT	Branch on No Carry, C=0	7				
		BOV	Branch on OVerflow, OV=1	7				
		BNOV	Branch on No OVerflow, OV=0	7				
		BPL	Branch on PLus, S=0	7				
		BMI	Branch on Minus, S=1	7				
		BZE, BEQ	Branch on ZEro or EQual	7				Z=1
		BNZE, BNEQ	Branch if Not ZEro or Not EQual	7				Z=0
		BLT	Branch if Less Than	7				SVOV=1
		BGE	Branch if Greater than or Equal	7				SVOV=0
		BLE	Branch if Less than or Equal	7				ZV(SVOV)=1
		BGT	Branch if Greater Than	7				ZV(SVOV)=0
		BUSC	Branch if Sign ≠ Carry	7				CVS=1
		BESC	Branch if Sign = Carry	7				CVS=0
		BEXT	Branch if External condition is True	7				4 LSB of Instruction are decoded to select 1 of 16 external conditions.

1 MICROCYCLE = 2 CLOCK CYCLES

10A

Input/Output Buffer

FEATURES

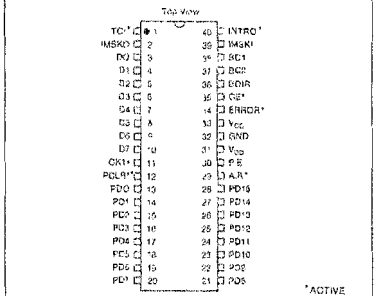
- Single 16-Bit Port or Dual 8-Bit Ports for Bidirectional Input/Output
- Parity Check Logic on Both Ports
- Three Levels of Priority Interrupt Logic
- 'Real Time' Presetable 16-Bit Timer
- Capability to Monitor Peripheral Error Status
- Three Interrupt Vectors for Error, I/O and Timer
- Automatic Handshake Logic and Signals
- Control Register
- TTL Compatible

DESCRIPTION

The IOB1680 is a byte oriented programmable input/output buffer which provides comprehensive interfacing facilities for the CP1600 microprocessor with a minimum of additional components. The circuit is fabricated in General Instrument N-Channel Ion Implant GIANT II process insuring high performance with proven reliability and production history

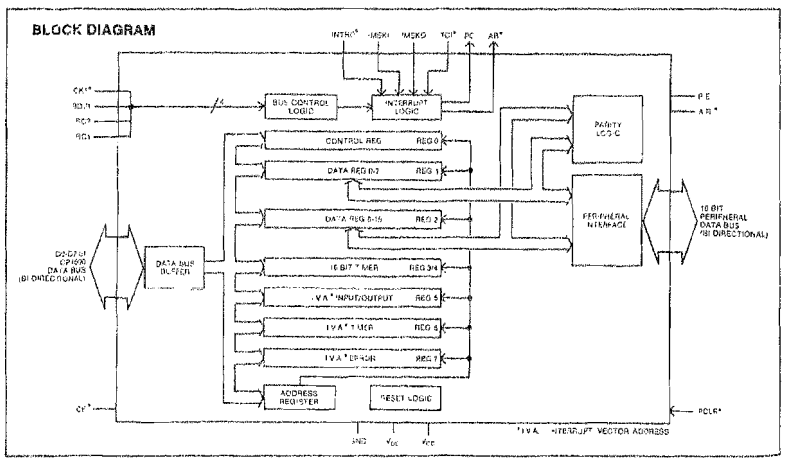
The IOB1680 enables efficient interfacing between a peripheral and the CP1600 by the use of six 8-bit registers and a 16-bit programmable timer. Two of the 8-bit registers are a buffer store between the CP1600 and the bidirectional I/O lines to peripheral, latching any data sent to them from the CP1600. Three other 8-bit registers hold the Interrupt Vector Addresses associated with I/O, Error Status and the Timer. The Control Register governs the operation and characteristics of the IOB1680 and provides a convenient means for the CP1600 to monitor I/O status information. The 16-bit timer gives the IOB1680 a real time capability which is suitable for confirming system security and for timing peripheral activities. These registers are initialized after power clear by the CP1600 program writing the required interrupt vector addresses into the appropriate registers. The interrupt vectors may also be altered at any time by program.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



*ACTIVE LOW LEVEL

BLOCK DIAGRAM



IOB1680/CP1600 SIGNALS

Data Bus:

D0-D7 (Input/Output/High Impedance)
DATA 0-7: The bidirectional data lines D0-D7 are used to transmit data and address information between the Series 1600 Microprocessors and the IOB1680. These correspond to the lower 8-bits of the Series 1600 Microprocessor's data bus. These data lines have tristate capability, being in the high impedance state except when transferring data or status information from the IOB1680 under control of the control bus signals BDIR, BC1 and BC2.

Bus Control Signals

BDIR, BC1, BC2 (Inputs)
Bus DIRection, Bus Control 1 and 2: Bus control signals from the CP1600 which define the state of data bus operations. These signals are decoded internally by the IOB1680 to control its operation

TCI* (Input)
Terminate Current Interrupt. A pulse output by the CP1600 in response to the TCI instruction to indicate the end of the current interrupt service routine.

INTRQ* (Output)
INTerrupt ReQuest: This output is pulled low to a logic '0' by the IOB1680 to request an Interrupt from the series 1600 Microprocessor. This is an open drain output capable of sinking 1.6mA with an output voltage 0.5V. Because of the open drain feature the INTRQ* output of several IOB1680s can be wired ORed together

CK1* (Input)
Clock 1: This clock defines when the bus control signals BDIR BC1 and BC2 are valid and is used in the IOB1680 to strobe their decode signals. It is also used to increment the timer.

CE* (Input)
Chip Enable: This low true address input enables the IOB1680 for data read and write operations.

IMSKI/MSK0 (Input/Output)
Interrupt MaSK In, Interrupt MaSK Out: These two signals are used to form the interrupt priority daisy chain and prevent a lower priority device from requesting an interrupt while a higher device is being serviced. The IMSKI input of the IOB1680 which is to have highest priority must be connected to GND

IOB1680 PERIPHERAL SIGNALS

Data

PD0-PD15 (Input/Output)
Peripheral Data 0-15: Communication of data to and from the peripheral device is via this 16 bit highway. Each output can sink 1.6mA for an output voltage of 0.5V. In the high state each output can source 100µA. These lines can be used as wire ORed inputs by 'pulling down' the line to a logic '0' sinking the 100µA externally.

Peripheral Control Signals:

PE (Output)
Peripheral Enable: This output is a function of the Ready bit of the control register. When it is at a logic '0' no action is required by the peripheral, a '1' indicates that peripheral activity has been requested by the CP1600

AR* (Input)
Attention Request: This input from the peripheral device is normally high at a logic '1' and is taken low to a logic '0' by the peripheral to request attention. This edge triggers the Ready bit of the control register pulling it to a logic '0', causing an interrupt request to be made via the INTRQ* output if the peripheral interrupt enable bit of the control register is set. If the interrupt is disabled the Ready bit of the control register can be used in 'polling' handshake routines.

ERROR* (Input)
ERROR: The error status of the peripheral is indicated by this input, being low indicating an error condition, e.g. tape low

PCLR* (Input)
Power CLeaR: Initializes registers

INTERNAL CONTROL SIGNALS

Control Register:
The Control Register can be written and read under program control. The function of the individual bits are

Bit 7—Parity Status for Peripheral Data 0-7:
The parity of the low order byte of the Peripheral Data bus is indicated by this Control bit, a logic '0' indicates even parity while a '1' indicates odd.

Bit 6—Parity Status for Peripheral Data 8-15:
Similar to bit 7, but indicates the parity of the high order byte of Peripheral Data.

Bit 5—Timer Clock Enable (TCE)
The clock to the 16-bit timer is controlled via TCE, the clock is enabled by setting TCE to a logic '1'. The timer can only request an interrupt when its clock is enabled by TCE

Bit 4—Timer Interrupt Enable (TIE)
For the timer to cause an interrupt request on the INTRQ* output TIE must be set to a logic '1', a '0' disables the timer interrupt logic

Bit 3—Peripheral Interrupt Enable (PIE):
PIE must be set to a logic '1' to enable interrupt requests on the INTRQ* output as a result of peripheral Attention Request or Error Status conditions.

Bit 2—Data Width Select (DWSL):
The re-enabling of the peripheral by automatic handshake can be chosen to occur with 8 or 16-bits wide data; DWSL being an '0' indicates an 8-bit wide data word while a '1' indicates a sixteen bit wide data word.

Bit 1—Error Summary
The ERROR STATUS of the peripheral is indicated by this bit of the Control Register, being a logic '0' shows an error condition. This will cause an interrupt request on the INTRQ* output if PIE is set to a '1'

Bit 0—Ready
This READY bit indicates the operational status of the peripheral. When it is a logic '0' the peripheral is active while a logic '1' indicates that the peripheral is idle and requiring service. The AR* input going low indicates to the Ready bit the end of a peripheral activity and thereby causes the Ready bit to be set. In this condition, if the PIE bit is set, an interrupt request results via the INTRQ* output. Reading or writing to the Peripheral Data lines causes the resetting of this Ready bit re-enabling the peripheral activity.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{CC} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

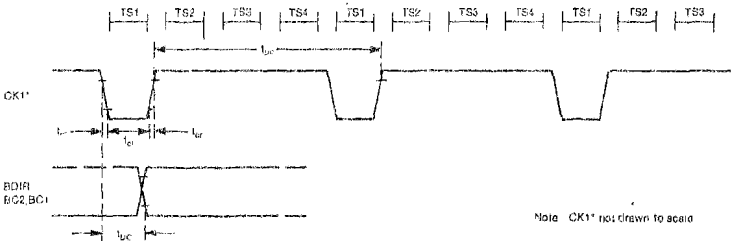
Standard Conditions (unless otherwise noted)

All voltages referenced to GND
V_{DD} = +12V ± 5%
V_{CC} = +5V ± 5%
Operating Temperature (T_A) = 0°C to +70°C

Characteristic		Symbol	Min	Typ**	Max	Unit	Condition
DC CHARACTERISTICS							
Clock Input:	High	V_{ihc}	2.4	—	V_{DD}	V	
	Low	V_{ilc}	0	—	.5	V	
Logic Inputs:	High	V_{ih}	2.4	—	V_{CC}	V	
	Low	V_{il}	0	—	.65	V	
Logic Outputs	High	V_{oh}	2.4	V_{CC}	—	V	I_{oh} = 100μA
	Low	V_{ol}	—	—	.5	V	I_{ol} = 1.6mA
AC CHARACTERISTICS							
Clock Inputs							
CK1* Clock period		tpc	0.4	—	4.0	μS	
Clock width		tcl	70	—	—	nS	
Rise & Fall times		tcr,tcf	—	—	10	nS	
CAPACITANCE (T_A = 25°C, V_{DD} = +12V, V_{CC} = +5V)							
Input Capacitance	D0-D7	C_{in}	—	6	12	pF	V_{in} = 0V
	All others		—	5	10	pF	V_{in} = 0V
Output Capacitance:		C_{out}	—	8	15	pF	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



CIRCUIT DESCRIPTION

This circuit is designed to provide all the data buffering and control functions required when interfacing the Series 1600 Microprocessor System to a simple peripheral device. Data is transferred to and from the peripheral on 16 bidirectional lines, each of which can be considered to be an input or output. The transfer of information with the CP1600 is accomplished via an 8-bit highway, the 16-bits being transferred as two 8-bit bytes, the register addresses are assigned CP1600 memory locations, as follows (N is an arbitrary starting address):

Register Address	Description
N	Control Register
N + 1	Data Register Low Order 8-bits
N + 2	Data Register High Order 8-bits
N + 3	Timer Low Order 8-bits
N + 4	Timer High Order 8-bits
N + 5	Peripheral Interrupt Address Vector
N + 6	Timer Interrupt Address Vector
N + 7	Error Interrupt Address Vector

8-Bit Data Registers

These two 8-bit registers are the buffer store between the CP1600 and the peripheral interface. These registers, when addressed, accept data from the CP1600 data bus during a Move Out (MVO) instruction to the peripheral lines on the IOB1680.

During a CP1600 Move In (MVI) instruction, the data present on the IOB1680 peripheral lines is transferred to the CP1600 data bus. If the registers have not been set to a '1' prior to the Move In instruction, the data read will be the wire OR of the peripheral data and that contained in the registers.

These two registers have consecutive word addresses N + 1 and N + 2. The high order byte is held in register N + 2.

16-Bit Binary Counter-Timer

This 16-bit down counter can be set under program control to give any count length up to 64K. Since only 8-bits are available to transfer data between the CP1600 and the IOB1680 the counter must be set as two 8-bit bytes, these bytes having word addresses N + 3 and N + 4. The clock for the timer is the Series 1600 Microprocessor System clock divided by 8. The clock input to the counter is enabled when the 'timer clock enable' bit of the control register is set to a '1', being disabled when this bit is reset to a '0'.

Everytime the count reaches zero the timer signals 'end of count' which will generate an interrupt request via the INTRQ* output of the IOB1680 if both the 'timer interrupt enable' and 'timer clock enable' bits of the control register are both set to a '1'. The clock to the timer is still enabled after this interrupt request has been made and remains so even after it has been serviced, assuming that the service routine did not disable it by resetting the TCE bit of the control register. After requesting an interrupt therefore the counter begins from a count of 64K, giving the IOB1680 a 'Real Time' Clock capability.

The timer has the lowest priority on the IOB1650 daisy chain. The peripheral error summary has the highest priority.

When the timer is set under program control the 'end of count' logic is reset clearing any previously unserviced interrupt requests from the timer. The acknowledge flip flop and the control register are unaffected.

It is not possible to read the 'current' state of the timer as it is counting in 'real time' and therefore asynchronously with any program running on the CP1600. A typical operating sequence is:

1. Load two bytes of counter.
2. Set 'timer interrupt enable' and 'timer count enable' bits of Control Register.

If an interrupt is required only once after the preset count the service routing would reset the 'timer clock enable' bit of the Control register disabling the timer clock and interrupt capability. If, however, the interrupt was required on a 'regular real time' basis then the service routine would leave the 'timer interrupt enable' and 'timer clock enable' bits set.

8-Bit Interrupt Vector Address Registers

The start address of the interrupt service routines for the error status, peripheral and timer are held in these three registers. The 8-bit Interrupt Vector Addresses are written into these registers during system initialization. When an interrupt request (INTRQ*), generated from the IOB1680 is acknowledged by an INTAK from the CP1600, the subsequent IAB signal on the control bus causes the contents of the appropriate interrupt vector address register to be strobed onto the lower 8-bits of the CP1600 data bus. This data is used as the program counter start address of the interrupt service routine.

The word addresses of these registers are N – 5, N + 6 and N + 7. This corresponds to the peripheral, timer and error respectively.

Power Clear Status of Circuit

Reset logic sets the initial state of the chip upon application of Power Clear. In this condition the states of the on chip registers are:

(a) Data Registers.
These are set to a logic '1' so that the peripheral input/output interface is high at a logic '1', this allows the peripheral lines to be used as inputs without any setting up procedure.

(b) Timer.
This is set to its maximum count length of 64K, all bits set to a logic '1'.

(c) Interrupt Vector Address Registers
These registers have all their bits reset to a '0' by the power on reset logic.

Control Register

(i) Bit 0 - Ready. This bit is set to a logic '1' indicating that no activity is required by the peripheral.

(ii) Bit 1 - Error Summary. This is a hard wired input indicating the status of the peripheral and is unaffected by the power on reset logic.

(iii) Bit 2 - Data Width Select. This bit is reset to a logic '0', selecting the data width of the interface to be 8-bits.

(iv) Bit 3 - Peripheral Interrupt Enable
Bit 4 - Timer Interrupt Enable
Both bits 3 and 4 are reset to a '0' at power on, disabling interrupts from the peripheral, and the timer.

(v) Bit 5 - Timer Clock Enable. During power up this bit is reset to a logic '0' disabling the counter clock.

(vi) Bit 6 - Parity Data 8-15
Bit 7 - Parity Data 0-7
Both these bits will be at a logic '0' showing even parity as the data register bits are all set to a '1'. This assumes no inputs from the peripheral; if this is not so, these bits will settle to a state depending upon the wire OR condition of the data registers and the peripheral inputs.

Interrupt Logic

The interrupt priority of the peripheral error status, peripheral interface and the timer is established by a daisy chain. The peripheral error status has the highest priority and the timer the lowest.

If a number of IOB1680s are being used then they can be connected in a daisy chain using the signals IMSKI, IMSKO and TCI to define their priority. An interrupt request is made by the IOB1680 pulling down, to a logic '0', the INTRQ* output. This output is open drain enabling wire OR capability. The acknowledgement to this request is an INTAK signal via the Series 1600 Microprocessor control bus. Each IOB1680 decodes this signal which sets an acknowledge flip flop in the interface of the interrupting device, causing the IMSKO output of that device to go to a '0'. This propogates to all lower priority devices causing their IMSKI inputs to go to a '0', thus disabling their interrupt capability.

When an IAB is valid on the control bus only the highest priority interrupting device must strobe its Interrupt Vector Address onto the Data Bus. Thus the IMSKI input of a device controls its IAB decode. The IAB signal is only enabled on the IOB1680 which has its IMSKI input at a logic '0' and its acknowledge flip flop set.

If two devices interrupt simultaneously they will both be acknowledged by an INTAK since this is decoded on each chip. However, the IMSKO output of the higher priority device going to a '1' will force the IMSKI input of the lower priority device being set to a '1'. The IMSKI input of the lower priority device being set to a '1' disables the IAB decode of the control bus thereby resolving simultaneous interrupts.

The negative edge of the TCI signal from Series 1600 Microprocessor resets the interrupt logic of the highest priority device whose interrupt logic has been set by an interrupt request and acknowledged by an INTAK.

The IMSKI/IMSKO daisy chain has a propogation delay which allows a maximum of eight IOB1680s to be daisy chained in series.

The IMSKI input to the highest priority device should be connected to Gnd.

Control Logic

The CP1600 control bus signals BDIR, BC1, BC2 are decoded to perform the internal control functions required.

Parity Logic

The peripheral interface is constantly monitored and the parity of bits 0-7 and 8-15 checked. Depending on the parity of these two words, bits 6 and 7 of the control register are updated. These bits can be conveniently accessed by the CP1600 for use in branch instructions.

Branching on Parity

Bits 6 and 7 of the IOB1680 Control register contain the parity status of the upper and lower eight bits of the peripheral interface respectively. The positioning enables the standard branch instructions of the CP1600 to be conveniently utilized. A typical example is:

```
MVI CTRLRS  R;Fetch Control Register
RLC R2, 2
BC          ;Branch if lower eight bits have odd parity
BNC         ;Branch if lower eight bits have even parity
BOV         ;Branch if higher eight bits have odd parity
BNOV        ;Branch if higher eight bits have even parity
```

10A

The IOB1680 as an Output Device

The power clear reset logic of the IOB1680 sets the Ready bit of the Control Register to a '1' causing the Peripheral Enable/Ready* output to go to a '0', a condition that requires no activity from the peripheral. This power clear reset logic also disables the IOB1680's ability to request an interrupt on the status of the peripheral by resetting the Peripheral Interrupt Enable bit of the Control Register to a '0'.

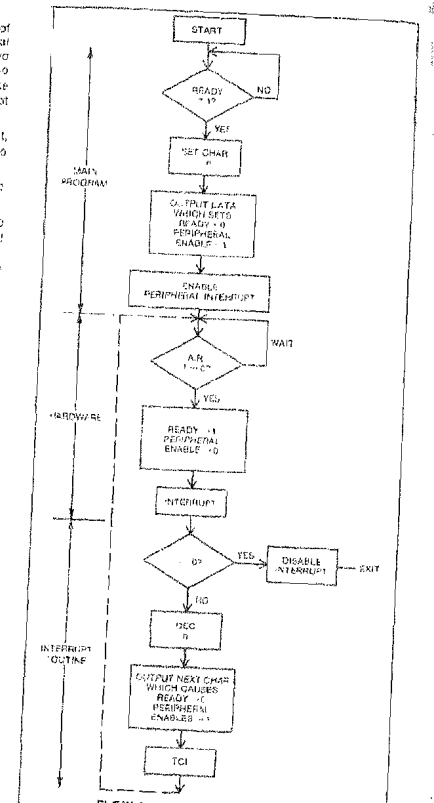
A flow chart for a typical output operation is shown to the right, the waveform diagram corresponding to this operation is also shown to the right.

The main program setting up the output operation would go through the following sequence of operations.

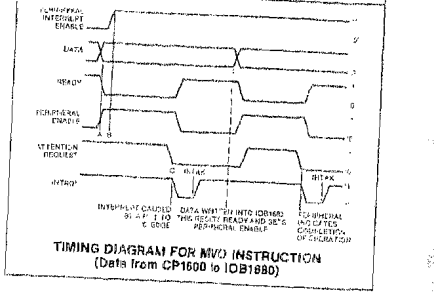
1. The Ready bit of the Control Register would be tested to ensure that the peripheral was indeed inactive. This would be so initially after power clear.
2. If condition (1) above is met, memory location CHAR of the CP1600 would be set to the number of output operations required. This is shown as 'SET CHAR = n'.
3. Send data from CP1600 to IOB1680 using MVO instruct. This operation resets the Ready bit to a '0' causing the Peripheral Enable/Ready* output to go to a '1', requesting an operation by the peripheral device. This is shown at A in the waveform diagram.
4. The Peripheral Interrupt Enable (PIE) bit of the Control Register is now set to a '1' by programmer allowing the IOB1680 to request interrupts from the CP1600 via the INTRQ* output. Enabling the PIE bit after sending the data to the peripheral ensures that no 'false' interrupts are generated.
5. After the data has been sent to the peripheral (3) above, the IOB1680 hardware monitors the status of the Attention Request input. A '1' to '0' edge on the input sets the Ready bit to a '1' and the Peripheral Enable/Ready* output to a '0', stopping the peripheral activity. The PIE bit and the Ready bit both being set to a '1' causes an interrupt request to be generated via the INTRQ* output, if no higher priority devices are interrupting. Refer to C in the waveform diagram.
6. When the CP1600 accepts the interrupt it starts the interrupt sequence by issuing the INTAK acknowledge signal which resets the INTRQ* output to its inactive state. The subsequent IAB signal causes the Interrupt Vector Address for the peripheral device to be strobed onto the data bus and then used as the start address for its service routine.

   Once entered, the service routine might go through the following sequence:
7. Decrement n, the number of output operations required (buffer length).
8. Test the resulting value n.
   (a) If it is zero the output operations are completed. Reset the PIE bit to disable the interrupt capability of the IOB1680 and EXIT.
   (b) If n is not zero output the next data to the IOB1680. This resets Ready to a '0' and Peripheral Interrupt Enable/Ready* to a '1' re-enabling the peripheral activity automatically.

   The peripheral acknowledges this operation by returning the Attention Request input to a '1', the timing of this signal is not too critical as the it edge triggers the Ready bit of the control register by a 1-0 transition.
9. The interrupt is terminated by TCI instruction which resets the acknowledge flip flop in the IOB1680 interface logic.



FLOW CHART FOR DATA OUTPUT



TIMING DIAGRAM FOR MVO INSTRUCTION
(Data from CP1600 to IOB1680)

The IOB1680 as an Input Device

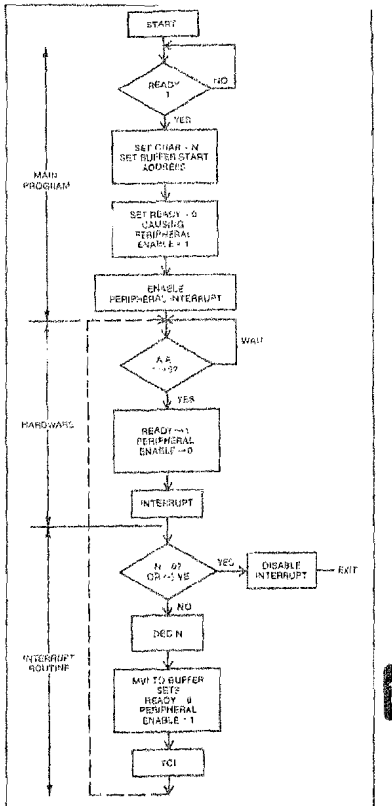
The power clear status of the IOB1680 for input is the same as for output which is described under the section 'The IOB1680 as an Output Device'.

A flow chart for a typical input operation and the corresponding waveform diagram is shown to the right.

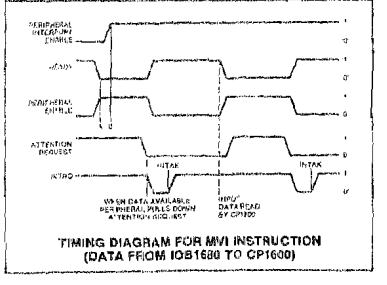
The main program setting up the input operation would probably go through the following sequence:

1. Test the Ready bit of the Control Register to ensure that the peripheral device is inactive. After power clear this will be its condition, i.e. set to '1'.
2. If condition (1) is true a CP1600 memory location will be set to contain the number of input operations required. Another memory location will be set to the input buffer start address. This is shown as 'SET CHAR = N, SET BUFFER START ADDRESS'.
3. The Ready bit of the Control Register should now be reset to a '0' by program. This causes the Peripheral Enable/Ready* output to go to a '1', requesting an operation from the peripheral device. On the waveform diagram, this is point A.
4. The Peripheral Interrupt Enable bit, PIE, of the Control Register is now set to a '1' by program. This allows the IOB1680 to request interrupts from the CP1600 via the INTRQ* output (see point B). Enabling the PIE bit after the Ready Bit ensures that initially no false interrupts are generated.
5. After the Ready bit has been reset by program, (3) above, hardware on the IOB1680 monitors the Attention Request input. A '1' to '0' edge on this input causes the Ready bit to be set to a '1' and the Peripheral Enable/Ready* output to go to a '0'. The change in state of the output stops the peripheral operation. As both the PIE bit and Ready bit of the Control Register are set an interrupt request will be generated via the INTRQ* output if no higher priority devices are interrupting.
6. When this interrupt is accepted by the CP1600 the acknowledge signal, INTAK, will reset the INTRQ* output to its inactive state. The subsequent IAB signal will cause the interrupt Vector Address associated with the peripheral to be strobed onto the data bus. This address will be used as the start address for the peripheral's interrupt service routine.

   A typical service routine for the peripheral could be:
7. Test value of N, the number of input operations required.
   (a) If it is zero all the required input operations have been completed. Reset the PIE bit of the Control Register to a '0' to disable the interrupt capability of the IOB1680 and EXIT.
   (b) If not zero increment the buffer address and decrement N.
8. Move data from the IOB1680 and CP1600 by a MVI instruction. This resets the Ready bit to a '0' and sets the Peripheral Enable/Ready* output to a '1' re-enabling the peripheral. The handshake from the peripheral in response to this action is to return the Attention Request input high to a '1'. This timing, however, is not too critical as the input edge triggers the Ready bit.
9. The interrupt is terminated by a TCI instruction which resets the acknowledge flip flop in the IOB1680 interface.



FLOW CHART FOR DATA INPUT



TIMING DIAGRAM FOR MVI INSTRUCTION
(DATA FROM IOB1680 TO CP1600)

Dual Digital to Analog Converter

DESCRIPTION

The DAC1600 Digital to Analog Converter has been designed to serve as a powerful, yet economic interface to a process control loop. The DAC1600 provides two 10-bit Pulse Width Modulated outputs and an array of switch inputs and light driver outputs. Essentially the DAC1600 contains four registers which can be loaded or read through a 10-bit I/O data port. Fig. 1 shows the data base information in these registers.

ANALOG OUTPUTS

The value of the analog outputs SP and VO are determined respectively by the ten-bit numbers loaded in the Set Point Register and the Valve Register. An output is a pulse train with a period of approximately 1KHz (1MHz/1024) whose high/low ratio is inversely related to the 10-bit value stored in the register. (See Fig. 2)

The high/low ratio is unaffected by temperature and supply variations and is the basis of the 10-bit D/A accuracy. The length of the high or low portions of the pulse will never be in error by more than a fraction of an LSB.

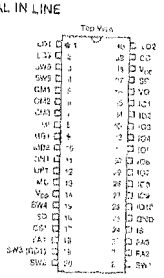
If the chip output (SP or VO) is passed through a low pass filter the result will be approximately equal to the desired analog voltage. However, it will not be accurate because , while the output ratio is accurate, the chip's output voltage levels are not, and would thereby degrade the accuracy of the signal. The chip's output should be used to drive a good switch which, in conjunction with a voltage reference and filtering will yield an analog voltage having 10-bit accuracy.

VALVE REGISTER (Manual Mode)

In addition to being a register, the Valve Register (B) is also an UP/DOWN counter. By setting MI (Manual Interrupt) to a "1" and either UP or DN to a "1", the B register will be slewed up or down. This allows an operator to manually adjust the B register value. The design allows bumpless, balanceless transfers between computer and manual control. In order to provide both a precise degree of manual control and an ability to slew the B register through a substantial change, a variable slewing rate has been incorporated in the chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



MODE REGISTER

The first five bits of Mode Register (A) may be used to store the mode of control. Manual Interrupt is in bit 1. Bits M2, M3, M4 and M5 can be read or loaded via the I/O bus or set by inputs from three switch inputs CM1, CM2, or CM3. The condition of these bits is encoded and output on light drivers MB1 and MB2. The Mode Register may be used to inform the operator of computer determined conditions or inform the computer of operator actions.

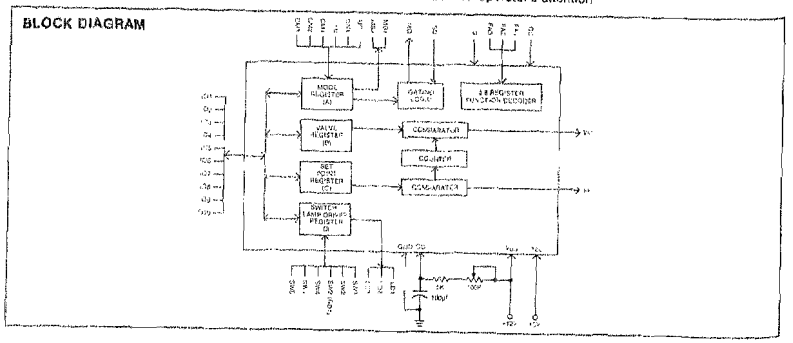
SWITCH/LAMP DRIVER REGISTER

The Switch/Lamp Driver Register contains three light drivers which can be used for panel alarm lights. It also stores six switch inputs.

ADDITIONAL ALARM FEATURE

Light driver M0 outputs a 2 cps signal which can flash a light to attract an operator's attention.

BLOCK DIAGRAM



PIN FUNCTIONS

IO1-10: 10 bit bidirectional data bus. Data can be loaded synchronously or asynchronously. Data are read onto the I/O bus without strobing.

MI: Manual input line. It forces the chip into a manual mode of operation.

CS*: Chip select line. It is low active for sychronous data transfer, high active for asychronous data transfer.

IS: Input strobe line. It loads one of the four internal registers defined by FA1-3, when CS* is low. If the chip is in the manual mode via MI, the ability to load one of the four registers,namely. the valve register, is unconditionally inhibited independent of the CS* signal.

FA1-3: Function select lines. It is used to specify one of the four registers and whether an input or output function is to be performed. See Table 2 for definition.

CM1-3: Control mode lines. A pulse on one of these lines will alter the bit M3, M4 or M5 in the mode register. See Table 3.

UP1, DN1, RD1: Up counting, down counting and reversing lines. They are used to control the direction of counting serially in the value register during the manual mode. Overflow or underflow of the register is prevented by internal circuitry. See Table 4 for definition.

SD: DAC1600 shed signal. It is used in conjunction with manual input line to form different manual mode outputs. See Table 5.

MO: DAC1600 manual mode output. It oscillates around 2Hz whenever MI is low and SD is high. See Table 5.

MB1, MB2: Mode bit-lines. They are used to indicate the status of the mode register. See Table 6.

VO: Valve register output. It is a 10 bit pulse width modulated waveform. See Fig. 2.

SP: Set point register output. It is a 10 bit pulse width modulated waveform. See Fig. 2.

CC: DAC1600 counter clock input.

SW1-SW6: They are used by CPU as switch word. SW3 (RD1) is also used in reversing the direction of counting in valve register during manual mode.

LD1-LD3: Panel lamp driver outputs.

	IO-10	IO-9	IO-8	IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1
I/O Buffer										
Register A (mode register)	1	1	1	UP*	DN*	M5	M4	M3	M2	M1
Register B (valve register)	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1
Register C (set point register)	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1
Register D (switch/lamp driver register)	0	SW6*	SW5*	SW4*	SW3*	SW2*	SW1*	LD3	LD2	LD1

*Read only locations

Fig. 1 REGISTERS DATA BASE

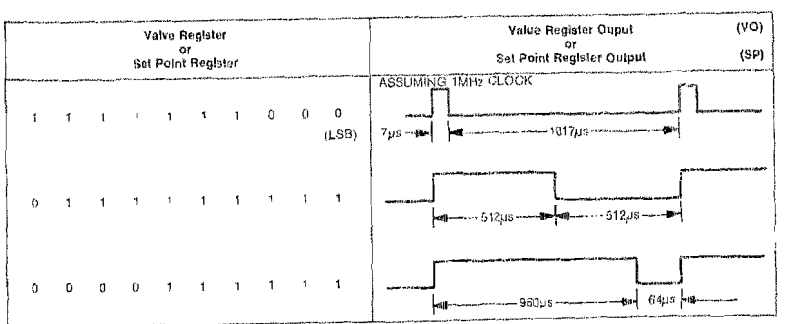


Fig. 2 PULSE WIDTH MODULATED OUTPUT WAVEFORMS

ELECTRICAL CHARACTERISTICS
Standard Conditions (unless otherwise noted)
T_A = 0°C to 75°C
V_{DD} = +12V ± 5%
V_{CC} = +5V ± 5%

Symbol	Characteristic	Min.	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	+0.65	V	*
V_{IH}	Input High voltage	2.2	V_{CC}	V	*
I_{IN}	Input Current	--	± 10	µA	V_{IN} = 0V to 5.25V
I_{LOH}	Output Lkg. Curr.	--	10	µA	CS* = 2.2V IO (1-10) = 4.0V
I_{LOL}	Output Lkg. Curr	--	-10	µA	CS* = 2.2V; V_{CC} = 5.25 V, IO (1-10) = 0.4V
C_{IN}	Input Capac	--	8	pF	f = 1MHz
C_{OUT}	Output Capac	--	10	pF	f = 1MHz @ V_{OUT} = 0.0V Tri-State Mode
V_{OL}	Output Low Voltage	--	0.45	V	*I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.7	V_{CC}	V	I_{OH} = 300µA* C_L = 100pF
I_{CC}	Supply Current	--	5	mA	
I_{DD}	Supply Current	--	25	mA	No Load

* Applies to TTL compatible inputs and outputs See Table 1 for other inputs and outputs

Table 1: THE FOLLOWING TABLE DEFINES INTERNAL PULL UP CURRENT SOURCES

Signal	In / Out	Pull Up	Comp	Loading
FA1,2,3	In	To +5V	TTL	≤ 1ma @ .4V
LD1	Out	--	--	Load Type A
LD2	Out	--	--	Load Type A
MI	In	None	Comp Type 1	
M0	Out	--	--	Load Type A
CM1	In	None	Comp Type 1	
CM2	In	None	Comp Type 1	
CM3	In	None	Comp Type 1	
MB1	Out	--	--	Load Type A
MB2	Out	--	--	Load Type A
SW3 (RD1)	In	To +5V	TTL	≤1ma @ .4V
SW2	In	To +5V	TTL	≤1ma @ .4V
SW1	In	To +5V	TTL	≤1ma @ .4V
VG	Out	--	--	Load Type B
SP	Out	--	--	Load Type A
UP1	In	None	Comp Type 1	
SW5	In	None	Comp Type 1	
DN1	In	None	Comp Type 1	
SW6	In	None	Comp Type 1	
SW4	In	None	Comp Type 1	
LD3	Out	--	--	Load Type A
SD	In	To +5V	TTL	≤1ma @ .4V
CC	In	Series RC to Common		
IS	In	To +5V	TTL	≤1ma @ .4V
CS*	In	To +5V	TTL	≤1ma @ .4V
I01, -10	In/Out	Tri State	--	Load Type C

COMPATABILITY

Comp. Type 1 High ..... 4V to 12V
Low 0.4V

LOADING

Load Type A Source ..... 2.5 mA @ 4V Min
Sink ..... 300 µA @ 0.4V Max

Load Type B Source ..... 10 µA @ 9V Min
Sink ..... 1mA @ 1.2V Max

Load Type C Sink ..... 1.6 mA 0.45V Max
Source ..... 300 µA @ 2.7V Min
Cap ..... 100 pF Max Load

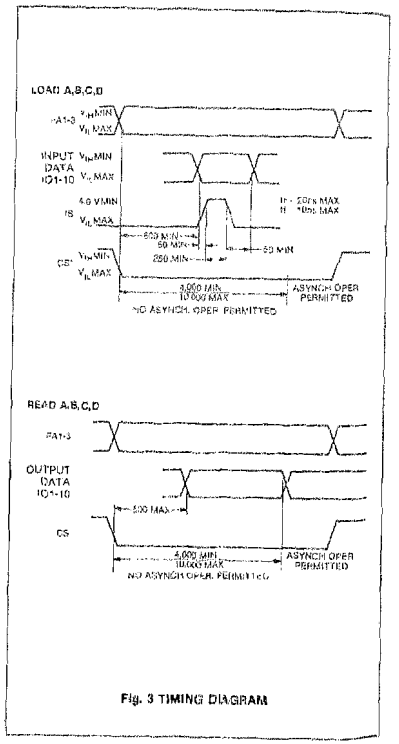


Fig. 3 TIMING DIAGRAM

Table 2 REGISTER AND FUNCTION SELECT

FA 3	FA 2	FA 1	Operation	Condition
0	0	0	Load 'A'	MI = 0
0	0	1	Load 'B'	
0	1	0	Load 'C'	
0	1	1	Load 'D'	
1	0	0	Read 'A'	
1	0	1	Read 'B'	
1	1	0	Read 'C'	
1	1	1	Read 'D'	

Table 3 MODE CONTROL

CM 3	CM 2	CM 1	M5	M4	M3	M2
		⊓	1	0	0	0
	⊓		0	1	0	0
⊓			0	0	1	0

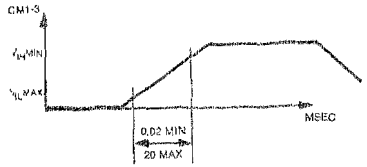


Table 4 MANUAL MODE FUNCTION CONTROL

MI	CS*	UP1	DN1	RD1	Operation
1	1	0	0	0	No Op
1	1	0	0	1	No Op
1	1	0	1	0	Incr "B"
1	1	0	1	1	Decr "B"
1	1	1	0	0	Decr "B"
1	1	1	0	1	Incr "B"
1	1	1	1	0	Indeterminate
1	1	1	1	1	Indeterminate
1	0*	X	X	X	No Op.
0	0	X	X	X	As specified by FA1-3
0	1	X	X	X	No Op

INCR/DECR speed is controlled by an internal variable frequency clock. The clocking rates are as follows
16Hz for 2 Sec
64Hz for 2 Sec
128Hz thereafter until UP1 or DN1 are deactivated

If CS remains low for longer than 10 µsec normal operation (per UP/DN) will resume.

Table 5 MANUAL MODE OUTPUT

MI	SD	MO
0	0	0
0	1	⊓⊓⊓ f = 2Hz
1	0	1
1	1	1

Table 6 MODE REGISTER STATUS

M5	M4	M3	M2	MB 2	MB 1
0	0	0	0	0	0
0	0	0	1	0	1
0	1	0	0	1	0
1	0	0	0	1	1

10A

18 Channel Analog Multiplexer

FEATURES

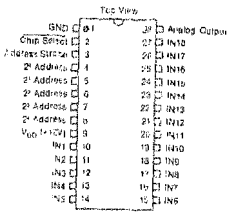
- Connects 1 of 18 analog inputs to analog output pin
- Address latch on-chip
- 0 to 6 volt input range
- Single +12V supply
- Analog output controlled by chip select signal

DESCRIPTION

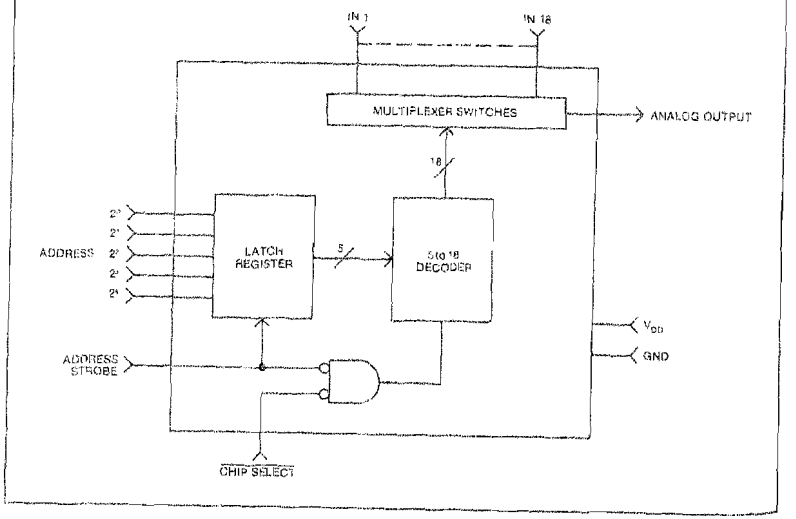
The MUX1600 is a binary addressed 18 channel analog multiplexer fabricated in General Instrument's advanced N-channel ion implant process. Featuring on-chip address latches and separate address strobe and chip select signals, the MUX1600 operates from a single +12 Volt supply.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and all other input/output voltages with respect to GND ..... -0.3V to +18V
Storage Temperature ..... -55°C to +150°C
Operating Temperature ..... 0°C to +70°C

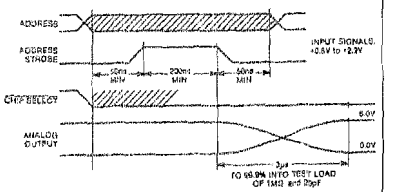
*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

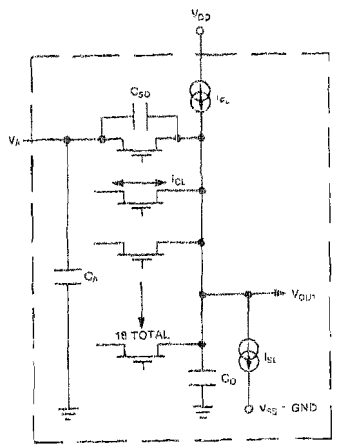
All voltages referenced to GND
V_{DD} = +12V ± 5%
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Symbol	Min	Typ	Max	Unit	Condition
Input Load Current (all digital inputs)	I_{IN}	--	--	±10	µA	V_{IN} = 0V to 5.25V
Power Supply Current	I_{DD}	--	--	8	mA	All digital inputs = 5.25V
Input Low Voltage	V_{IL}	-0.5	--	0.80	V	
Input High Voltage	V_{IH}	2.2	--	V_{DD}	V	
Analog Input Voltage	V_A	0.0	--	6.0	V	
Channel on Resistance	R_{ON}	--	--	600	Ω	V_A = 0V to 6V
Channel leakage (each channel)	I_{CL}	--	--	5	nA	V_A - V_{OUT} = 6V
V_{DD} Leakage	I_{PL}	--	--	10	nA	V_{DD} - V_{OUT} = 17V
Source to Drain Capacitance	C_{SD}	--	--	5	pF	f = 1 MHz
Analog Input Cap	C_A	--	--	5	pF	f = 1 MHz
Analog Output Cap	C_O	--	--	20	pF	f = 1 MHz
Digital Input Cap	C_D	--	--	5	pF	f = 1 MHz
Substrate Leakage	I_{SL}	--	--	410	nA	V_D - V_{SS} = 6V
18 I_{CL} + I_{PL} + I_{SL}	I_{LT}	--	--	500	nA	V_D - V_{SS} = 6V

SWITCHING CHARACTERISTICS



LEAKAGE CURRENT DIAGRAM



10A

16-Bit Microcomputer System

FEATURES

- Built around the General Instrument's CP1600 MOS N-Channel Microprocessor.
- Complete microcomputer system to enable rapid program development.
- Separate Data, Address and Control Buses.
- Up to 65K memory space
- Unlimited DMA channels
- Nested interrupt system with full priority resolution.
- Includes— MC1600 Microcomputer Module
  RM1602 8K RAM Memory Module
  I/O1600 TTY High Speed Reader Punch Interface Module
  CC1600 Control Console (Operator's Front Panel) and Control Console Module
  CF1600 Card File
  CA1600 TTY/EIA Cable Assembly
  CA1601 Reader/Punch Cable Assembly
  A full set of Software necessary to prepare and debug programs

GIMINI MICROCOMPUTER

DESCRIPTION

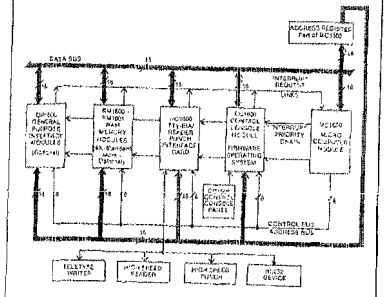
To simplify microprocessor hardware and software development, speed the product design cycle, and support product prototyping, a microcomputer development system and its associated components are a must. The Series 1600 family fills these requirements with the GIMINI Microcomputer—a versatile, general purpose, stand alone computer system built with the Series 1600 Semiconductor Components.

The GIMINI utilizes a totally modular design allowing the system designer maximum configurability. The system provides direct addressing to 65K words, unlimited DMA channels, and a multi-line/multi-level nested interrupt system with full priority resolution and self-identifying addresses. All control and timing signals as well as data and address buses are fully buffered and available for use in expanding memory or designing specialized I/O interfaces.

The basic hardware includes a card cage, front panel, and four printed circuit boards: the MC1500 Microcomputer Module, the RM1602 8K×16 RAM Memory Module, the CC1600 Control Console and Control Console Module, and the I/O1600 TTY-EIA/High Speed Reader Punch Interface Module. Up to 9 additional cards of any type can be added as required. With the addition of a TTY and a high speed reader/punch, the GIMINI becomes a test bed for customer designed interfaces and related hardware as well as a full program preparation facility. Its resident On-Line Debug Program allows testing of hardware and software directly on the system in real time and also totally eliminates the annoying bootstrap procedure. The On-Line Software Package provides the necessary program preparation aids, such as the Assembler, Super Assembler, Text Editor, the Relocating/Linking Loader and the Object Module Linker.

All of the card level modules of the GIMINI are available on an OEM basis for further system integration.

BLOCK DIAGRAM



GIMINI Accessories

FEATURES

CF1600 CARD FILE
- 13-position
- P.C. backplane with wirewrap capability
- Rack-mountable
- Cards are keyed to connectors
- 10.5" high x 19.0" wide x 12.0" deep

EX1600 EXTENDER CARD
- For use with all GIMINI cards
- Two 70-pin connectors

WW1600 WIREWRAP CARD
- 126 16-pin positions
- Power and ground planes provided
- 10 Test points on edge of card

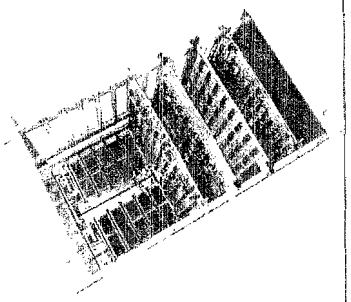
PS1600/PS1601 POWER SUPPLIES
- Provides all required voltages for the GIMINI Microcomputer System.
- PS1600 (115V, 60Hz): +5V at 12A, +12V at 2A; -12 V at 2A capability.
- PS1601 (200/250V, 50Hz): +5 at 15A; +12 at 2A; -12V at 2A capability.
- 1% line and load regulation
- Remote sensing capability.

CA1600 TTY/EIA CABLE ASSEMBLY
- 6-ft. cable for connecting I/O1600 Interface Module to TTY or EIA compatible device.

CA1601 READER PUNCH CABLE ASSEMBLY
- 6-ft. Cable for connecting I/O1600 Interface Module with high speed reader-punch.

CA1602 GP1600 MODULE CABLE ASSEMBLY
- 6-ft. cable for connecting GP1600 Interface Module with external device.

CARD FILE



CF1600 CARD FILE

SLOT	CARD
1	MC1600 Microcomputer Module
2	CC1600 Control Console Module
3-12	Memory or I/O Cards
13	I/O1600 TTY-EIA/Reader-Punch Interface Module

DESCRIPTION

The CF1600 Card File is designed to house up to 13 cards of the GIMINI family. The MC1600 Microcomputer Module, the CC1600 Control Console Module, and the I/O1600 TTY-EIA/Reader-Punch Interface Module each have one assigned position. The 10 remaining positions are available for memory modules, general purpose input-output cards, or special interface cards.

The printed circuit backplane parallels the power supply rails and the data, address and control buses for all 13 cards. There are separate voltage and voltage sense lines on the P.C. backplane for the +12V, -12V and +5V supplies. The bus system can be extended to another card file by wirewrapping or soldering a ribbon cable to one of the rear connectors.

The EX1600 Extender Card can be used with any other card of the GIC1600 family.

The WW1600 Wirewrap Card contains 126 16-pin sockets for prototyping special interface cards. Power and ground planes are provided.

The PS1600/PS1601 Power Supply provides all the power necessary to run the GIMINI Microcomputer System. The user has 2A of +12V and 2A of -12V available for extra memories and interfaces.

Also available is 9A of +5V if the system uses only one 8K RAM Memory Module. Special power supply configurations are available upon request.

The CA1600 TTY/EIA Cable Assembly is a 6' cable that has a 10-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections: one is left unterminated for connection to a TTY; the other is terminated in a 26-pin data connector for connection to an EIA device.

The CA1601 Reader/Punch Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the I/O1600 TTY-EIA/Reader-Punch Interface Module on one end. The other end is split into two sections; both are terminated in 26-pin data connectors, one for connection to the reader and the other for connection to the punch.

The CA1602 GP1600 Module Cable Assembly is a 6' cable that has a 34-pin 3M connector to interface with the GP1600 General Purpose Interface Module on one end. The other end is unterminated.

Analog to Digital Module

FEATURES

- 12-bit Analog to Digital Conversion
- ±10 volt inputs.
- 25KHz Standard Throughput Rate, Option 35KHz, 50KHz, 100KHz.
- 16 Channel Input
- Plugs directly into GIMINI System
- Operates from +5V DC source.
- Program controlled
- Interrupt capability.
- Interfaces directly with MC1600 Module

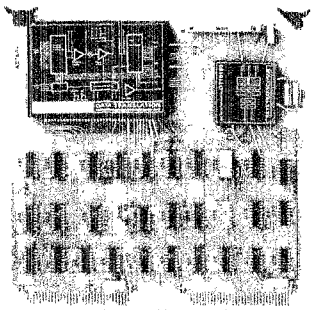
DESCRIPTION

The AD1600 is a multichannel analog data acquisition module which interfaces directly to General Instrument GIMINI microcomputers. The AD1600 provides 16 channels of ± 10 Volt Analog to 12-bit 2's complement digital data with a standard conversion rate of 25KHz. Conversion rates of 35KHz, 50KHz and 100KHz are available.

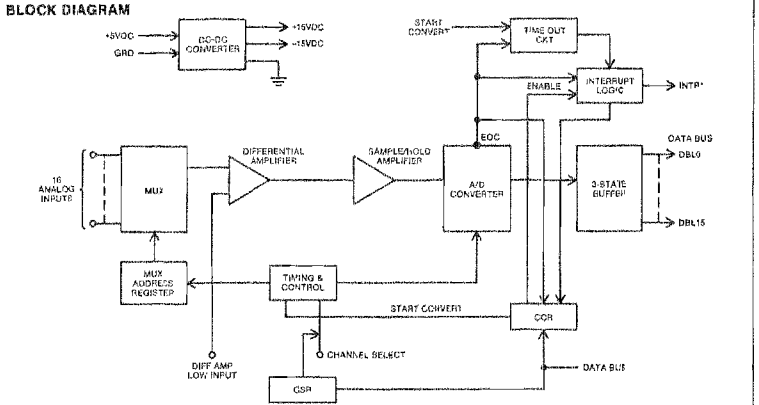
The AD1600 is controlled via three operational registers which are used to select a specific analog input channel, start data conversion, determine when conversion is complete and input the resultant digital data. These registers are cleared initially when a console master clear is issued and set under program control.

The AD1600 is operated by first setting an analog input channel address (0-17) in the Channel Select Register (CSR). Analog to digital conversion is started by setting the Start Conversion bit in the Conversion Control Register (CCR). When the analog to digital conversion is complete the End Conversion bit in the CCR becomes a "1". This bit may be sampled under program control or if the CCR Interrupt Enable bit is set, an interrupt is generated when end of conversion occurs. If after a start convert signal is generated an end of conversion doesn't occur, the CCR Error bit is set instead of the End Conversion bit. This bit may also be sampled under program control or if the CCR Interrupt Enable bit is set, an interrupt is generated when the error bit becomes a "1"

ANALOG TO DIGITAL MODULE



BLOCK DIAGRAM



AX1600: Auxiliary Module

FEATURES

- Companion to MC1600 and RM1602
- 1K×16 PROM
- UART I/O
- Interrupt Capability
- 16-Bit Output Latch
- 16-Bit Input Port
- Automatic Start-up Circuitry
- RS-232 or 20 MA TTY Loop
- Selectable BAUD Rates 110 to 9600 BAUD

DESCRIPTION

The AX1600 Auxiliary Module is the third card of a set of three of the Series 1600 modules that form a complete 16-bit microcomputer. The first two are the MC1600 Microcomputer Module and the 8K×16 RAM Memory Module. The AX1600 Auxiliary Module contains all other computer functions other than processing and memory; specifically, it has serial I/O, a 16-bit output port, a 16-bit input port, 1K×16 of PROM, interrupt circuitry, and automatic start-up circuitry. It is contained on a a 9.75"×9.25" PC board which mates with a dual 70 pin connector

DA1600: Digital to Analog Module

FEATURES

- 4 D/A's on One Card
- 12-Bit Resolution
- ±10 Volt Outputs

DESCRIPTION

The DA1600 is a multichannel digital to analog data output module which interfaces directly to GI's GIMINI Microcomputers. The DA1600 provides four separate 12-bit 2's complement digital to ±10 Volt analog outputs. Each of the four analog outputs is controlled by a corresponding Analog Data Register (ADR) which has a unique bus address. A stabilized analog output signal is generated in a maximum of 8us after a 12-bit digital quantity is placed in the corresponding ADR. The four analog outputs are initially set to zero Volts when a console master clear is issued and are under program control thereafter. The DA1600 Digital to Analog Module is contained on a 9.75"×9.25" PC board which mates with a dual 70 pin connector

SC1600: GIMINI Single Card Microcomputer Module

FEATURES

- CP1600 with multi-level priority interrupt structure and DMA channel for floppy disc
- 16K words of RAM
- 4K words of PROM sockets
- Real Time Clock - crystal controlled with 4 strap selectable frequencies
- Power Down Interrupt
- 6-bit System I/O Port with full handshake control lines
- Two UART-RS232 compatible Serial I/O Channels with strap selectable baud rate
- Up to 32 Digital Output Lines with interrupt capability (IOB1680)
- Up to 32 Digital Input Lines with Interrupt capability (IOB1680)
- Up to 5 Programmable 16-bit Timers
- Resident Operating Systems in PROM
- ROM Resident Utility Functions including MUL, DIV, SQRT, Floating Pnt. Operations, Code Conversions, etc
- Resident Drivers for all I/O Functions and Floppy Disc
- Integral Power Supply with power-down detection output and power-up initialization output

GIMINI SINGLE CARD MICROCOMPUTER

Under Development

10A

Control Console and Control Console Module

FEATURES

- 16-bit Data/Address Display
- 16-bit Switch Register
- Easy to use Control Panel:
  - Display/Modify all 8 internal registers
  - Display/Modify the CPU Status Word.
  - Display/Modify all 65K Memory Space.
  - Single Instruction operation.
  - Program Counter Inhibit capability
- ROM based Operating System
  - Conversational Monitor
  - On-Line Debug Program/Software Breakpoints
  - Relocating Loader (Eliminates Bootstrap)
  - Memory Dump Program
  - General Utilities/Input-Output Drivers
- Standard 19" x 10½" rack mountable Control Panel

DESCRIPTION

The CC1600 Control Console and Control Console Module is designed to provide a convenient method of controlling and monitoring the GIMINI System. The CC1600 consists of a front panel and a printed circuit module that are connected with two 34 pin flexible cables. The module contains the control logic to handle all front panel commands as well as the required interrupt logic to interface with the Microcomputer Module.

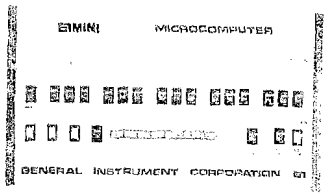
The Control Console Module consists of six control ROMs, scratch pad memory (256x16), a 16-bit Switch Register, a 16-bit Display Register, and the control logic to service any front panel request.

All functional operations for the Control Console are performed by the execution of program stored in the control ROMs. Pressing any action switch on the Control Console results in an interrupt request to the CP1600. After this interrupt is acknowledged, the CC1600 supplies the starting address of the Control Console service routine which performs the required function. In addition, the program automatically stores all CP1600 register in the scratch pad memory which is accessible via front panel selection. Consequently, whenever the CP1600 is in the HALT mode, the Control Console has direct access to all updated CP1600 information.

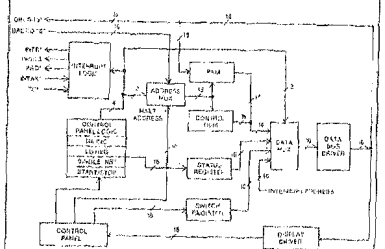
The control ROMs also contain all the firmware necessary for the development of micro-processor based systems. An On-Line Debug program is included so that software breakpoints and memory search routines may be executed. The system monitor allows the user to maintain conversational control via teletype interaction. The Relocating Loader can be used to input data from either a TTY or High Speed Reader, while the Memory Dump program allows any block of memory to be punched onto paper tape.

The Control Console Module is packaged on a 9.75" x 9.25" P.C. board, which mates with a dual 70-pin connector. It also interfaces with two 34-pin connectors for connection to the control console. Its operating temperature is 0° C to 55°C. It requires +5V ±5% at 1.0A.

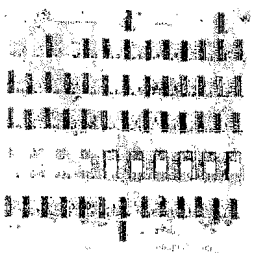
CONTROL CONSOLE



BLOCK DIAGRAM



CONTROL CONSOLE MODULE



General Purpose Interface Module

FEATURES

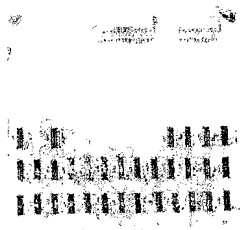
- 1 16-bit Addressable Input Port
- 1 16-bit Addressable Output Port
- 2 Addressable Status Registers
- Interfaces directly with MC1600 Module
- Space provided for sockets for I/O Control Logic
- Full Interrupt Capability.

DESCRIPTION

The GP1600 General Purpose Interface Module has two software addressable ports: one 16-bit input port and one 16-bit output port. Each port has an associated 4-bit status register that is addressable via program control. Provision is made so that the peripheral device can be operated on an interrupt or polling basis. Address decoding for the module is provided on the card although specific port assignments are determined by backplane selection. It is therefore possible to use up to eight GP1600 in a given system.

Connection to a given peripheral device is accomplished by a flat ribbon cable. Dual 34 pin connectors are mounted at the top end of the module. Space has been provided to accommodate wire wrap sockets so that specific interface circuitry may be incorporated on the module. Control and data signals have been brought out to wire wrap pins to facilitate prototype development.

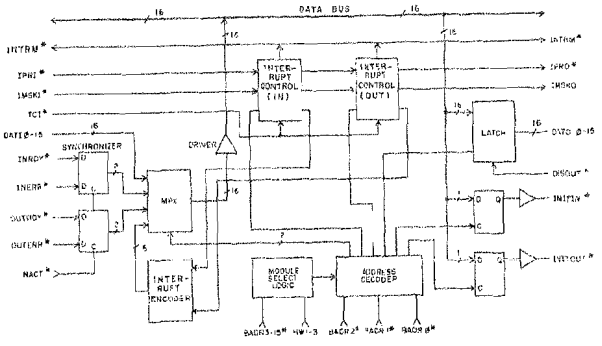
GENERAL PURPOSE INTERFACE MODULE



The module will accept dual-in-line package components mounted in standard wire wrap sockets. Locations for 14, 16, 22, 24 pin sockets are available.

The GP1600 General Purpose I/O Module is a 9.75" x 9.25" printed circuit card. Its operating temperature range is 0°C to 55°C.

BLOCK DIAGRAM



10A

TTY-EIA/Reader-Punch Interface Module

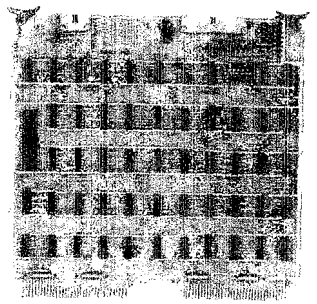
FEATURES

- Teletype Asynchronous Transmitter-Receiver and Control (UART)
- High Speed Reader/Punch Controller
- EIA (RS-232C) Interface
- Interfaces directly with MC1600 Microcomputer Module
- TTL Compatible to I/O Peripherals

DESCRIPTION

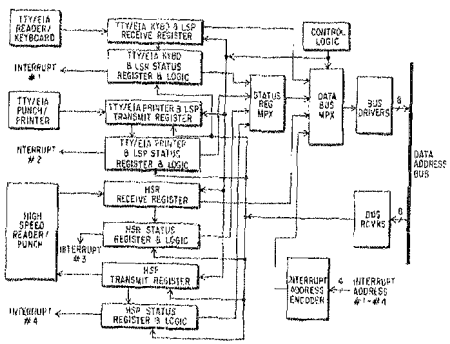
The I/O1600 TTY-EIA/Reader-Punch Interface Module handles full duplex communication between a Teletype, High Speed Reader/Punch combination or any RS-232C compatible device and the MC1600 Microcomputer Module. The I/O1600 Module has complete interrupt capability with four separate channels: two for the receiver section, High Speed Reader and TTY Reader/Keyboard; and two for the transmitter section, High Speed Punch and TTY Punch/Printer. These four interrupt channels operate independently with the receiver sections taking priority over the transmitter sections on simultaneous interrupts. The High Speed Reader/Punch has a higher priority than the TTY. Electrically, the I/O1600 Module has a 20 mA currentloop for TTY operation and a TTY reader control line which allows the microprocessor to control the Teletype reader during on-line operation. The High Speed Reader/Punch interface controls a high speed Reader/Punch combination capable of reading paper tape at 300 characters per second and punching tape at 60 characters per second. The I/O1600 module also provides the additional capability of interfacing with any RS-232C compatible terminal.

TTY-EIA/READER-PUNCH INTERFACE MODULE



The I/O Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. It also interfaces with a 10 pin connector for the TTY and a 34 pin connector for the high speed reader/punch. Its operating temperature is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at .2A and −12V±5% at .2A.

BLOCK DIAGRAM



Microcomputer Module

FEATURES

- Complete microcomputer module with system clocks, memory interface, and fully buffered Address, Data, and Control Buses
- Built with General Instrument's CP1600 MOS N-Channel microprocessor
- Two Phase CPU Clock
- Direct and Register Addressing up to 65K memory space
- Memory stack pointer
- Two Programmable Interrupt Lines/Multi-Level and Self Identifying
- DMA Channel Capability
- 16 External Sense Conditions for Conditional Branching
- Generalized Initialization Logic
- Real Time Clock Interrupt
- Power Fail Interrupt

DESCRIPTION

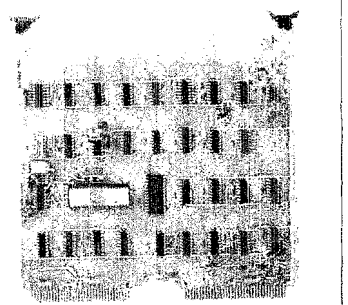
The MC1600 Microcomputer Module is a complete 16-bit parallel processing unit. It contains the hardware necessary to interface with memory and I/O. This is the main module in the GIMINI System.

The Microcomputer Module is designed around the CP1600, a 16-bit microprocessor on a chip. The MC1600 contains a 16-bit wide Bidirectional Bus Driver, Address Register and Driver, Bus Control Decoder-Driver, Crystal Oscillator, Clock Driver, an External Branch Multiplexer, A Real Time Clock Interrupt and a Power Fail Interrupt.

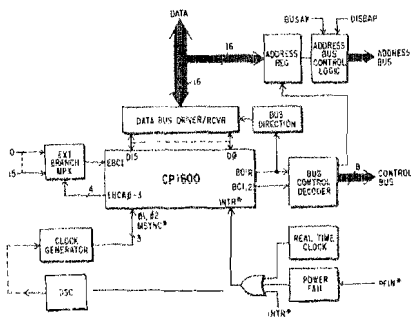
Two line, multi-level interrupt capability and Direct Memory Access are provided on this module. In response to an interrupt, the microcomputer automatically saves the current Program Counter on the Memory Stack, resolves interrupt priority and vectors to the device's interrupt service address. The direct memory access capability allows an alternate source to access memory or I/O while temporarily suspending processor operation. At the completion of a DMA operation, normal program execution continues in normal fashion.

The Microcomputer Module is a 9.75" × 9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0°C to 55°C. It requires +5V±5% at .5A, +12V±5% at 1A and −12V±5% at 4 ma.

MICROCOMPUTER MODULE



BLOCK DIAGRAM:



PROM Memory Module

FEATURES

- Provides sockets for up to sixteen PROMs (4096×16)
- Static Memory - no clocks required
- Field programmable
- Erasable with short wave ultra-violet light
- 1 μs max. access time
- Buffered TTL inputs - 1 load
- Open collector TTL output - 30 loads
- Module decoding for 65K memory expansion

DESCRIPTION

The PM1600 PROM Memory Module is a standard 4096×16 memory module for use in the GIMINI Microcomputer System.

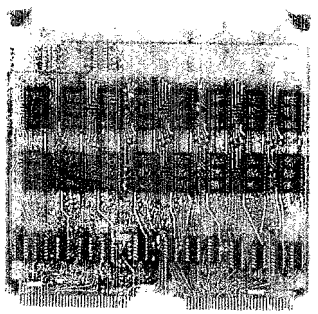
It is useful during the initial product design phase before freezing the program for a production quantity of lower cost masked ROMs, such as General Instrument's 16K RO-3-8316A(2K×8).

This memory module has sixteen sockets for 4096-bit static read-only memories. Each row of 8 rows will provide 512 16-bit words of memory. Each row contains 2 PROMs.

The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the PROMs. The sixteen data outputs from the PROMs are buffered onto the Data bus of the GIMINI System. For memories larger than 4K×16, decoding on the module allows addressing for a total of 65K memory.

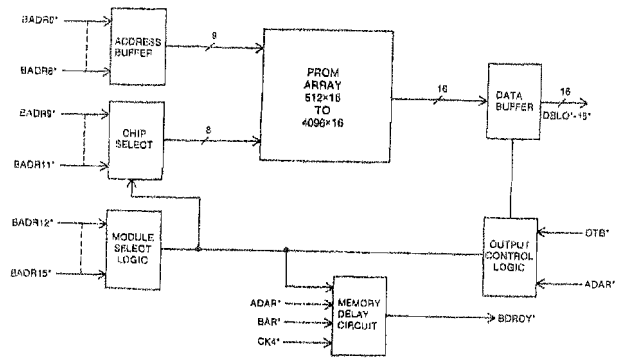
A special memory delay circuit is also provided on the board and is used to insure that the CP1600 microprocessor waits until stable data is available from the PROMs

PROM MEMORY MODULE



The PM1600 PROM Memory Module is a 9.75"×9.25" P.C. board, which mates with a dual 70 pin connector. Its operating temperature range is 0° to 55° C. A board fully loaded with all 16 PROMs will require +5±5% at .5A and -12±5% at .5A.

BLOCK DIAGRAM



2Kx16 RAM Memory Module

FEATURES

- 2048—16-bit words per module
- Static memory, no clocks required
- Single +5 Volt Supply
- Byte or Word Capability
- Module decoding for 65K memory expansion
- 750 ns Read/Write Cycle Time
- Open Collector TTL Output—30 Loads
- Buffered TTL Inputs—1 Load

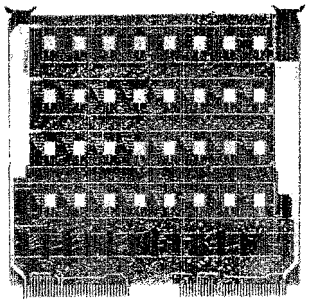
DESCRIPTION

The RM1600 Memory Card is a standard 2Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, low or high byte word selection logic, and is implemented with General Instrument's RA-3-4256B 1024 bit static Random Access Memory. There are thirty-two 22 pin 256x4 static RAM's packaged on a 8.75" x 9.25" x .062" printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0°C to 55°C. It requires +5V ±5% at 2.0A typical.

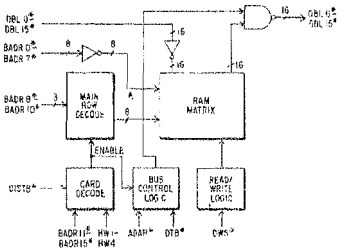
The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System

If more than one 2K memory card is used in the GIMINI System, provisions are provided for proper selection of 2K increments, up to 65K (32 modules) memory space

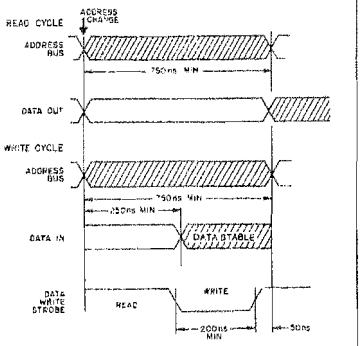
2KX16 RAM MEMORY MODULE



2Kx16 MEMORY CARD



TIMING DIAGRAMS



10A

RM1601

8Kx16 RAM Memory Module

FEATURES

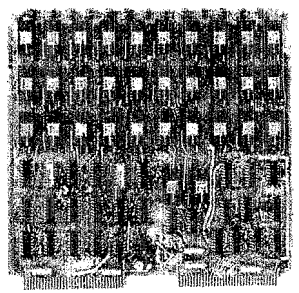
- 8192 — 16-bit words per module.
- Static memory, no clocks required.
- Byte or Word Capability.
- Module decoding for 65K memory expansion
- 400 ns Read Time.
- 500 ns Cycle Time.
- Open Collector TTL Outputs—30 Loads
- Buffered TTL Inputs—1 Load

DESCRIPTION

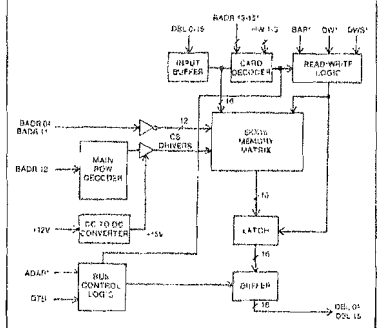
The RM1601 Memory Card is a standard 8Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, low or high byte word selection logic, and is implemented with General Instrument's RA-3-4402 4096 bit static Random Access Memory. There are thirty-two 22 pin 4Kx1 static RAM's packaged on a 8.75" x 9.25" x .062 printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0°C to 55°C. It requires +5V ±5% at 0.5A typical, +12V ±5% at 0.5A typical and -12V ±5% at 0.1A typical. The Address bus inputs from the GIMINI to the memory card are buffered to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System

If more than one 8K memory card is used in the GIMINI System, provisions are provided for proper selection of 8K increments, up to 65K (8 modules) memory space.

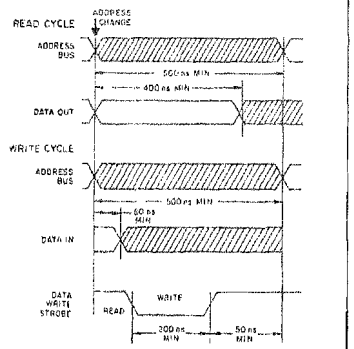
8Kx16 RAM MEMORY MODULE



8K×16 MEMORY CARD



TIMING DIAGRAMS



RM1602

8Kx16 RAM Memory Module

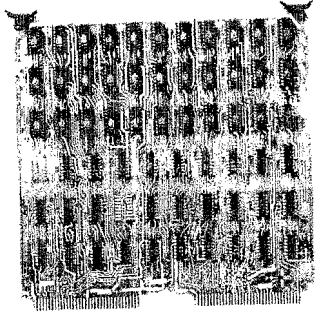
FEATURES

- 8192 — 16-bit words per module
- Dynamic memory with Refresh logic (Refresh during no-action state of CP 1600).
- Byte or Word Capability
- Module decoding for 65K memory expansion
- 400ns Read time
- 500ns Cycle time
- Open collector TTL outputs - 30 loads
- Buffered TTL inputs — 1 Load

DESCRIPTION

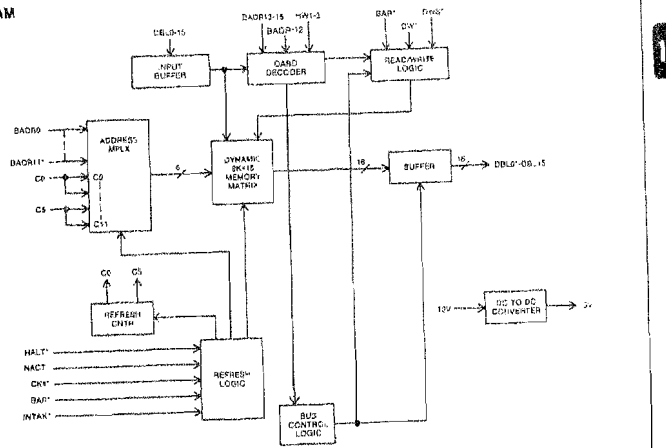
The RM 1602 Memory Card is a standard 8Kx16 memory module for use in the GIMINI Microcomputer System. This memory card contains address and data buffers, read/write circuits, refresh logic, address multiplexer, low or high byte word selection logic. There are thirty-two 16-pin 4Kx1 dynamic RAM's packaged on a 9.75"x9.25"x.062 printed circuit board, which mates with a dual 70 pin connector. Its operating temperature is 0° C to 55° C. It requires +5V ±5% at 2A, +12V ±5% at .5A, typical and -12V ±5% at 0.02A typical. The address bus inputs from the GIMINI to the memory card are buffered and multiplexed to provide the necessary address inputs to the RAM's. The sixteen data outputs from the RAM are buffered onto the Data bus of the GIMINI System

8Kx16 RAM MEMORY MODULE



If more than one 8K memory card is used in the GIMINI system, provisions are provided for proper selection of 8K increments up to 65K (8 modules) memory space

BLOCK DIAGRAM



Software

FEATURES

- Cross Software Package including Assembler/Simulator programs
- On-Line Software Package for Program Preparation on Microcomputer.
- Resident Firmware in ROMS on Control Console Module in GIMINI Microcomputer allows conversational debugging of programs.
- Subroutine Library: Math packages, Code Conversion routines, String Operators, etc.

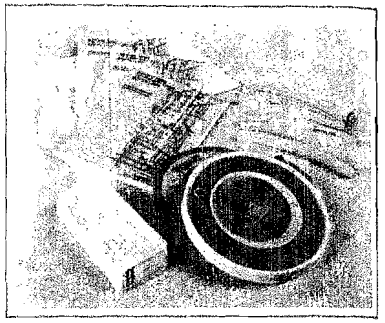
DESCRIPTION

Software is fundamental to making every microprocessor come alive and the Series 1600 is no exception. The entire product family is supported by an extensive software system designed to make program development fast and efficient. Most important, the software structure is designed to grow with the hardware to insure a long term product continuity.

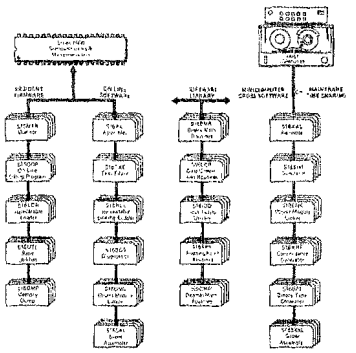
The Series 1600 Cross Software Package contains a versatile set of program preparation tools including compatible Assembler/Simulator programs operating at two different computer system levels—large machine or time share, or popular minicomputer systems. Each accepts Series 1600 assembly language statements as input and produce relocatable, linkable object code as output. In addition, the full microprocessor environment, including I/O operations, is simulated on the host machine so that complete program debugging and testing can be performed before committing to hardware. The combination of these features along with the ability to use a minicomputer as a host processor results in the lowest cost,easiest to use, Cross Software Package in the industry.

The GIMINI Microcomputer System also serves as a program preparation and hardware debug facility with the aid of its resident firmware and the On-Line Software Package. The resident firmware consists of a basic operating system containing a Monitor, the On-Line Debug Program, the Relocating Loader, the Memory Dump Program, and a number of other basic utility routines. The firmware also supports the system I/O with generalized routines for input/output from a TTY, high speed paper tape reader/punch, or any RS232 compatible device.

The On-Line Software Package includes the Symbolic Assembler, the Text Editor and the Relocating/Linking Loader, the Object Module Linker and the Super Assembler. The Object Module Linker provides the same features as S16LNK allowing generation of relocatable or absolute load modules on-line. The Super Assembler allows programs to be coded using high level procedure oriented statements while providing all the flexibility of basic assembly language.



SOFTWARE LINEUP



S16XSFT CROSS SOFTWARE PACKAGE

The Series 1600 Cross Software Package is coded in low level Fortran IV and is specifically designed to operate in a 16-bit minicomputer environment. The Cross Software package has been installed on many popular minicomputer systems such as DGC NOVA and DEC PDP11. The Cross Software package has also been installed on many popular time-sharing computer systems.

S16XAL CROSS ASSEMBLER
Symbolic representation of all instructions
User defined six character symbols
Octal, decimal, hexadecimal and ASCII literals
Expression evaluation
Extensive assembly directives
Absolute, Relocatable or Relocatable/Linkable assembly
Full program and sorted symbol listing
Extensive error detection

S16XRF CONCORDANCE GENERATOR
Assembly symbol cross reference map

S16LNK OBJECT MODULE LINKER
Resolves global/external symbol linkages
Relocates and merges object modules
Produces relocatable/absolute load module
Produces load module map

S16SIM SIMULATOR
Full Series 1600 instruction set simulation
Full 65K word memory simulation
I/O and interrupt simulation
Memory and/or Register breakpoints
Memory and/or Register traces
Simulated program execution time accumulation
Program execution time and stack size limits
Inspection and modification of memory and registers
Symbolic memory addressing

S16BPT BINARY PAPER TAPE GENERATOR

S16RTG ROM PATTERN TAPE GENERATOR

S16SXAL SUPER ASSEMBLER
High level procedure oriented instructions plus all features of S16XAL

GIMINI RESIDENT FIRMWARE

The resident firmware in the GIMINI Microcomputer System creates an efficient, easy to use, prototyping tool for the development of microprocessor based products. The firmware performs all front panel functions as well as creating a terminal driven operating environment. Features include the following:

S15MTR MONITOR
Conversational system control
TTY communications

S16DP ON-LINE DEBUG PROGRAM
Eight program breakpoints
Register/Memory display and modify
Memory search and initialize
Single step/Execute commands
Modify Branch and Jump destinations
Module Relocation Origins

S16LDR RELOCATING LOADER
Full relocation capability
TTY or H.S. Paper Tape Reader Input

S16MDP MEMORY DUMP PROGRAM
Punches in S16LDR format
TTY or H.S. Paper Tape Punch output
Generalized Code Conversions
TTY input/output driver
H.S. Paper Tape Reader/Punch driver

SERIES 1600 ON-LINE SOFTWARE PACKAGE

The Series 1600 On-Line Software Package is written in assembly language and runs on the GIMINI Microcomputer System. All programs are designed to be directly input/output compatible with the S16XSFT Cross Software Package so that either means of program preparation can be used interchangeably.

S16AL ASSEMBLER
Same features as S16XAL

S16TXE TEXT EDITOR
Multiple line buffering
Symbol search
Character, line, string editing

S16RLL RELOCATING/LINKING LOADER
Global and external symbol resolution
Full relocation capability
Loads and links multiple object modules
Memory map

S16DGS DIAGNOSTICS
Memory diagnostic
Instruction test
I/O Controller exerciser

S16OML OBJECT MODULE LINKER
Same features as S16LNK

S16SAL SUPER ASSEMBLER
High level procedure oriented instructions plus all features of S16AL

SERIES 1600 SUBROUTINE LIBRARY

The Series 1600 Microprocessor System is supported by an extensive and growing library of useful subroutines designed to relieve the user of many time consuming software chores. All of Subroutine Library programs are written in Series 1600 Assembly Language making them both fast and efficient. They are compatible with both the Series 1600 Symbolic Cross Assembler (S16XAL) and the Series 1600 On-Line Assembler (S16AL). In addition, all library programs are designed to be directly compatible with hardware extensions to the Series 1600 product family so that increased performance can be achieved without software complications.

S16BMR BINARY MATH ROUTINES
Signed Multiply/Divide
Square Root
Double Precision Multiply/Divide
Double Precision Square Root

S16CCR CODE CONVERSION ROUTINES
Binary to BCD—BCD to Binary
Binary to ASCII—ASCII to Binary
Binary to HEX—HEX to Binary
Binary to OCTAL—OCTAL to Binary
Fixed to Floating—Floating to Fixed

S16IOD INPUT/OUTPUT DRIVERS
TTY Input/Output
H.S. Paper Tape Reader/Punch Input/Output
Byte Table Pack—Byte Table Unpack

S16FPR FLOATING POINT ROUTINES
Floating Add/Subtract
Floating Multiply/Divide
I/O Conversion

S16DMR DECIMAL MATH ROUTINES
Decimal Add/Subtract
Decimal Multiply/Divide
Decimal Square Root
Decimal Compare

Super Assembly Language

FEATURES

- High level operations LET, GOTO, GO@, CALL, IF, IF-THEN, IF-THEN-ELSE, DO, DO-FOR, DO-WHILE
- Array subscripting
- Literal representation in Binary, Octal, Decimal, Hexadecimal and character notation
- Symbolic representation of all CP1600 instructions
- Directives for
  - Controlling register utilization of high level operations
  - Controlling storage allocation
  - Initializing storage
  - Specifying character strings
  - Declaring a program entry point
  - Declaring global and external symbols
  - Declaring a program entry point
  - Specifying assembly output form
  - Controlling conditional assemblies
- Absolute and Relocatable load module output
- Absolute and Relocatable linkable object module output
- Program listing
- Extensive error diagnostics

DESCRIPTION

The General Instrument Super Assembly Language enables the CP1600 user to implement programs at a procedural level using FORTRAN-like statements rather than at the machine level of conventional assembly languages. Super Assembly Language includes LET, IF, CALL, DO, GOTO, and GO@ high level operations as well as all the instruction mnemonics and assembly directives of basic CP1600 assembly language. Super Assembly Language provides both the novice and the experienced programmer with the convenience and efficiency of procedural level programming while retaining the flexibility and economy of basic assembly language. Many applications can be completely coded using the high level operations, but when required, basic assembly statements can be intermixed freely with high level statements. The CP1600 Super Assembly Language is based on the popular high level programming languages, FORTRAN and BASIC.

The Super Assembler Program converts source programs written in CP1600 Super Assembly Language into binary machine code. This conversion process is accomplished by making two passes through a source program. The Super Assembler Program also produces a listing of the assembled program; the full instruction expansion into machine assembly language for each high level statement may be printed on the listing, if the expanded listing option is selected by the user.

HIGH LEVEL STATEMENTS

GOTO

The GOTO statement is used to transfer program control unconditionally to a specified destination.

Ex GOTO SCAN

GO@

The GO@ statement is used to transfer program control unconditionally indirectly through a specified storage designator to a destination. The destination is defined by the current contents of the storage designator.

Ex. GO@ TABLE(I)

CALL

The CALL statement is used to transfer program control to a subroutine. Arguments, i.e. parameters to be passed to the subroutine, follow the subroutine name enclosed in parenthesis and separated by commas.

EX. CALL SQRT(I,J)

LET

The LET statement is used to perform data transfers, arithmetic computations and logical operations involving constants, variables and subscripted variables. Addition, subtraction, multiplication, division, negation and logical NOT, AND, exclusive OR and inclusive OR operations may be performed using the LET statements.

EX. LET X = .NOT. Y .AND. Z + 5

IF

The IF statement is used to perform tests on single quantities and make comparisons between two quantities. The quantities may be constants, variables, assembly expressions and subscripted variables. An IF statement may be of three types: arithmetic, conditional or relational. The arithmetic IF is used to test a quantity for negative, zero and positive and directly transfer to a corresponding destination. The conditional IF is used to test a quantity for positive, negative, zero and non-zero and the relational IF is used to compare two quantities. The conditional and relational IF statements may execute a GOTO statement if true. They may also cause a THEN-ELSE (THEN, if true and ELSE, if false) sequence of instructions to be executed. The THEN-ELSE capability is a feature not found in FORTRAN or BASIC and is similar to the IF-THEN-ELSE facilities in more powerful languages such as ALGOL, COBOL and PL/I.

```
EX.  IF ANSWR .ZERO. GO TO NEXT
     IF QUANT .EQ. LIMIT THEN
     CALL SQRT(A)
     END

EX:  IF A .EQ. 2 THEN
     LET B=5
     ELSE
     LET B=6
     END
```

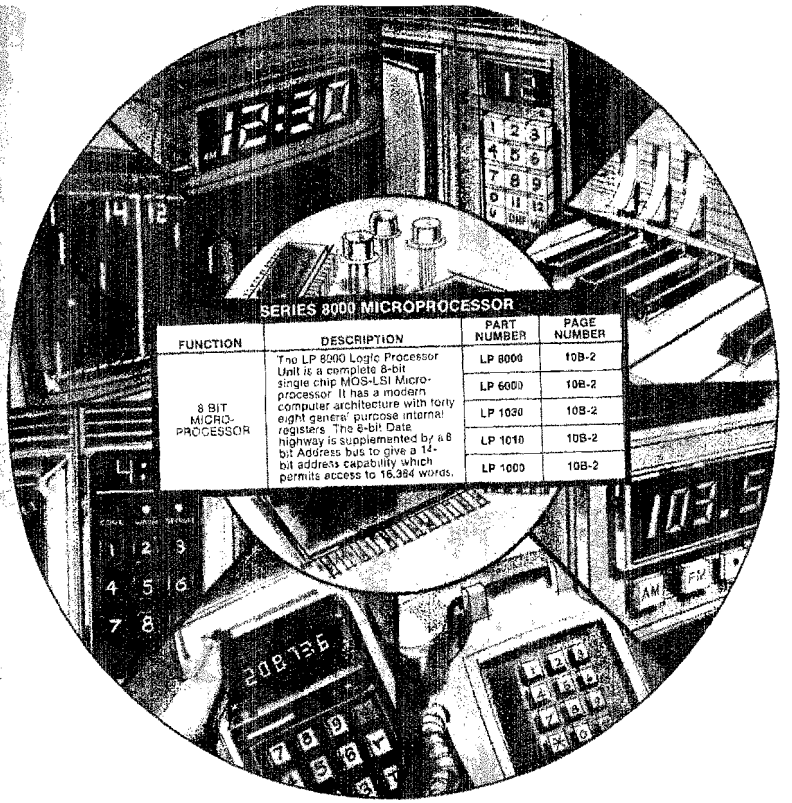
DO

The DO statement is used to perform looping and iterative operations by causing a sequence of statements between the DO statement and a corresponding CONT (CONTinue) statement to be executed repeatedly. Such a statement sequence is known as a DO loop. DO loops may be nested i.e. contain other DO loops up to a depth of four levels. When DO loops are nested, inner loops terminate before outer loops. DO loops may be controlled by FOR or WHILE conditions.

```
EX.   ABC   DO ABC FOR I = INIT, MAX, INCR
            IF (TBL (I) .EQ. QTY) GO TO GETOUT
            CONT

EX..  XYZ   DO XYZ WHILE QTY .GT. LIM
            LET K = K .AND. MASK
            LET QTY = K + INCR
            CONT
```

10A



SERIES 8000 MICROPROCESSOR

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 BIT MICRO-PROCESSOR	The LP 8000 Logic Processor Unit is a complete 8-bit single chip MOS-LSI Micro-processor. It has a modern computer architecture with forty eight general purpose internal registers. The 8-bit Data highway is supplemented by a 8 bit Address bus to give a 14-bit address capability which permits access to 16,384 words.	LP 8000	10B-2
		LP 6000	10B-2
		LP 1030	10B-2
		LP 1010	10B-2
		LP 1000	10B-2

10B

SERIES 8000 MICROPROCESSOR

MICRO ELECTRONICS

8-Bit Microprocessor System

FEATURES

- 2 Chip Minimum System (plus clock)
- 48 Accessible 8 Bit Internal Registers
- 48 Basic Instructions
- Binary and Decimal Arithmetic Capability
- Direct and Indirect Input Output Capability
- Automatic subroutine nesting on memory devices
- Family of development devices

DESCRIPTION

The Series 8000 Logic Processor System is designed to perform any digital function using far fewer packages than a TTL or CMOS implementation. Typically a 100 package system can be reduced to a three chip solution of LP8000 Processor, LP6000 Program Memory and LP1030 Clock Generator (two 40 lead DIP plus one 8 lead DIP). The consequent savings in development and production costs and increased reliability give the user many of the advantages of a customized LSI solution but without the restriction that it must be a high volume product.

The System is fabricated with General Instrument's P-channel Nitride Process which has a proven reliability and production history. All members of the Series 8000 family including Read Only Memories, General Purpose Input Output and Memory interface parts are fully compatible with each other.

The LP8000 Logic Processor Unit itself is a complete 8-bit single chip MOS-LSI Microprocessor. It has a modern computer architecture with forty eight general purpose internal registers. This, coupled with a binary and decimal capability arithmetic unit allows a versatile and sophisticated implementation of a microcomputer system. The 8-bit Data highway is supplemented by a 6-bit Address bus to give a 14-bit address capability which permits access to 16,384 words in combination of program memory, data memory or peripheral devices. The address space consists of 64 "modules" which can be either 256 words of memory or one 8-bit bidirectional I/O port.

LOGIC PROCESSOR - LP (Part number LP8000)

The logic processor (LP) is the heart of the Series 8000 system. It performs all of the arithmetic and logical functions required and also controls all activities occurring in the Series 8000 system. It has 48×8 bit working registers and an 8 bit input/output interface to which external peripherals may be attached directly.

PROGRAM MEMORY - PM (Part number LP 6000)

The program memory PM contains a 1K x 8 bit memory which stores the user's program. This chip also includes the program counter which points to the current address. It is arranged at the top of a four word hardware stack which is controlled by the LP for subroutine nesting. Two directly addressable 8 bit I/O interfaces are included, so that a minimum system consisting of one LP and one PM has 24 I/O leads. Extra PMs can be connected to the main system bus, up to a maximum of 16K words. Each PM and I/O interface can be addressed by the LP, the module addresses being programmed at the same time as the customer's program.

MEMORY INTERFACE CHIP - MIC (Part number LP 1000)

The memory interface chip consists of an 11 bit program counter at the top of four word hardware stack. The address output are TTL compatible and enable any external 2K×8 bit memory to be addressed. Other circuits allow the MIC to interface directly to the Series 8000 system without any external components. It is intended for use when breadboarding systems or when using non-standard memory, e.g. diode matrix, core, etc.

The memory area can be extended by using several MIC/external memory combinations. The addresses are selected by hardwiring pins to V_{GG} or V_{CC}.

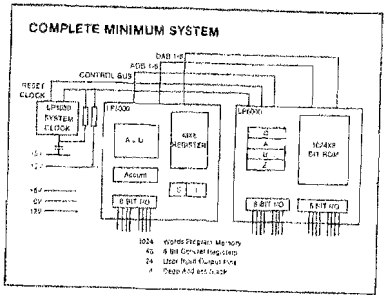
INPUT/OUTPUT BUFFER - IOB (Part number LP 1010)

The input/output buffer consists of two addressable 8 bit I/O interfaces. The addresses are selected by hardwiring pins to V_{GG} or V_{CC}.

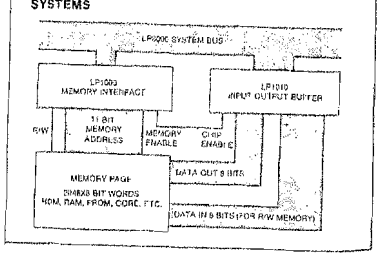
CLOCK GENERATOR - CG (Part Number LP1030)

The Series 8000 needs only an 800KHz clock, a power-on-reset signal to clear and synchronize the system and two power supplies. Virtually all external components may be eliminated by using the clock generator (CG). The frequency of the built in oscillator is determined by an external resistor or can be optionally over-ridden by an input from an external oscillator. A data synchronizing signal ϕ_{SN} is provided to act as an oscilloscope trigger and as a Data Valid signal for exteral hardware.

COMPLETE MINIMUM SYSTEM



MEMORY IMPLEMENTATION FOR DEVELOPMENT SYSTEMS



PIN FUNCTIONS

Processor Signals

DAB 1-8
Bidirectional 8-lead precharged data bus, used in conjunction with address bus to implement 14-bit address word.

ADB 1-6
Push pull 6-lead address bus. This 6-bit word specifies the memory 'module' address and the 8-bit data bus specifies the 1 of 256 'intra module address'.

Processor Control Signals

CIO
Indicates direction of data flow on data bus.

CDA
Indicates if data bus is carrying data or address information.

CQZ
Used to select the Q counter or Z register for memory addressing.

CRA
Used to control the internal address stack.

Peripheral Signals

PEB 1-8
This is a bidirectional 8-bit latched input/output port with an open drain output configuration. In the case of the LP8000 chip the 8-bit port is organised such that only bits 5-8 are bidirectional bits 1-4 are only available as inputs. For all other chips in the family the peripheral interfaces are 8-bit all bidirectional.

Drive Requirements

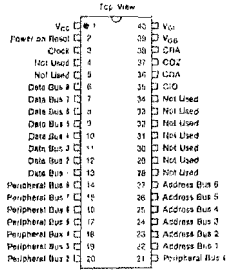
CLOCK
A single phase high level clock is required by the system and this would normally be provided by the LP1030 Clock Generator. The clock frequency used can be selected between 500 and 800KHz. With an 800KHz clock the machine provides a 5μSec machine cycle time.

RESET
This is a clock synchronized high level signal, normally provided by the LP1030 Clock Generator.

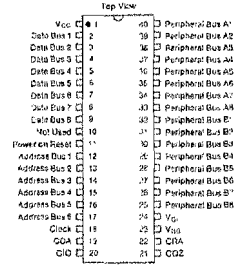
POWER
V_{CC} +5 Volt supply
V_{GG} 0 Volt (GND) supply
V_{BB} -12 Volt supply

PIN CONFIGURATIONS

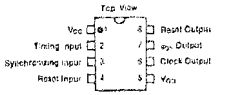
40 LEAD DUAL IN LINE
LP8000 LOGIC PROCESSOR



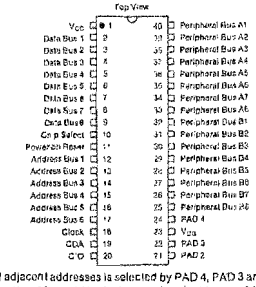
40 LEAD DUAL IN LINE
LP6000 PROGRAM MEMORY



8 LEAD DUAL IN LINE
LP1030 CLOCK GENERATOR

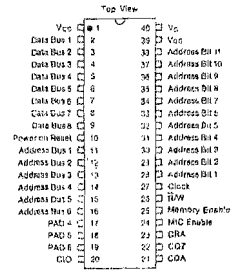


40 LEAD DUAL IN LINE
LP1010 INPUT/OUTPUT BUFFER



A pair of adjacent addresses is selected by PAD 4, PAD 3 and PAD 2 in the range 48 to 63, e.g. 011 selects peripheral addresses 54 and 55.

40 LEAD DUAL IN LINE
LP1000 MEMORY INTERFACE



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All pins with respect to V_{SS}	−20V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

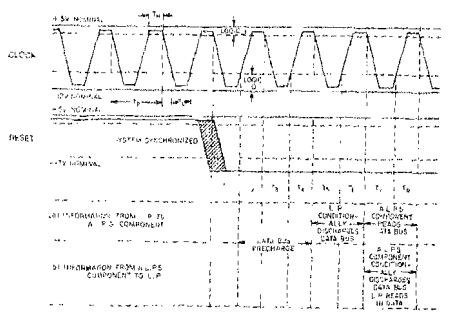
*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

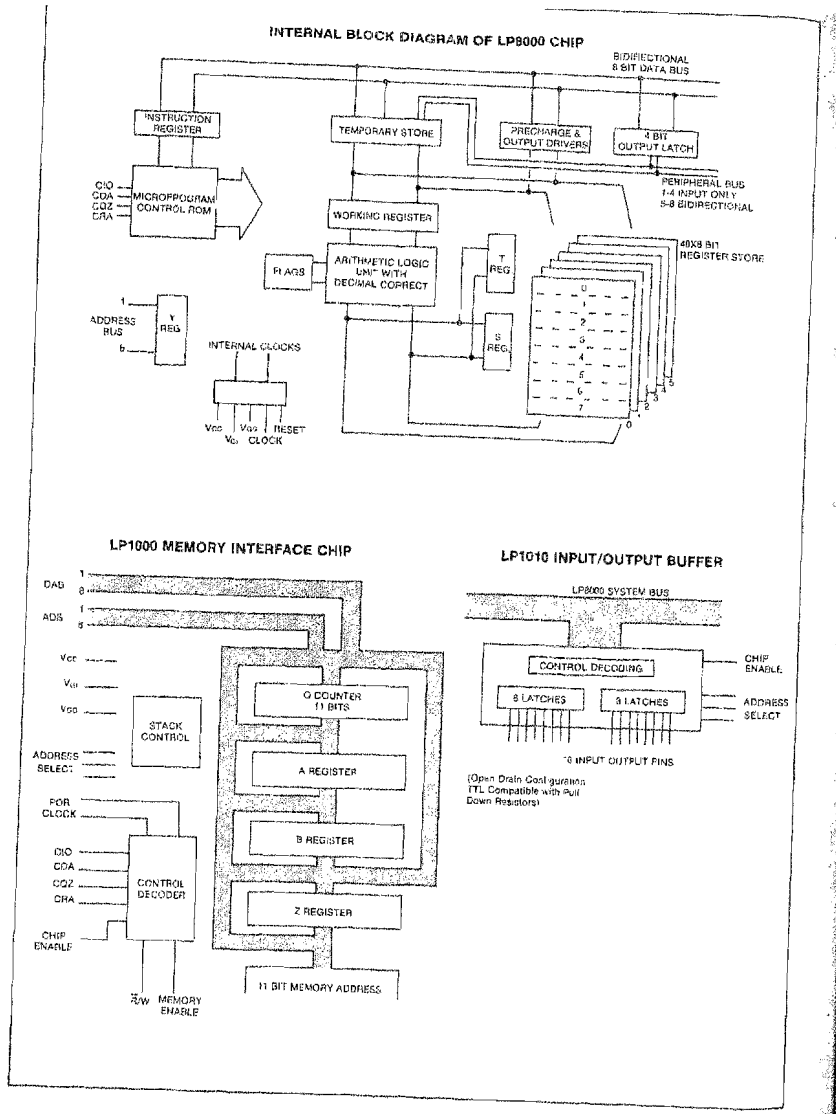
V_{CC} = +5V ±0.25V
V_{SS} = GND (substrate at V_{CC})
V_{DD} = −12V ±1V

Characteristic	Min	Max	Units	Conditions
Clock Frequency	400	600	KHz	
Machine Cycle Time	6.7	10	µs	
Clock and Reset Input				
Logic '1'	V_{CC} −1.5	—	Volts	
Logic '0'	—	−9.5	Volts	
Data Bus				
Input Conditions				
Logic '1'	V_{CC} −1.5	—	Volts	
Logic '0'	—	+0.8	Volts	
Output Conditions				
Logic '1'	V_{CC} −1.0	—	Volts	Capacitive load
Logic '0'	—	+0.4	Volts	only, maximum 275pF
Control & Address Bus				
Input Conditions				
Logic '0'	V_{CC} −1.5	—	Volts	
Logic '1'	—	−0.8	Volts	
Output Conditions				
Logic '0'	V_{CC} −1.0	—	Volts	Capacitive load
Logic '1'	—	−7.0	Volts	200pF
Peripheral Bus				
Input Conditions				
Logic '1'	V_{CC} −1.5	—	Volts	
Logic '0'	—	−0.8	Volts	
Output Conditions				
ON Current: LP1010	2	—	mA	$V_{OUT} = V_{CC}$ −1V
Other Devices	1	—	mA	$V_{OUT} = V_{CC}$ −1V
OFF Current: All Devices	—	1	µA	$V_{IN} = V_{SS}$ at 25°C
LP1000 Memory Controls (Address, R/W, Enable)				
Logic "1"	V_{CC}−1.0	—	Volts	I_{OH} = 100µA
Logic "0"	—	−0.4	Volts	I_{OL} = 0.5mA
Power Consumption: LP 8000	—	1000	mW	
All other devices	—	500	mW	

TIMING DIAGRAMS



	Mnemonics	Operation	Cycles	Comments
INTERNAL REGISTER INSTRUCTION	LAR	Load Accumulator from Register	1	These instructions are used to manipulate the contents of the accumulator with one of the 48 internal registers. They have a four bit argument and direct addressing is assumed for 0-11 but indirect for 12, 13 and 14. For indirect addressing the register address is held in S,T. Argument 12 gives register pointed to by S & T; 13 gives the same then S is decremented. 14 also addresses via S & T and then S is incremented
	SAR	Store Accumulator in Register	1	
	DEC	Decrement Register by one *	1	
	ADR	BCD Add Accumulator with Register *	2	
	BAD	Binary Add Accumulator with Register	1	
	AND	Logical AND Accumulator with Register	1	
	EOR	Exclusive OR Accumulator with Register	1	
		*The results of these operations are stored in the respective register. The result of all other operations is stored in the accumulator		
REGISTERS S&T	LSS	Load S with Short (3-bit) Literal	1	
	LST	Load T with Short (3-bit) Literal	1	
	SAT	Store Accumulator in Register T	1	Lower order bits (1-3) of accumulator are copied in register T
	SST	Store Accumulator in Registers S & T	1	Bits (1-3) of accumulator copied in register S bits (4-6) copied in register T
EXTERNAL REFERENCE INSTRUCTIONS	LAL	Load Accumulator with 8-bit Literal	2	The lower six bits of the X and Y registers are used to address 256-bit modules of data and program respectively. The 8-bit data bus is used to provide the intra-module address. These three instructions respectively fetch or store data using the address in the register to specify the module
	LAS	Load Accumulator with 4-bit Literal	1	
	ALL	Logical AND, Accumulator with 8-bit Literal	2	
	ORL	Logical OR, Accumulator with 8-bit Literal	2	
	EOL	Exclusive OR, Accumulator with 8-bit Literal	2	
	ALA	Add Accumulator with 8-bit Literal	2	
	CMP	Compare Accumulator with 8-bit Literal	2	
	LIX	Load Accumulator Indirect Module X	4	
	LIY	Load Accumulator Indirect Module Y	4	
	SIX	Store Accumulator Indirect Module X	3	
SIMULATOR & ADDRESS CONTROL REGISTERS	SAX	Store Accumulator in Register X	1	Used in normal register operation and also for setting up module addresses for program and data manipulation.
	SAY	Store Accumulator in Register Y	1	
	LAX	Load Accumulator from Register X	1	
	LAY	Load Accumulator from Register Y	1	
	SZX	Store Accumulator in Z Register Module X	3	Used to set Q Counter or Z register of required module
	SZY	Store Accumulator in Z Register Module Y	3	
	SQX	Store Accumulator in Q Counter Module X	3	The Y register points to the active program module, the X register points to an alternative module or a data space.
	SQY	Store Accumulator in Q Counter Module Y	3	
	SAV	Store Accumulator in Register V	1	These four instructions allow direct access to the internal registers which are masked by the operand code used for indirect addressing i.e. 12, 13.
	SAW	Store Accumulator in Register W	1	
	LAV	Load Accumulator in Register V	1	
	LAW	Load Accumulator in Register W	1	
	CLA	Clear Accumulator to Zeros	1	
SHIFT	LSA	Shift Accumulator Left 1-bit	1	Carry Flag set unconditionally
	RSA	Shift Accumulator Right 1-bit	1	Carry Flag cleared unconditionally
	LSN	Shift Accumulator Left 4-bits	1	
	RSN	Shift Accumulator Right 4-bits	1	
INPUT/OUTPUT INSTRUCTIONS	LAM	Load Accumulator from Module Direct	2	The indirect I/O operations use the X register for module addressing. The SAX instruction is used to set up the system for the indirect mode.
	SAM	Store Accumulator in Module Direct	3	
	LIM	Load Accumulator from Module Indirect	4	
	SIM	Store Accumulator in Module Indirect	3	
JUMP WITHIN2K PAGE	JMP	Jump Unconditional	3	3 if true, 2 if false. Used to sequence through a 'page' of internal registers.
	JIZ	Jump if all Zeros	3/2	
	JNZ	Jump if not all zeros	3/2	
	JIP	Jump if sign bit positive	3/2	
	JRS	Jump if Register S not equal to seven	3/2	
	JCS	Jump if carry bit set	3/2	
	JCN	Jump if carry bit not set	3/2	
SUBROUTINE INSTRUCTIONS	GOS	Go to Subroutine	3	Program counter automatically stored in memory chip stack.
	RET	Return from Subroutine	2	



DEVELOPMENT FAMILY

A production system may consist of only a Logic Processor, LP8000, and ROM, LP6000, (plus Clock Generator, LP1030). However, the practical development family which complements the LP8000 allows the user to implement his hardware and software in a real time replacement mode for his final mask programmed product. LP1000 and LP1010 parts, plus PROM, can directly replace the LP6000 ROM. Indeed the development family may well be used as the complete solution for short run multi-variety systems

DEVELOPMENT SUPPORT

Circuits

LP 8000 systems use only a small number of integrated circuits for cost effective implementation. For development and pre-production LP 1000 (Memory Interface Circuit) and LP 1010 (Input-Output Buffer) can be used with PROM, EAROM or RAM to replace the final mask-programmed ROM (see diagram). The system using PROM or EAROM behaves identically with the final mask-programmed ROM version. When the program has been proved, the LP1000, LP1010, and PROM/EAROM can all be replaced by LP 6000 to give the final low-cost system using perhaps as few as two 40 lead DIPs (LP 8000 + LP 6000), and one 8 lead DIP (LP 1030). Small production runs, or systems needing extensive RAM memory can remain with LP 1000 and LP 1010.

Prototype System

To simplify hardware and softwsre development and help speed the users product design cycle time, a complete hardware prototype development system is available to support the Series 8000 family. The GIC 8000 Microcomputer System provides a test bed for user designed interfaces and related hardware as well as a program preparation facility with resident, on-line hardware and software debug aids. The users program can be tested and modified under real time operating conditions. To make program development fast and efficient, peripheral interfaces and their related software including TTY high speed reader, high speed punch and serial line printer are included on the prototype system. In addition, all of the card level modules of this system, ranging from complete microcomputers to memory or I/O modules, are available on an OEM basis for further system integration.

Software

For pure program development to check the flow of instructions, a complete assembler and simulator written in FORTRAN IV is available for operation on minicomputer systems or on internal or external time share networks

Manual

A manual describing complete hardware aspects of Series 8000, and details of the program preparation software is available from all General Instrument Microelectronics Sales Offices, Agencies, and Distributors

Series 8000 Cross Assembler — Program Specification

INTRODUCTION

The Symbolic Cross Assembler is capable of converting programs written in Series 8000 symbolic assembly language into a tape format suitable for loading into the prototyping system. The program runs on a General Instrument GIMINI prototyping system with 8K of 16 bit RAM memory using either a teletype or reader/punch for input/output operations. The symbolic assembly language used by this cross-assembler is an extension of the original specification and closely resembles the language format of the Series 1600 Assembler.

FEATURES

The Symbolic Cross Assembler provides the following major features:

- Symbolic language representation of all instructions and data
- Up to 250 user defined names for variables/registers.
- Binary, octal, decimal, hex and character representations for literals
- Arithmetic evaluation of operand expressions.
- Assembly directives for
  - —Controlling memory allocation
  - —Defining character strings
  - —Specifying input/output options
  - —Establishing and controlling conditional assemblies
- Program listings - which are optional
- Comprehensive error detection and diagnostics

OPERATION

The Symbolic Cross Assembler converts symbolic source programs into machine code format in a two pass process. During the first pass through the source file, all user specified symbols are placed in a symbol table containing the symbol, its value, and several other attributes. During the second pass through the source file, symbolic instruction mnemonics are translated, symbol references resolved, errors diagnosed, a machine code file generated, and an optional program listing produced.

The machine code file produced by the Cross Assembler is an absolute load module that can be punched on paper tape for subsequent loading in a GIC8000 microcomputer system by the resident loader. Both standard and modified hexadecimal codes can be generated.

8-Bit Microcomputer System

FEATURES

- Built around the General Instrument LP8000 Microprocessor
- Complete microcomputer system to enable rapid program development
- Up to 16K × 8 of memory space
- PROM resident system monitor
- Load and dump routines for Teletype, Reader, Punch, V.D.U and Line Printer
- Examine/Store all 48 internal CPU registers, user memory locations and user I/O ports
- Auto increment for examining and storing in sequential locations.
- 'Breakpoint' facility for halting execution of user program at specified address
- 'Start from address' facility for starting execution of user program at any specified address
- Up to 6K × 8 of user RAM or PROM memory
- Up to 15 8-bit user I/O ports
- 8-bit data and 14-bit address displays
- Internal power supplies

DESCRIPTION

The GIC8000 Microcomputer System is a complete development system designed to support the General Instrument Series 8000 family. It provides a test bed for user designed interfaces and related hardware as well as a program preparation facility with resident, on-line hardware and software de-bug aids. It also allows the user program to be tested and modified under real time operating conditions. To make program development fast and efficient, peripheral interfaces and their related software including TTY, high speed reader, high speed punch and serial line printer are included. In addition all the cards of the system, ranging from complete microcomputers to memory or I/O modules are available on an OEM basis for further system integration.

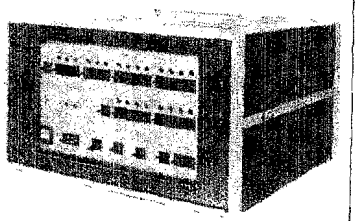
The GIC8000 is of modular design, the basic hardware consisting of a steel cabinet 12 position card file, front panel control console, power supply and 5 plug-in cards;

MC8000 MICROCOMPUTER MODULE (INCLUDING USER IOB)
OS8000 SYSTEM MONITOR MODULE
IO8000 TTY/RDR-PCH MODULE
RM8000 2K × 8 USER RAM MODULE
CC8000 FRONT PANEL DRIVER MODULE

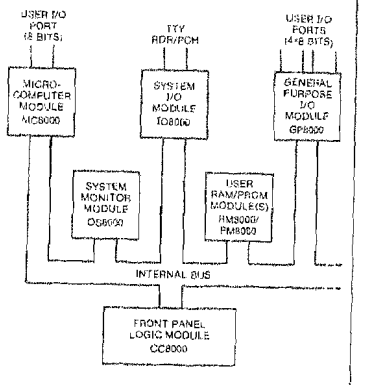
In addition, the following modules are also available

GP8000 GENERAL PURPOSE I/O MODULE
EX8000 EXTENDER CARD
PM8000 2K × 8 USER PROM MODULE

GIC8000 MICROCOMPUTER



BLOCK DIAGRAM



OPERATING MODES

The machine can operate in either SYSTEM or USER mode. In SYSTEM mode, the PROM resident System Monitor program controls all the operational features of the machine and provides a wide range of monitoring and editing facilities which can be used to rapidly develop user programs. In USER mode, the machine is under the exclusive control of the user program and can therefore be used as a test bed for user defined interfaces and related hardware as well as testing the program itself.

OPERATIONAL FACILITIES

Load and Dump Tapes

Load and dump routines allow user program tapes to be read and dumped from a standard teletype, teletype compatible V.D.U., high speed reader, high speed punch or serial line printer. Ready and fault lamps on the front panel indicate the status of the machine during these operations. In dump mode, the whole or only certain specified areas of user memory can be punched out.

Examine Memory, I/O Modules and CPU Registers

The user area of memory (up to 6K × 8), all user I/O modules and all 48 internal CPU registers can be examined from the front panel. A 14 bit address register and an 8 bit data register are used to set and display address and data information respectively. To allow sequential locations to be rapidly examined, a special increment key has also been provided.

Start Execution at Specified Address

Normally, execution of the user program starts from line zero. However in certain circumstances this may not be convenient and so a start from address facility has been incorporated. This allows the user to start execution of his program at any specified address in it and is controlled by a special key on the front panel.

Store in Memory, I/O Modules and CPU Registers

Data can also be written into user memory, user I/O modules and CPU registers via the same address and data registers. Again, the auto increment facility is available to rapidly store data in sequential locations.

Stop Execution at Specified Address

Execution of the user program can be stopped by operating MASTER RESET to return control of the machine to the System Monitor Program. However as it is not possible to define exactly where execution ceases using this method, a 'Breakpoint' facility has been provided. This allows the user to execute his program up to a specified point and then automatically switch into Monitor mode where the full range of monitoring and editing facilities can be used.

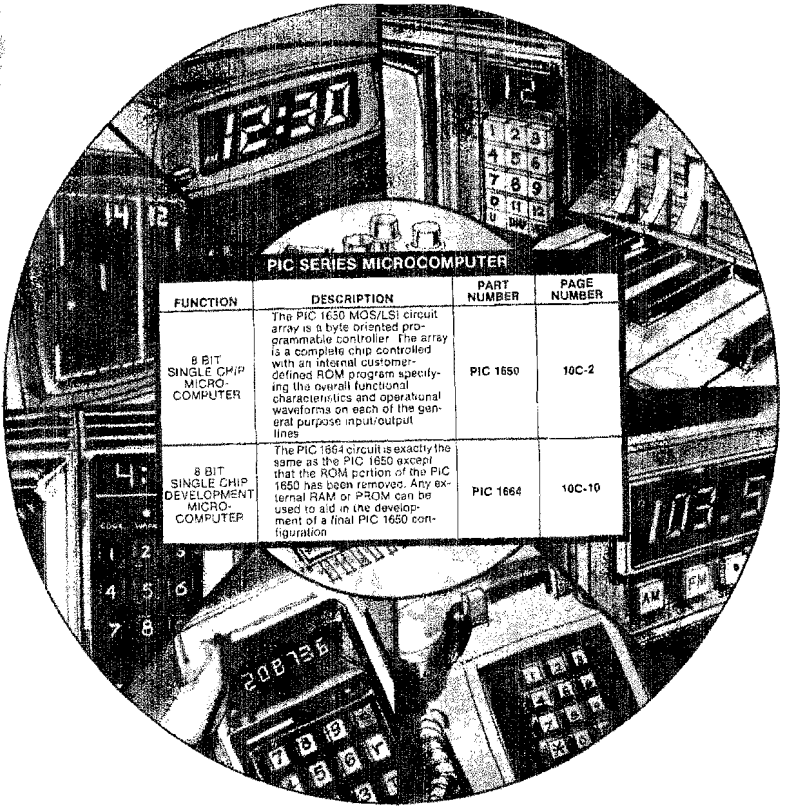
USER MEMORY MODULES

The total memory area of 16K is divided into 8 pages of 2K and each page is further sub-divided into 8 modules of 256 words. The bottom three pages, 0, 1 and 2, are available to the user and can consist of up to 3, plug-in static RAM or UV Erasable PROM cards or any combination of the two. To prevent accidental corruption of the RAM modules during development, each card is provided with a Memory Freeze switch which effectively converts them to volatile ROM memory. One 2K × 8 RAM module is normally supplied with the basic kit.

USER I/O MODULES

The top 15 modules in memory are allocated for user as user I/O ports. Each port is 8 bits wide and occupies one module address. The microcomputer module has two IOB's, one of which is used by the LP8000 microcomputer chip but the other is available to the user. If the user requires additional I/O ports, then General Purpose I/O Modules can be added as necessary.

Each General Purpose I/O Module supports two, dual 8 bit IOB's giving the user four, individually addressable 8 bit I/O ports. I.e. 32 bi-directional lines. Pull-down resistors fitted on the card make the I/O lines TTL compatible (one load). In addition up to eight 16 pin DIL packages can be added to the cards for user designed circuitry. All I/O lines enter the machine via sockets on the rear panel.



PIC SERIES MICROCOMPUTER

FUNCTION	DESCRIPTION	PART NUMBER	PAGE NUMBER
8 BIT SINGLE CHIP MICRO-COMPUTER	The PIC 1650 MOS/LSI circuit array is a byte oriented programmable controller. The array is a complete chip controlled with an internal customer-defined ROM program specifying the overall functional characteristics and operational waveforms on each of the general purpose input/output lines	PIC 1650	10C-2
8 BIT SINGLE CHIP DEVELOPMENT MICRO-COMPUTER	The PIC 1664 circuit is exactly the same as the PIC 1650 except that the ROM portion of the PIC 1650 has been removed. Any external RAM or PROM can be used to aid in the development of a final PIC 1650 configuration	PIC 1664	10C-10

PIC SERIES MICROCOMPUTER

MICRO ELECTRONICS

Programmable Intelligent Computer

FEATURES

- User Programmable
- Intelligent Controller for Stand-Alone Applications
- 32 8-Bit Registers
- 512 × 12-Bit ROM for Program
- Arithmetic Logic Unit
- 4 Sets of 8 User Defined TTL-compatible Input/Output Lines.
- Real Time Clock Counter
- Self contained Oscillator
- Access to RAM Registers inherent in instruction.

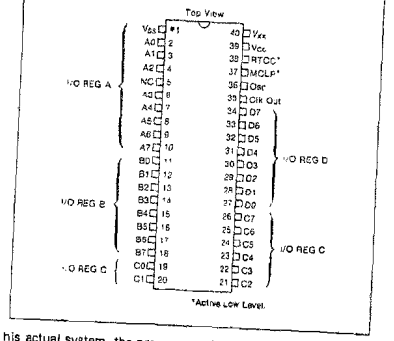
DESCRIPTION

The PIC1650 MOS/LSI circuit array is a byte oriented programmable controller designed to satisfy the requirements for a low-cost, stand-alone 8-bit micro-computer. The array is a complete chip controlled with an internal customer-defined ROM program specifying the overall functional characteristics and operational waveforms on each of the general purpose input/output lines. The array can be programmed to scan keyboards, drive multiplexed displays, control vending machines, control traffic lights, control printers and to control automatic gasoline pumps. Since it contains ROM, RAM, I/O as well as the central processing unit on one device, the PIC1650 is truly a complete 8-bit micro-computer on one chip.

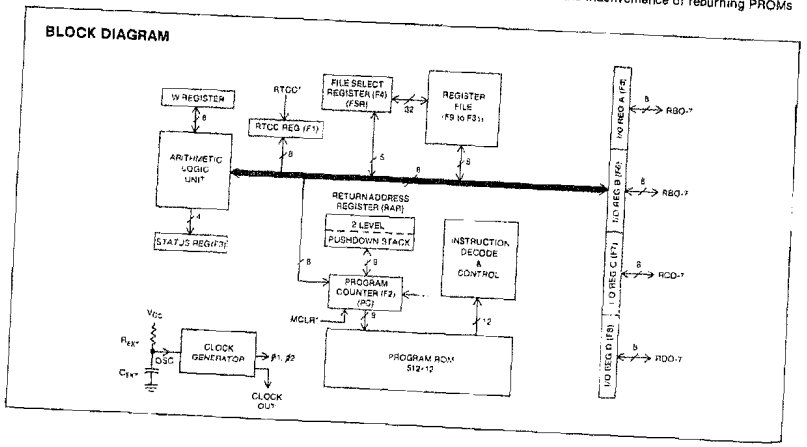
The PIC1650 is fabricated with N-Channel Ion Implant technology resulting in a high performance product with proven reliability and Production history. Only a single +5 volt power supply is required for operation, and an on-chip oscillator provides the operating clock with only an external R/C network to establish the frequency. Inputs and outputs are TTL compatible. The PIC1650 is supplied in a 40-pin dual-in-line package.

The PIC product family (PIC1650 and all extensions) is supported by an extensive software and hardware package. The software package includes Cross Assembler/Simulator programs designed to run on the large machine, on time share and minicomputer system levels. The hardware package includes a prototype TTL Emulator Board with which the user can verify, in his actual system, the program in either RAM or PROM before committing it to mask tooling. For added flexibility, the board can be interfaced into the GIMINI developmental system for conversational capability via a terminal with the PIC TTL Emulator's RAM memory. The PIC program is stored in RAM on the PIC Emulator board as memory as part of the CP1600 microprocessor address space. Thus, on-line changes in code can be implemented without the inconvenience of reburning PROMs

PIN CONFIGURATION
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

Signal	Function
OSC (input)	Oscillator input. This signal can be driven by an external oscillator if a precise frequency of operation is required or an external R/C network can be used to set the frequency of operation of the internal clock generator. The maximum oscillator frequency is 1MHz
RTCC* (input)	Real Time Clock Counter. Used by the microprogram to keep track of elapsed time between events. The maximum RTCC* frequency is 250KHz. This register can be loaded and read by the program.
RA0-7, RB0-7, RC0-7, RD0-7 (input/output)	User programmable input/output lines. These lines can be inputs and/or outputs and are under direct control of the program.
MCLR* (input)	Master Clear. Used to initialize the internal ROM program to address 777_8. Should be held low at least 20 μs past the time when the power supply is valid.
CLOCK (output)	A signal derived from the internal oscillator. Used by external devices to synchronize themselves to PIC timing.

ARCHITECTURAL DESCRIPTION

The firmware architecture of the PIC1650 microcomputer is based on a register file concept with very simple, low level, commands designed to emphasize bit, byte, and register transfer operations. The primary purpose of the PIC is to perform logical processing, basic code conversions, formatting, and to generate fundamental timing and control signals for I/O devices. The instruction set also supports computing functions as well as these control and interface functions.

Internally, the PIC1650 is composed of three functional elements connected together by a single bidirectional bus: the Register File composed of 32 addressable 8-bit registers, an Arithmetic Logic Unit, and a Control ROM composed of 512 program words each 12 bits in width.

The Register File is divided into two functional groups: operational registers and general registers. The operational registers are addressed as F0 to F8 (the first 9 of the total of 32 file registers) and include, among others, the Real Time Clock Counter Register, the Status Register, the Program Counter (PC), and I/O Registers A, B, C and D (RA, RB, RC and RD). The general registers are addressed as F9 to F31 and are used for data and control information under command of the instructions.

The Logic Unit contains one temporary working register or accumulator (W Register) and gating to perform Boolean functions between data held in the working register and any file register.

The Control ROM contains the operational program for the rest of the logic within the controller. Sequencing of a micro-instructions is controlled via the Program Counter (PC) which automatically increments to execute in-line programs. Program control operations can be performed by Bit Test and Skip instructions. Jump instructions, or loading computed addresses into the PC. In addition, an on-chip pushdown stack is employed with the return address register serving as the top element of the stack. This permits easy to use subroutine nesting. Application of the +5V power supply initializes the ROM microprogram to address 777_8.

REGISTER FILE ARRANGEMENT

File	Function
F0	Not a physically implemented register. F0 calls for the contents of the File Select Register (low order 5 bits) to be used to select a file register. F0 is thus useful as an indirect address pointer. For example, W+F0 → W will add the contents of the file register pointed to by the FSR (F4) to W and place the result in W
F1	Real Time Clock Counter Register. This register can be loaded and read by the microprogram. Clock keeps counting up after zero is reached.
F2	Program Counter (PC). The PC is automatically incremented and can be written into; e.g., MOVWF F2 if cannot be read, however.
F3	Status Word Register. The bits in this register can be set or cleared only by the Bit Set and Bit Clear instructions; they cannot be altered by other commands operating on F3.

(4)	(1)	(1)	(1)	(1)	
1	PC9	Z	DC	C	:F3

PC9. Tenth bit of PC for future use. Future ROM space of 512-1023 can be addressed with this bit set.

C (Carry): Stores the carry out on arithmetic operations, and acts as a bit link on rotate operations. This bit is set high on an SUBWF instruction if the addition of f, the one's complement of W, and a 1 results in a carry

DC (Digit Carry): Stores the carry out of low order digit on arithmetic operation. This bit is set high on a SUBWF instruction if the addition of f, the one's complement of W, and a 1 results in a carry from the low order digit

Z (Zero): Set if the result of the arithmetic operations is zero.

F4	File Select Register (FSR). Low order 5 bits only are used. The FSR is used in generating effective file register addresses under program control. When accessed as a directly addressed file, the upper 3 bits read as a logic "1".
F5	I/O Register A (RA)
F6	I/O Register B (RB)
F7	I/O Register C (RC)
F8	I/O Register D (RD)

10C

Instruction Set Summary

For an oscillator frequency of 1MHz, the instruction execution time is 4 μsec, except if a conditional test is true or if the PC register is changed as a result of an instruction. In these two cases, the instruction execution time is 8 μsec

In the following PIC instruction descriptions "k" represents an eight bit constant or literal value, "f" represents a file register designator and "d" represents a destination designator. The file register designator specifies which one of the 32 PIC file registers is to be utilized by the instruction. The destination designator specifies where the result of the operation performed by the instruction is to be placed. If "d" is zero, the result is placed in the PIC W register. If "d" is one, the result is returned to the file register specified in the instruction. If the "d" operand is omitted, the f register is assumed as the destination. "f" and "d" may be numbers, characters, or symbols as described in the PIC Assembler and PIC Simulator instructions. "C" represents the carry bit, "Z" represents the zero bit, and "DC" represents the digit carry bit

GENERAL FILE REGISTER OPERATIONS

(6)	(1)	(5)
OP CODE	d	f (FILE #)

for d = 0, f→W
d = 1, f→f

Instruction (Octal)				Name	Syntax			Operation	Status
000000	0	00000	(0000)	No Operation	NOP	–	–	–	–
000000	1	fffff	(0040)	Move W to f *	MOVWF	f		W→f	–
000001	0	fffff	(0100)	Clear W	CLRW	–		0→W	Z
000001	1	fffff	(0140)	Clear f	CLRF	f		0→f	Z
000010	d	fffff	(0200)	Subtract W from f	SUBWF	f, d		f - W→d	C,DC,Z
000011	d	fffff	(0300)	Decrement f	DECF	f, d		f - 1→d	Z
000100	d	fffff	(0400)	Inclusive OR W and f	IORWF	f, d		W∨f→d	Z
000101	d	fffff	(0500)	AND W and f	ANDWF	f, d		W∧f→d	Z
000110	d	fffff	(0600)	Exclusive OR W and f	XORWF	f, d		W∨f→d	Z
000111	d	fffff	(0700)	Add W and f	ADDWF	f d		W+f→d	C,DC,Z
001000	d	fffff	(1000)	Move f	MOVF	f, d		f→d	Z
001001	d	fffff	(1100)	Complement f	COMF	f, d		$\bar{f}$→d	Z
001010	d	fffff	(1200)	Increment f	INCF	f, d		f+1→d	Z
001011	d	fffff	(1300)	Decrement f Skip if Zero	DECFSZ	f o		f - 1→d skip if Zero	–
001100	d	fffff	(1400)	Rotate Right f	RRF	f o		f(n)→d(n-1), f(0)→C, C→d(7)	C
001101	d	fffff	(1500)	Rotate Left f	RLF	f. d		f(n)→d(n+1), f(7)→C C→d(0)	C
001110	d	fffff	(1600)	Swap halves f	SWAPF	f d		f(0-3)⇄f(4-7)→d	–
001111	d	fffff	(1700)	Increment f, Skip if Zero	INCFSZ	f o		f+1→d skip if zero	–

BIT LEVEL FILE REGISTER OPERATIONS

(4)	(3)	(5)
OP CODE	b (BIT #)	f (FILE #)

Instruction (Octal)				Name	Syntax			Operation	Status
0100	bbb	fffff	(2000)	Bit Clear f	BCF	f, b		0→f(b)	–
0101	bbb	fffff	(2400)	Bit Set f	BSF	f, b		1→f(b)	–
0110	bbb	fffff	(3000)	Bit Test f, Skip if Clear	BTFSC	f, b		Bit Test f(b) skip if clear	–
0111	bbb	fffff	(3400)	Bit Test f, Skip if Set	BTFSS	f, b		Bit Test f(b) skip if set	–

LITERAL AND CONTROL OPERATIONS

(4)	(8)
OP CODE	I (LITERAL)

Instruction (Octal)				Name	Syntax			Operation	Status
1000	k k k k k k k k		(4000)	Return	RET	–		0 → W, RAR → PC	–
1000	k k k k k k k k		(4000)	Return and place Literal in W	RETLW	k		k → W, RAR → PC	–
1001	k k k k k k k k		(4400)	Call subroutine *	CALL	k		PC → RAR, k → PC	–
101x	k k k k k k k k		(5X00)**	Go To address	GOTO	k		k → PC	–
1100	k k k k k k k k		(6000)	Move Literal to W	MOVLW	k		k→W	–
1101	k k k k k k k k		(6400)	Inclusive OR Literal and W	IORLW	k		k∨W→W	Z
1110	k k k k k k k k		(7000)	AND Literal and W	ANDLW	k		k∧W →W	Z
1111	k k k k k k k k		(7400)	Exclusive OR Literal and W	XORLW	k		k∀W→W	Z

*The 9th bit of the program counter in the PIC1650 is zero for a CALL and a MOVWF F2. Therefore, subroutines must be located in page 0. However, subroutines can be called from page 0 or page 1 since the RAR is 9 bits wide. (Page 0: 0-255, Page 1: 256-511).
**If X = 0, the address is in page 0; if X = 1, the address is in page 1. The PIC assembler takes care of assigning the correct op codes.

OTHER INSTRUCTION MNEMONICS REGONIZED BY THE PIC1650 ASSEMBLER

Instruction (Octal)		Name	Syntax	Equivalent Operation(s)	Status
0100 000 00011	(2003)	Clear Carry	CLRC	BCF3, 0	–
0101 000 00011	(2403)	Set Carry	SETC	BSF3,0	–
0100 001 00011	(2043)	Clear Digit Carry	CLRDC	BCF3,1	–
0101 001 00011	(2443)	Set Digit Carry	SETDC	BSF3,1	–
0100 010 00011	(2103)	Clear Zero	CLRZ	BCF3, 2	–
0101 010 00011	(2503)	Set Zero	SETZ	BSF3,2	–
0111 000 00011	(3403)	Skip on Carry	SKPC	BTFSS3,0	–
0110 000 00011	(3003)	Skip on No Carry	SKPNC	BTFSC3,0	–
0111 001 00011	(3443)	Skip on Digit Carry	SKPDC	BTFSS3,1	–
0110 001 00011	(3043)	Skip on No Digit Carry	SKPNDC	BTFSC3, 1	–
0111 010 00011	(3503)	Skip on Zero	SKPZ	BTFSS3, 2	–
0110 010 00011	(3103)	Skip on No Zero	SKPNZ	BTFSC3, 2	–
001000 1 fffff	(1040)	Test File	TSTF f	MOVF f, 1	Z
001000 0 fffff	(1000)	Move File to W	MOVFW f	MOVF f, 0	Z
001001 1 fffff	(1140)	Negate File	NEGF, f,d	COMF f, 1 INCF f, d	Z
001010 d fffff	(1200)	Add Carry to File	ADDCF f, d	BTFSC 3,0 INCF f, d	Z
011000 0 00011 001010 d fffff	(3003) (1200)	Subtract Carry from File	SUBCF f,d	BTFSC 3,0 DECF f, d	Z
011000 0 00011 000011 d fffff	(3003) (0300)	Add Digit Carry to File	ADDDCF f,d	BTFSG 3,1 INCF f,d	Z
011000 1 00011 001010 d fffff	(3043) (1200)	Subtract Digit Carry from File	SUBDCF f,d	BTFSC 3,1 DECF f,d	Z
011000 1 00011 000011 d fffff	(3043) (0300)	Branch	S K	GO TO K	–
101× kkkkkkkk	(5×00)	Branch on Carry	BC K	BTFSC 3,0 GO TO K	–
0110 00000011 101× kkkkkkkk	(3003) (5×00)	Branch on No Carry	BNC K	BTFSS 3,0 GO TO K	–
0111 00000011 101× kkkkkkkk	(3403) (5×00)	Branch on Digit Carry	BDC K	BTFSG 3,1 GO TO K	–
0110 00100011 101× kkkkkkkk	(3043) (5×00)	Branch on No Digit Carry	BNDC K	BTFSS 3,1 GO TO K	–
0111 00100011 101× kkkkkkkk	(3443) (5×00)	Branch on Zero	BZ K	BTFSC 3,2 GO TO K	–
0110 01000011 101× kkkkkkkk	(3103) (5×00)	Branch on No Zero	BNZ K	BTFSS 3,2 GO TO K	–
0111 01000011 101× kkkkkkkk	(3503) (5×00)				

If x = 0, address is in page 0.
If x = 1, address is in page 1

10C

Sample Programs

In the following program steps, .dddd means literals, in decimal form, otherwise they are in octal form.

I OBJECTIVE: To display the file pointed to by F31 via I/O post A (F5). Assume .20 in F31 and .100 in F20.

Hence, the following program will display .100 via F5.

Program steps	Description
MOVF 31, W	Move the contents of F31 to the working register W. After execution W contains .20.
MOVWF 4	Move the contents of W to FSR (F4). After execution F4 contains .20
MOVF 0, W	Move the contents of the file pointed to by FSR, that is, the contents of F20, to W. Thus W contains .100 after execution.
MOVWF 5	Move the contents of W to F5. Hence .100 is in F5 now.

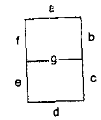
II OBJECTIVE: To compare F31 to a constant, if equal GOTO OK, if not equal GOTO NO

Program Steps	Description
MOVF .31, W	Move the contents of F31 to the working register W
XORLW CONST	Exclusive Oring, bit by bit, the contents of W and the literal CONSTANT. If the are equal, all zero bits will result in W and the second bit in the status register (F3) will be set.
BTFSS 3,2	If the second bit in F3 is one, skip the next step.
GOTO NO	They are not equal.
GOTO OK	They are equal.

III OBJECTIVE: To clear files F5 to F31

Program Steps	Description
MOVLW 4	Move the literal 4 to the working register W.
MOVWF 4	Move the literal 4 from W to the FSR (F4). These two steps initialize the pointer F4 to 4.
LPI INCF 4,5	Increment the contents of FSR by one. This is the same as saying that the pointer points to next file.
CLRF 0,F	Clear the contents of the file pointed to by FSR.
MOVLW .255	To sense the end of the file, which is F31, move the literal .255 to working register W. The literal .255 is used since the top three bits of F4 are read as one.
XORWF 4, W	Compare bit by bit the contents of FSR and W. If they are equal, the second bit in the status register (F3) will be set.
BTFSS 3,2	If they are not equal, go back to the step laballed LPI, otherwise stop
GOTO LPI	
END	

IV OBJECTIVE: BCD to 7-Segment Code Conversion



Digit is displayed in either I/O Register 5, 6, 7, or 8. F20 contains the BCD numbers

Label	Program steps		Description
	MOVLW	TBLSTR	Starting address of table
	ADDWF	20, W	Add BCD number as offset to Tablestart
	CALL	CONVRT	Obtain converted code
	MOVWF	5	Move the 7-segment code to the file pointed to by the file select register
	—		
	—		
	—		
	—		
	—		
	—		
	—		
	—		
	—		
	—		
	—		
	—		
CONVRT	MOVWF	2	Move the computed address into the PC
TBLSTR	RETLW	B'1111110'	0 in seven segment (abcdefg)
	RETLW	B'0110000'	1 in seven segment (abcdefg)
	RETLW	B'1101101'	2 in seven segment (abcdefg)
	RETLW	B'1111001'	3 in seven segment (abcdefg)
	RETLW	B'0110011'	4 in seven segment (abcdefg)
	RETLW	B'1011011	5 in seven segment (abcdefg)
	RETLW	B'0011111'	6 in seven segment (abcdefg)
	RETLW	B'1110000'	7 in seven segment (abcdefg)
	RETLW	B'1111111'	8 in seven segment (abcdefg)
	RETLW	B'1110011'	9 in seven segment (abcdefg)

10C

Electrical Characteristics

Operating Parameters

V_{CC} Voltage = +5 volts ± 5%
V_{XX} Voltage = +4.75V to +10.0V
I_{CC} Current = 50 ma typical; 75 ma max
Temperature = 0°C to +50°C
Storage Temperature Range: -55°C to +150°C

D.C. Parameters

Input Logic "1"	V_{IH} = 2.4V min
Input Logic "0"	V_{IL} = 0.8V max.
Input Leakage	I_{IL} = 15 µA max.
Input Capacitance	C_I = 5 pF max.
Output Logic "1"	V_{OH} = 2.4V min. @ 100 µA
Output Logic "0"	V_{OL} = 0.4V max. @ 1.8 mA
Output Leakage	I_{OL} = ± 5 µA max.
Output Capacitance	C_O = 10 pF max

A.C. Parameters

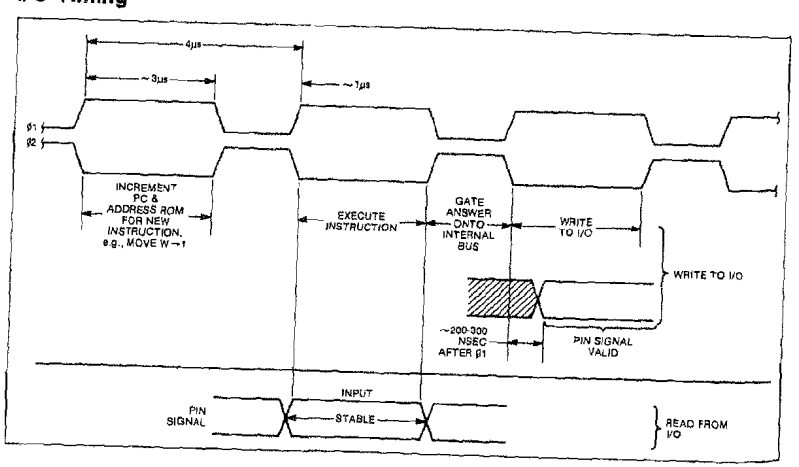
OSC Frequency	1 MHz
RTCC* Frequency	250 KC

LED Direct Drive

V_{XX} drives the gate of the output buffer, allowing adjustment of LED drive capability:

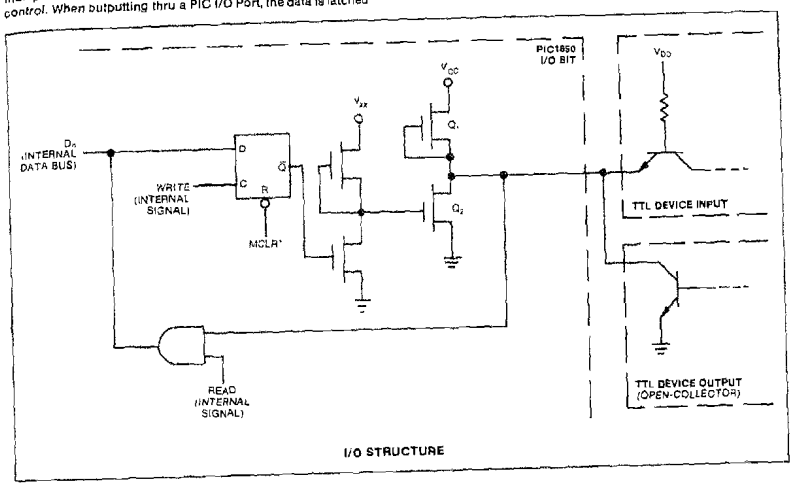
V_{XX}	V_{OUT}	I_{SINK} (typ.)
5V	0.4V	2.5mA
5V	0.7V	4.2mA
10V	0.4V	5.8mA
10V	0.7V	10.0mA
10V	1.0V	14.1mA

I/O Timing



I/O Interfacing

The equivalent circuit for an I/O port bit is shown below as it would interface with either the input of a TTL device (CPU chip is outputting) or the output of an open collector TTL device (CPU chip is inputting). Each I/O port bit can be individually time multiplexed between input and output functions under software control. When outputting thru a PIC I/O Port, the data is latched at the port and the pin can be connected directly to a TTL gate input. When inputting data thru an I/O Port, the port latch must first be set to a logic "1" level under program control. This turns off Q_2, allowing the TTL open collector device to drive the pad, pulled up by Q_1, which can source about 100µA.



I/O STRUCTURE

PRELIMINARY INFORMATION

Programmable Intelligent Computer Development Circuit

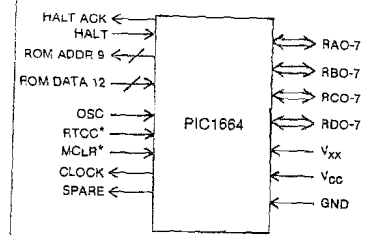
FEATURES

- PIC1650 computer with ROM removed
- Useful for engineering prototyping and field trial demonstrations
- PIC1650's ROM address & data lines brought out to pins
- PIC1650's ROM can be replaced by external RAM or PROM
- PIC1650 can be single stepped or stopped via the halt pin.

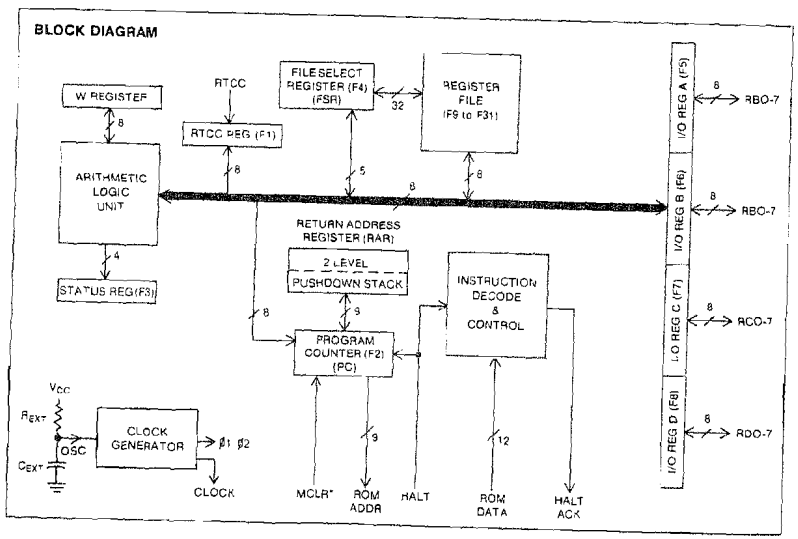
DESCRIPTION

The PIC1664 MOS/LSI circuit array is exactly the same as PIC1650 except for the fact that the ROM is removed and that the ROM address and data lines are brought out, resulting in a 64 pin package. The addition of a halt pin has also been made to the 64 pin package. This pin gives the user the ability to stop as well as single-step the chip. The PIC1664 is designed as a useful tool for engineering prototyping and field trail demonstration.

PIN CONFIGURATION
64 LEAD DUAL IN LINE



BLOCK DIAGRAM



TTL PIC Emulator

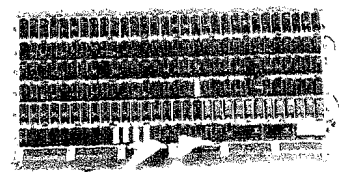
FEATURES

- Provides hardware emulation of the PIC1650
- PIC program can be in RAM or PROM.
- Interface with GIMINI provides interactive debugging of the PIC's program.
- I/O Data for all 512 instruction steps stored in RAM.

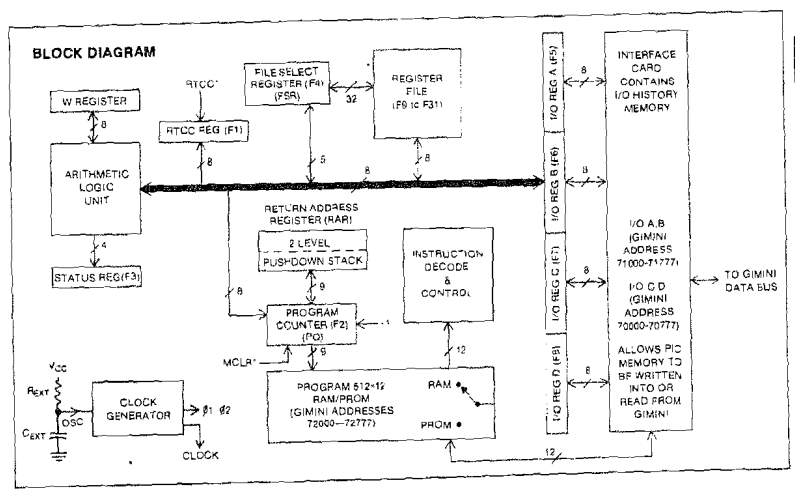
DESCRIPTION

The PIC Emulator is a hardware tool useful in the prototyping state of a product. It consists of a 180 IC wirewrap card containing a TTL emulation of the PIC chip, a cable terminating in a 40-pin male plug which would plug into the PIC's 40-pin socket on the end product's breadboard, an interface card to the GIMINI Microcomputer and 2 cables between the wirewrap card and the interface card. The interface card permits the PIC's ROM program to be interrogated (if the PROM/RAM switch on the PIC Emulator's wirewrap card is in the PROM position) or to be interrogated and modified (if the PROM/RAM switch is in the RAM position) via the GIMINI's front panel or via the GIMINI in conjunction with a terminal device. Thus, with a GIMINI and a terminal, on-line changes in the PIC's program can be implemented immediately in an interactive mode between the user and the GIMINI Microcomputer. The interface card also contains 512×16 of RAM to store the data present on each of the 512 instruction steps of the PIC1650. This I/O history feature is quite useful in program debugging.

TTL PIC EMULATOR



BLOCK DIAGRAM

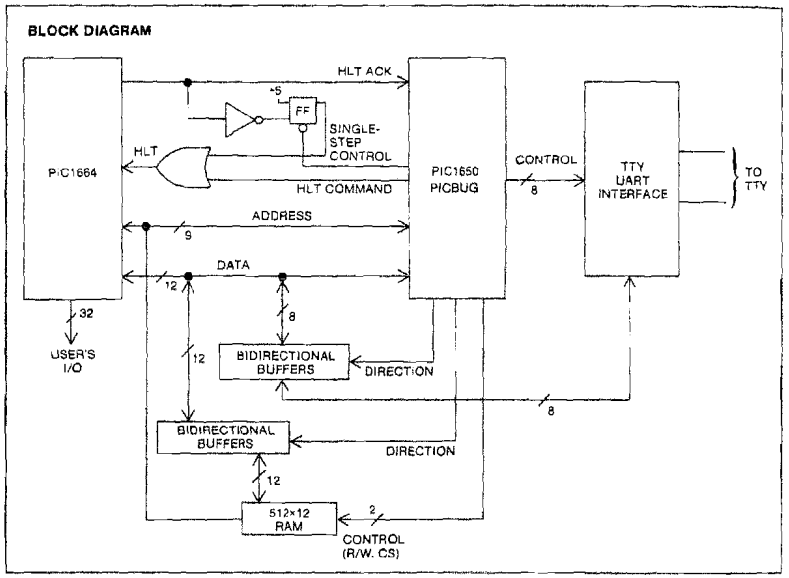


MOS PIC Emulator

DESCRIPTION

The MOS PIC Emulator is useful for debugging a PIC applications program. The card contains 512×12 of RAM, a PIC1650 containing PICBUG (see page 10C-19), a TTY interface and a PIC1664. A reset button is provided, which halts the PIC1664 and places PICBUG in the command mode.

BLOCK DIAGRAM

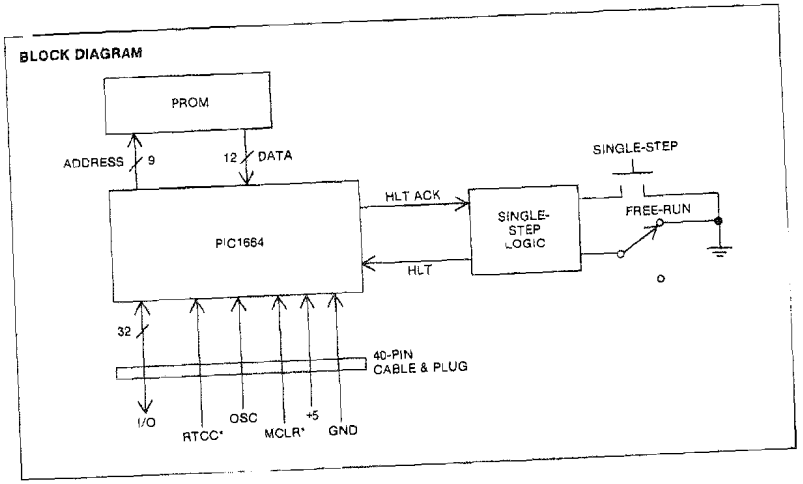


PIC Field Demo Card

DESCRIPTION

The PIC Field Demo Card is used to demonstrate a PIC 1650's capability in the field before committing to masked ROM. The card contains a PIC1684, 2 PROMs (512×8 organization with 1 µs or less access time) to hold the user's program, and logic to allow a single-step or free-run mode. The card terminates in a 40-pin plug to simulate the PIC1650's pinout.

BLOCK DIAGRAM



PIC Assembler

FEATURES

- Symbolic representation of all instructions
- User defined six character symbols
- Octal, decimal, hexadecimal and ASCII literals
- Expression evaluation.
- Extensive assembly directives
- Full program and sorted symbol listing.
- Extensive error detection

DESCRIPTION

The PIC assembler converts symbolic source programs for the PIC1650 into suitable code. Programs for the PIC may be coded symbolically using methods and techniques common to assembly level coding for conventional stored program computers. The PIC assembler produces a binary paper tape output which may be loaded and executed by the PIC TTL Emulator or used to directly mask program on PIC chip.

The PIC assemoler is available in two versions allowing execution on a wide variety of computers. One version, coded in FORTRAN IV is intended for use on popular mini-computer and larger computer systems and time sharing systems. The other version, coded in CP1600 assembly language executes on a GIMINI microcomputer with at least 6K words of 16-bit RAM storage.

USING PICAL ON GIMINI

A terminal and a high speed reader/punch are required to use PICAL on the GIMINI microcomputer system. The PIC Assembler is first loaded via the loader command "LH". To execute, command 'E' is typed in. PICAL identifies the version in use, indicates assembly pass 1 and requests source input device identifications by printing "SRC DEV? (H/L):" The user response with "L" (low speed tape reader, i.e., teletype) or "H" (high speed tape reader). Note that all user responses are terminated by a carriage return. The user is then requested to select the 7 level tape option by the message "7 level? (Y/N):" If the source tape contains valid 7 level ASCII characters, the response is "Y"; otherwise the response is "N". Next, the assembler requests the user to select a pass 1 listing option by printing "Listing? (Y/N)." A pass 1 program listing is complete except for forward symbol references and undefined symbol diagnostics.

Assembly pass 2 begins when "Pass 2? (Y/N)" is printed at the end of pass 1. The "LISTING? (Y/N)" is printed to allow the user to select a pass 2 listing. Next, the device upon which the object module is to be punched is requested by "OBJ DEV? (H/L/N):" being printed. If the high speed tape punch is to be used, "H" is entered; if low speed tape punch is to be used, "L" is entered. If no object module is to be generated, "N" is entered. If a pass 2 listing and object output on the low speed punch are selected, "DEV CNFLCT!!" is printed and the pass 2 options again requested because the listing and object code cannot be mixed on the teletype during the same assembly pass. If object output is to be punched on the low speed reader, the user must manually enable the teletype punch before entering the "L" response. Since pass 2 starts when the object option is entered, the source tape must be repositioned on the appropriate reader before the option is entered. At the end of pass 2, pass 2 may be rerun by entering "Y" in response to the message "Pass 2? (Y/N): If "N" is entered, pass 1 is reinitiated.

A program assembly can be aborted by depressing the teletype "CRTL" key while simultaneously striking the "C" key. This causes the assembly to be cancelled and control to be returned to the resident monitor.

SOURCE PROGRAM FORMAT

A PIC source program is composed of a sequence of statements with each statement contained on a single line terminated by a carriage return character. A statement may contain up to four fields identified from left to right as follows:

LABEL OPERATOR OPERAND COMMENT

The label and comment are optional, while the operator is always required. The presence and nature of the operand depends upon individual operators. Statements should not exceed approximately 50 characters so that assembled programs can be printed on a teletype or similar terminal.

LABEL

A label is a user defined character string, used to symbolically reference a specific location within a program. If a statement contains a label, the label must begin in the first character position in the statement. Labels may contain up to six characters, the first of which must be a letter (A-Z), a currency symbol ($), a question mark (?) or an ampersand (&). The remaining five optional characters may be any combination of A-Z, 0-9, $, ? or &.

OPERATOR

An operator follows the label field in a statement. A statement operator contains up to six characters and may be an instruction mnemonic or an assembly directive. Instruction mnemonics are symbolic character strings which represent the various PIC micro instructions. Assembly directives are symbolic character strings used to represent certain actions performed by the assembler. If a statement does not contain a label the operator must be preceded by at least one blank space. If the operator is the last field in a statement, it may be followed by a carriage return, otherwise it is followed by the comment field.

OPERAND

An operand follows the statement operator separated by at least one blank space. Operands may be blank space. Operands may be symbols, literals or expressions. When multiple operands are used, they are separated by commas. If an operand is the last field in a statement it is followed by a carriage return, otherwise it is followed by the comment field.

COMMENT

The comment field is optional in all statements and must be preceded by a semicolon(;) The contents of the comment field are printed on the program listing but have no effect on the assembled program. Entire lines may serve as comments if the first non-blank character is a semicolon. Blank lines may be used to separate statement lines in order to enhance program readability.

SYMBOLS

A symbol is a user defined character string which appers in an operand and is used to represent the value assigned to the symbol by the assembler. A symbol is given a value by direct assignment via an assembly directive or by appearing in the label field of a statement. Instruction labels are given the value of the assembly location counter associated with the instruction. The assembler recognizes the exclamation mark (!) as a special symbol for the current value of the program counter.

LITERALS

Literals are character strings which serve as sources of data, i.e., cannot be changed and are interpreted by the assembler as constants. Literals may be expressed as octal, decimal, hexadecimal, binary and character and may be preceded by a plus (+) or minus (-) to signify sign. Plus is assumed unless a minus is present.

Octal

soooo - s = optional + or -, + assumed
o = 0-7; 0 to 7777

Decimal

s.dddd - s = optional + or -, + assumed
. = leading character
d = 0-9; 0 to ± 2047

Hexadecimal

sX'nhh' - s = optional - or -, + assumed
X' = leading characters ' = trailing character
h = 0-9, A-F; 0 to FFF

Binary

sB'bbbbbbbbbbbb' - s = optional + or -, + assumed
B' = leading characters, ' = trailing character
b = 0 1; 0 to 111111111111

Character

s"C" or 'C' - s = optional + or -, + assumed
" or ' = leading and trailing characters
C = any ASCII character

EXPRESSIONS

Arithmetic operators + and - may be used to form operand expressions containing up to six elements. An expression element may be a user defined symbol, the assembly location counter (!) or a literal. Expression elements are separated by + or - and an expression is terminated by a comma, carriage return or a semicolon (;) Expressions are evaluated from left to right with no parenthetical groupings allowed.

ASSEMBLY DIRECTIVES

	ORG	exp	Set the assembly location counter of the value of expression. Program assembly starts at zero by default.
Symbol	EQU	operand	Assign the value of the operand to the symool. The operand may be a
Symbol	=	operand	symbol, a literal or the assembly location counter symbol (!). If ! is specified it may be followed by + or - and a literal. Note that only one level of forward symbol reference is allowed.
(Label)	ZERO	expression	Zero a block of storage whose length is specified by the expression. If a label is specified it is assigned a value equal to the address of the first word in the block
(Label)	DATA	expr [, expr. . .,expr]	Generate a data word for each operand expression. The contents of each word is set equal to the value of the respective expression. If a label is specified it is assigned a value equal to the address of the first word generated.
	END		End of the program, the assemply is terminated on the previous statement.
	PAGE		Advance the listing to the top of the next page.
	TITLE	name	Use the specified six character name in the listing page heading.

PROGRAM LISTING

The PIC assembler produces a listing of the assembled program containing the following fields: Line number; address; contents; label; opertor, operand(s) and comment. The address field contains three octal digits (eight bits), the contents field contains four octal digits (twelve bits) and the label, operator, operand(s) and comment fields are columnized to enhance program readability. Each page of listing contains sixty lines and begins with a one line heading. At the end of the program listing all user defined symbols and the number of diagnostics issued are summarized.

BINARY MACHINECODE

The PIC assembler produces binary machine code punched on paper tape formatted for loading by the CP1600 resident loader. This format permits the program to be loaded into suitable CP1600 microcomputer memory locations for execution by a PIC emulator. The paper tapes are formatted into one or more variable length binary records. Each record contains a four frame header and up to 132 data frames followed by a check sum frame. The first frame in each record contains a 001 except for the last record which contains a 377. The second frame contains the PIC assembly base address, the third frame contains 000 and fourth frame contains the number of data frames following in the record. The last data frame is followed by record check sum frame which is used to verify the data when the tape is read. Each PIC instruction is punched in a three frame sequence which contains 001, the least significant eight bits and the most significant four bits. Address adjustments resulting from impedded ORG or RES assembly directives result in a three frame sequence containing a 000, the address adjustment and 000.

DIAGNOSTICS

The PIC Assembler issues the following diagnostic messages when the indicated error conditions are detected:

SYNTAX	Syntax error
LABEL	Label illegal or missing
OP UNREC	Operator unrecognized
UNDF SYM	Undefined symbol referenced
DBL DEF	Double or multi-defined symbol
MDEF SYM	Double or multi-defined symbol referenced
FILE REG	File Register designator illegal
BIT NUM	Bit Number designator illegal
OPRN VAL	Operand value illegal
LITERAL	Literal illegal
DEST	Destination illegal
PHASE	Phase error, i.e., symbol has different definition in pass 2 than in pass 1
?SYNTAX	Questionable syntax
?LABEL	Questionable use of label
ADR/DEST	Questionable address or destination
?USE	Questionable use of directive
MEM LIM	PIC ROM limit exceeded
TRUNCATN	Statement field too long, truncated

USING PICAL

The PIC Assembler (PICAL) requires a GIMINI microcomputer with 8192 words of RAM and a ASR33 teletype terminal or equivalent for execution. A high speed paper tape reader/punch may be used for available. PICAL is loaded into the GIMINI by mounting the load module tape in either the low speed or high speed tape reader and entering "LL" (load via low speed reader) or "LH" (load via high speed reader) when at the monitor "$" level Note that all user inputs must be terminated by a carriage return. When the load is completed, a loader summary is printed and the monitor returns to the "$" level. Execution of PICAL is started by entering "E0" when at the "$" level.

Upon initial start-up, PICAL identifies the version in use, indicates assembly pass 1 and requests source input device identification by printing "SCR?(H/L)". The user must respond with "L" (low speed reader) or "H" (high speed reader). If the source tape contains valid 7 level ASC11 data, i.e., was punched on a parity generating device, a "7" is entered immediately following the device indicator. If only a carriage return is entered in response to the "SRC?" request, control is returned to the resident monitor. Next, the user may select a separated tape mode by responding to "SEP TAPES?(Y/N)" with "Y". If this mode is selected, PICAL will pause (GIMINI halts) after each physical tape segment is read (indicated by text ending with a form feed character). When the next source tape segment is mounted in the appropriate reader, the GIMINI START/STOP switch is depressed, continuing the assembly process. Finally, "LST?(Y/N)" is printed allowing the user to select a pass 1 program listing if desired.

At the end of pass 1 "PASS 2?(Y/N)" is printed allowing the user to elect to rerun pass 1 or proceed to pass 2. Prior to running pass 2 the source tape must be repositioned at the beginning. If in the segmented tape mode, physical tape segments must be read in the same order as in pass 1. After the pass 2 listing option is selected, "DEV?(H/L/N)" is printed allowing the user to select object tape output on the high speed punch, low speed punch or specify no object output. If a pass 2 listing and object output on the low speed punch have been selected, "DEVCNFLCT" is printed and the options are requested again.

If object output is on the low speed punch "PUNCH ON" is printed to remind the user to manually enable the teletype punch PICAL waits until the user enters a carriage return to indicate that the punch has been enabled. At the end of pass 2, "PASS 2?(Y/N)" is printed, allowing the user to rerun pass 2 or return to pass 1.

PIC Simulator

FEATURES

- Simulation of all PIC instructions.
- Access to all PIC operational registers.
- Execute, Trace and Step Modes.
- Console — interrupt and up to eight program breakpoints
- Real time clock simulation
- Input/output simulation.
- Execution time accumulation.
- Symbolic instruction mode.
- Numeric quantities expressed in octal or decimal.

DESCRIPTION

The PIC simulator (PICSIM) is a program which simulates the PIC1650. Programs assembled by the PIC symbolic assembler or programs entered manually may be quickly and easily debugged and verified using PICSIM

The PIC simulator is available in two versions allowing execution on a wide variety of computers. One version coded in FORTRAN IV is intended for use on popular minicomputer and larger time sharing systems. The other version executes on a GIMINI microcomputer.

PICSIM executes on a GIMINI microcomputer with at least 6K words of RAM memory and a teleptype or equivalent console. PICSIM is supplied as a relocatable load module which is loaded and executed using the GIMINI resident monitor. The user communicates interactively with PICSIM using a set of commands which are used to control the simulation environment and program execution.

USING PICSIM ON GIMINI

A terminal and a high speed reader/punch are required to use PICSIM on the GIMINI microcomputer system. The PIC simulator program tape is first loaded via the high speed reader by the loader command "LH". To execute, command "E" is typed in PICSIM identifies the version in use and prints out "Command summary? (Y/N)" The user responses with "N", if the printout of those commands are not required. Next PICSIM will request the next command to be executed by printing "Command?" To load the object tape, "LH" is entered. PICSIM will again request another command. The user can then enter any of the commands described below.

COMMANDS

The following commands may be entered on the console keyboard whenever a command prompt is displayed. Numeric quantities in commands, indicate by n, a, i, j in the descriptions may be entered in octal or decimal format. Decimal quantities are preceded by a period, i.e., ".15" is decimal 15 which "15" is octal 15. Quantities displayed by PICSIM are always in octal. If a command is unrecognized or contains an error, a "?" is displayed followed by another command prompt. All commands must be entered as indicated followed by a carriage return

? — Display Command Summary

Bn, A— Set program breakpoint n (0-7) at memory address a (0-7 777).

Bn — Remove program breakpoint n (0-7)

B — Remove all program breakpoints.

Cn — Continue program execution from the current breakpoint If optional n is specified, n subsequent program breakpoints that may be encountered will be ignored. This feature is useful when a program loop is to be breakpointed after n executions. If the current program was not breakpointed, the message "NO ACTIVE BRK PNT" is issued and the command is rejected.

DB — Display the currently specified program breakpoints. If the program was breakpointed, that breakpoint is preceded by "@". If a console interrupt (CNTRL/C) caused a breakpoint "@ C=address" is displayed. If there are no breakpoints set, "NONE!!" is displayed.

DIi,j — Display the instructions from memory locations i to j inclusive in symbolic format. See note 1.

DMi,j — Display the contents of memory from location i to j inclusive in dump format. See note 1.

DR — Display the contents of the W register, the RAR (Return Address Register Stack) and the 32 file registers. See note 1.

DT — Display the accumulated program execution time in microseconds.

Ea — Execute starting at memory address a. If a is not specified, execution starts at the current PC (File Reg. 2) address. When program execution starts, the execution time counter is zeroed. See note 3

Fn — Inspect/change the contents of File Register n (0-.32). See note 2

Ia — Inspect/change the instruction at memory address a in symbolic format. See note 2.

Lda — Load memory from device d (H=high speed, L=low speed) starting at address a.

Ma — Inspect/change the contents of memory address a. See note 2.

Pdi,j — Punch the contents of memory on device d (H=high speed, L=low speed) from address i to j inclusive

Rn — Set the interrupt repetition rate to n PIC machine cycles and activate the real time clock counter.

R — Deactivate interrupts.

R? — Display the current interrupt repetition rate

Sa — Step the program starting at memory address a. If a is not specified, stepping starts at the current PC (File Reg 2) address.

Ta — Trace program executions starting at memory address. If a is not specified, tracing starts at the current PC (File Reg 2) address. As each instruction is executed, the contents of the PC (program counter) is indicated by the display "@aaaa" where aaaa is the current address. See note 3.

W — Inspect/change the contents of the W register

X — Exit to the GIMINI resident monitor.

ZM — Zero memory.

ZR — Zero registers, (W, RAR and File Registers).

ZS — Zero RAR Stack

ZT — Zero the accumulated execution time.

NOTES

1. Striking console key "C" while depressing the "CTRL" key causes the console output to be terminated on GIMINI Systems On time sharing systems the "Break" key is used

2. Entering "/" opens the next location or register. "-" opens the previous location or register.

3. Striking console Reg. "C" while depressing the "CTRL" key on GIMINI Systems causes program execution to be suspended and interaction with the user resumed. The display "↑C@aaaa" indicates which instruction, i.e., aaaa is its address, was about to be executed. CTRL/C acts just like a breakpoint. On time sharing systems the "Break" key is used

INPUT/OUTPUT

PICSIM provides for simulation of both input and output operations through PIC file registers 5, 6, 7, 8 (IOA, IOB, IOC, IOD). Whenever an instruction sample file registers 5, 6, 7 or 8, the following display is output on the console "@aaaa, T=n USEC, ENTER IOREG DATA:" and program execution is suspended. In the display, "@aaaa" indicates the memory address of the instruction, "T=n USEC" indicates the accumulated execution time and "f" is A,B,C or D. Program execution resumes after the user enters appropriate data. Whenever an instruction places data in file registers 5,6,7 or 8, the following display is output on the console: "@aaaa, T=n USEC. IOREGf=dddd" and program execution continues. In the display. "@aaaa" indicates the memory address of the instruction, "T= USEC" indicates the accumulated execution time, "f" is A, B, C or D and "dddd" is the current contents of the register.

SYMBOLIC INSTRUCTIONS

The following symbolic instructions may be entered into memory from the console:

NOP	COMF f,d	BTFSS f,d
MOVWF f	INCF	RETLW i
CLRW	DECFSZ	CALL i
CLRF f	RRF f,d	GOTO x
SUBWF f,d	RLF f,d	GOTO0 i
DECF f,d	SWAPF f,d	GOTO1 i
IORWF f,d	INCFSZ f,d	MOVLW i
ANDWF f,d	BCF f,d	IORLW i
XORWF f,d	BSF f,d	ANDLW i
ADDWF f,d	BTFSC f,d	XORLW i
MOVF f,d		

where f = file register 0-37 (0-.31)
d = destination: 0 or W; 1 or F
i = literal 0-377 (0-.256)
x = literal 0-777 (0-.511)

ERROR CONDITIONS

PICSIM detects several error conditions while simulating the execution of PIC programs. The following error messages are issued as a result of the indicated error conditions. After the error message is displayed program execution is suspended and a command prompt is issued.

@aaaa, STK OVERFLOW!!	More than two levels of CALL instructions have been executed.
@aaaa, STK UNDERFLOW!!	More than two levels of RET instructions have been executed
@aaaa, INVALID READ OF PC!!	The program has attempted to read the contents of PC (File register 2), i.e., the program counter

PIC Debug

DESCRIPTION

PICBUG is a debug program contained in a PIC1650, which will enable the user to debug his PIC application program contained in 512×12 of RAM on the MOS PIC Emulator Card.

PICBUG contains the debug commands listed below (underlined items are typed by the user), the TTY service routines and the ability to terminate a lengthy display listing, and issue another command prompt, by the user depressing Control C.

PICBUG COMMANDS

1. **$Aa(CR):** Inspect address 200

   Example.
   $A200(CR)
   200 = 07142:(CR)
   $
   $A200(CR) Inspect addresses sequentially. Note that "/" causes the next address to be displayed, that "-" causes
   200= 07142:/ the previous address to be displayed and (CR) terminates activity
   201 = 10712:-
   200 = 07142:(CR)
   $A200(CR) ,Modify address
   200 = 07142:0(CR)
   $A200(CR) ,Modify addresses sequentially
   200 = 07142:0/
   201 = 10712:0-
   200 = 0(CR)
   $

2. **$Rn(CR):** ,Inspect/modify all PIC registers, W register is $R40_8$.

   Example:
   $R20(CR) ;Mofifying registers sequentially is not permitted — each register
   20 = 367:377 must be queried separately.
   $

3. **$La(CR):** Load memory contents of PIC instruction memory from the teletype reader, beginning at address a. If a is not specified, loading begins at the origin specified on the tape.

4. **$P,1,h(CR):** Punch memory contents of PIC instruction memory on the teletype punch, beginning at address 1 and ending at address h

5. **$DA1,h(CR):** Display contents of instruction addresses 1 to h inclusive

   Example:
   $DA202, 213(CR)

200	17036	17777	17776	01106	12571	00741	00741	00777
210	12525	05252	05252	12525	00000	00001	00002	00000

   $

6. **$DR(CR):** Display contents of all PIC registers and W register

   Example:
   $DR(CR)

W	131	141	172	100	404	303	313	121
7	000	777	123	421	727	777	121	111
17	000	121	515	172	200	556	555	554
27	000	131	161	172	400	000	222	111
37	101							

   $

7. **$Ea(CR):** Execute program from instruction address a. By default, a = 777_8.

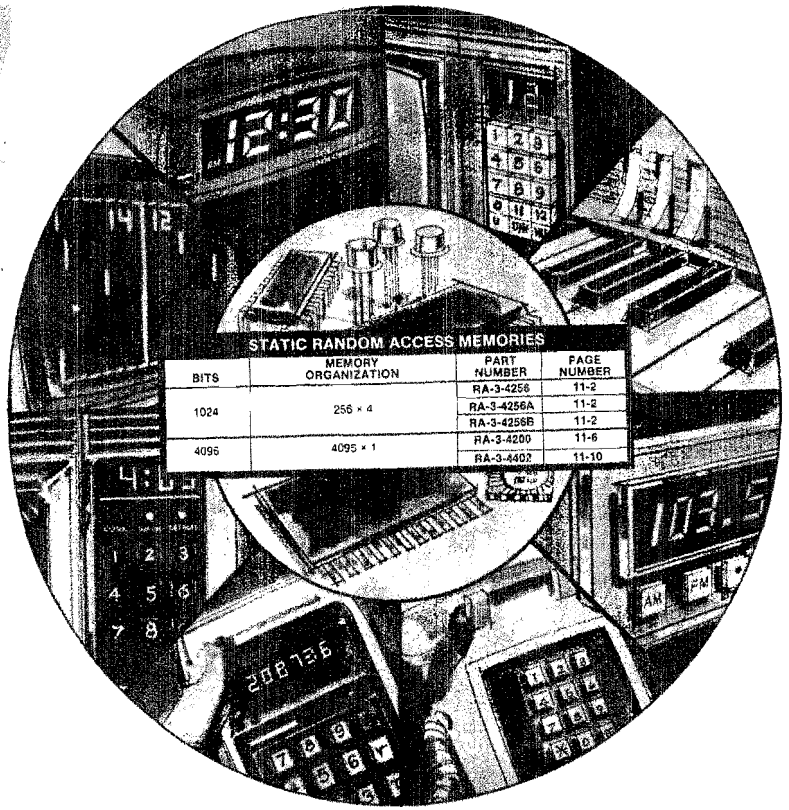
   Example:
   $E0(CR)

8. **$Bn,a(CR):** Set and execute program to breakpoint at address a. The breakpoint is automatically removed upon execution. The program continues from the last breakpoint upon setting a new breakpoint. If the previous breakpoint is not specified, the program is executed from 777_8

   Example. Set breakpoint 0 at address 100 and execute program from address 777_8 to address 100_8
   $B100(CR):

9. **$T(CR):** Trace (step) program one instruction at a time. Displays the contents of the W register each time. Use the breakpoint command to get to the desired starting address

10C



STATIC RANDOM ACCESS MEMORIES

BITS	MEMORY ORGANIZATION	PART NUMBER	PAGE NUMBER
1024	256 × 4	RA-3-4256	11-2
		RA-3-4256A	11-2
		RA-3-4256B	11-2
4096	4095 × 1	RA-3-4200	11-6
		RA-3-4402	11-10

11

STATIC RANDOM ACCESS MEMORIES

MICRO ELECTRONICS

RA-3-4256
RA-3-4256A
RA-3-4256B

1024 Bit Static Random Access Memories

FEATURES

- 256 x 4 Organization
- Single +5 Volt Supply
- True TTL Compatability
- Static Operation—no clocks required
- 500ns Access Time: RA-3-4256
- 650ns Access Time: RA-3-4256A, RA-3-4256B
- Separate Data Input and Output Lines
- Low Power
- Three State Outputs—under control of Chip Select signals
- Power Down State: RA-3-4256, RA-3-4256A
- Zener Protected Inputs

DESCRIPTION

The General Instrument RA-3-4256, RA-3-4256A and RA-3-4256B are 1024 bit, high-speed static random access memories organized as 256 4-bit words. Low voltage N-channel ion implant technology results in true TTL compatibility from a single 5 volt supply, and static operation. These devices are extremely useful in small read-write memory systems for terminals, peripherals, microcomputers, and a wide variety of portable equipment.

The RA-3-4256 and RA-3-4256A can also utilize a back bias substrate and split supply for applications where a low standby power drain is required. These devices may be switched to the power down state under system control with no danger of memory storage errors.

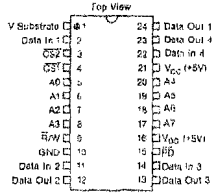
The RA-3-4256B's 22-pin package, which has a 0.4" width, permits tight packing density on printing circuit cards

	RA-3-4256	RA-3-4256A	RA-3-4256B
Package	24-pin	24-pin	22-pin
No. of Chip Select Inputs	2	2	1
Power Down Capability	Yes	Yes	No
Max Access Time	500ns	650ns	650ns

PIN CONFIGURATIONS

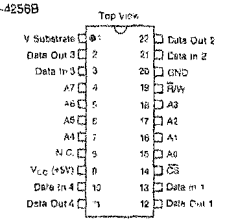
24 LEAD DUAL IN LINE

RA-3-4256/RA-3-4256A

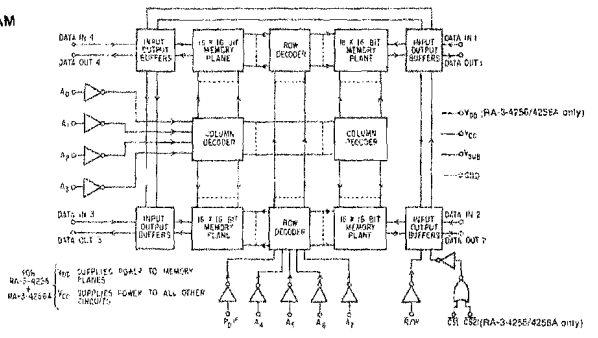


22 LEAD DUAL IN LINE

RA-3-4256B



BLOCK DIAGRAM



POWER DOWN OPERATION

The RA-3-4256 and RA-3-4256A bring out, to separate pins, the circuit Substrate, the memory plane supply (V_{DD}) and the peripheral circuit's power supply (V_{CC}). These three connections, plus the Power Down input, allow extremely flexible control of the memory during standby and/or reduced voltage and power dissipation operation.

In a static memory the memory cell is a flip flop and, in order to retain information, one side of the flip flop must be on continuously. Thus the static memory power dissipation is higher than for a dynamic memory and techniques for reducing this dissipation when the device is in the standby condition become attractive for the system user

The power down pin ($\overline{PD}$ pin 15) isolates the memory from the address decoders, so that incorrect data cannot be written into the memory when V_{CC} is not within its specified limits. Even if V_{DD} is maintained by a battery, if V_{CC} falls in a manner such that the R/W circuitry considers itself to be in a write mode for a short interval of time, then false data will be written into the memory. To prevent this from happening, $\overline{PD}$ is driven low by a signal (Power Down In) that senses V_{CC} is going below its allowable range. this is usually done by monitoring the power supply's AC input voltage. Fig. 1 shows the timing required before V_{CC} falls, to preserve a memory with a battery backup on V_{DD}

To prevent miswriting a data word, the fall of the $\overline{PD}$ signal must not intersect the R/W pulse. Otherwise, the write operation may not be complete at a given address when $\overline{PD}$ falls. The fall of $\overline{PD}$ during the R/W pulse would prevent that address (and all others) from having access to the memory section of the device. The external gating in Fig. 1b disallows $\overline{PD}$ from falling during a write operation.

Battery backup for V_{DD} can be accomplished as shown in Fig. 2. The germanium power translator (2N3612) is used here as a power diode. For a card with 10 RA-3-4256's, V_{DD} would draw a maximum current of 500 mA. The 2N3612 would have a maximum collector emmiter voltage drop of .25 v dc at 500 mA base current. During normal operation, if V_{CC} varied from 4.75 to 5.25 volts, V_{DD} would vary from 4.5 to 5.00 volts, which is within the operating specification. In the power down mode, V_{DD} would be supplied by the 5v standby battery. The battery voltge could fall from 5v to 4.5v (which would be from 4.25V to 3.75V for V_{DD} because of the silicon diode) and still keep the memory alive.

Once the memory is powered down so that the total supply current is reduced by a factor of 2 (since V_{CC} = 0 and is not drawing any current), I_{DD} can be reduced in half by placing −5 volts on V_{SS} — pin 1. This back-biases the substrate which reduces the current drawn in each flip-flop in the memory during this memory hold state. The −5 volts on V_{SS} can only be used to retain the information in the memory and must be removed (V_{SS} = 0) before writing into or reading from the memory

Thus, using the power down mode and placing −5 volts on the substrate, total power dissipated would be reduced 75%, from a maximum of 500mW (5v × 100 mA) to 125 mW (5v × 25 mA)

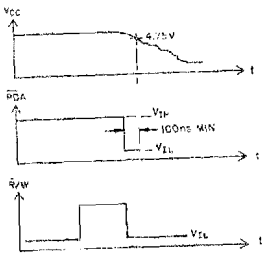


Fig.1a POWER DOWN TIMING

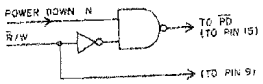


Fig.1b POWER DOWN GATING

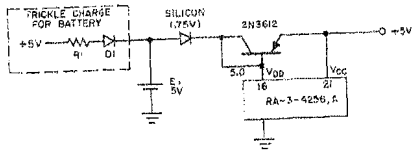


Fig.2 BATTERY STANDBY SCHEMATIC

11

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC}, V_{DD} and Input voltages (with respect to GND) .....-0.3V to +8.0V
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below

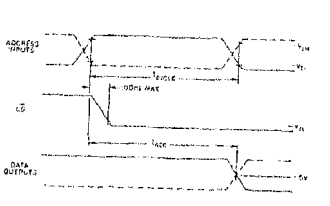
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±5% (V_{CC} is the peripheral circuitry supply for the RA-3-4256/4256A and the power supply for RA-3-4256B.)
V_{DD} = +5V ±10% (V_{DD} is the memory cell supply for the RA-3-4256/4256A.)
$V_{Substrate}$ = GND
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L(INCL)}$ = 100pF

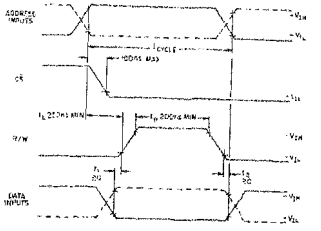
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input load current (all inputs)	I_{IN}	—	—	10	µA	V_{IN}=0V to 5.25V
Output leakage current	I_{LOH}	—	—	10	µA	V_{OUT}=4.0V
Output leakage current	I_{LOL}	—	—	−10	µA	V_{OUT}=0.4V
Input low voltage	V_{IL}	—	—	0.65	V	
Input high voltage	V_{IH}	2.2	—	—	V	
Output low voltage	V_{OL}	—	—	0.40	V	I_{OL}=1.6mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH}=100µA
Input capacitance (all inputs)	C_{IN}	—	5	—	pF	f=1 MHz
Output capacitance (all outputs)	C_{OUT}	—	10	—	pF	f=1 MHz
Total Power Supply Current	I_{DD} & I_{CC}	—	60	100	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{DD}	—	30	50	mA	RA-3-4256, RA-3-4256A
Power Supply Current	I_{CC}	—	60	100	mA	RA-3-4256B
AC CHARACTERISTICS						
Access Time RA-3-4256	T_{ACC}	—	—	500	ns	
Cycle Time RA-3-4256	T_{CYCLE}	500	—	—	ns	
Access Time RA-3-4256A	T_{ACC}	—	—	650	ns	See Timing Diagrams
Cycle Time RA-3-4256A	T_{CYCLE}	650	—	—	ns	
Access Time RA-3-4256B	T_{ACC}	—	—	650	ns	
Cycle Time RA-3-4256B	T_{CYCLE}	650	—	—	ns	
POWER DOWN DC CHARACTERISTICS (RA-3-4256 & RA-3-4256A ONLY):						
Power Down Sink Current	I_{DD}	—	—	100	µA	V_{DD}=0.4V
Memory hold voltage	V_{DD}	3.75	—	7.0	V	V_{CC}=0
Substrate Power Supply	V_{SS}	−5	—	0	V	−5V in Power Down Mode only
Substrate Power Supply Current	I_{SS}	—	20	100	µA	V_{SS}=−5V, V_{CC}=0

**Typical values are at −25°C and nominal voltages

TIMING DIAGRAMS

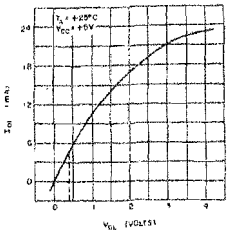


READ ACCESS

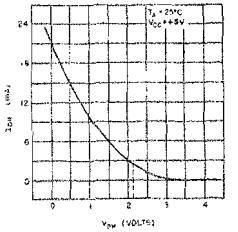


WRITE CYCLE

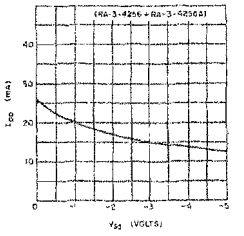
TYPICAL CHARACTERISTIC CURVES



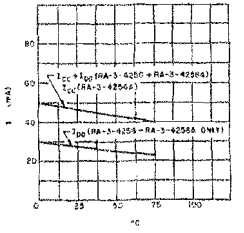
TYPICAL OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



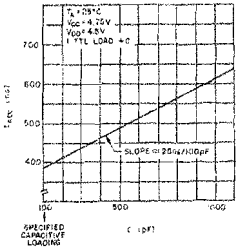
TYPICAL OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



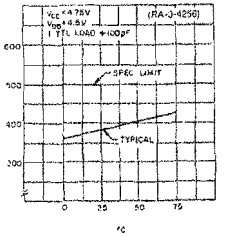
TYPICAL I_{DD} VS. V_{SS} (for memory hold during power down)



TYPICAL POWER SUPPLY CURRENT VS. TEMPERATURE



T_{ACC} (Typical) VS. CAPACITIVE LOADING



T_{ACC} VS. TEMPERATURE

RA-3-4200

4096 Bit Static Random Access Memory

FEATURES

- 4096×1 Organization
- Static Memory-no refresh required
- TTL Compatible Inputs (except CS)
- TTL Compatible Output
- Wire-Or'able Output-under control of a 'Chip Select' input
- High Speed: 215ns access time, 400ns cycle time
- Low Power: typically 450mW operating, 35mW standby
- Pin and Voltage Compatible with Popular 22 pin 4K Dynamic RAMs

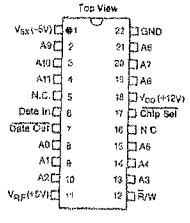
DESCRIPTION

The General Instrument RA-3-4200 is a 4096 bit static Random Access Memory ideally suited for memory system applications where there is an advantage in utilizing a static memory without sacrificing the high speeds that current dynamic memories offer. The RA-3-4200 is fabricated in GI's advanced GIANT II N-channel Ion Implant process and features a fully static memory cell to eliminate the need for any refresh or charge-pump circuitry and TTL compatibility except for a +12Volt Chip Select which dynamically accesses the memory

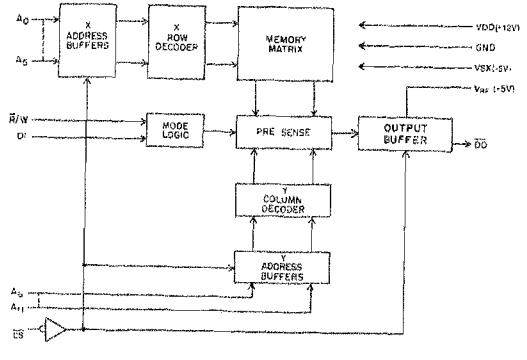
The RA-3-4200 is a direct replacement in pin connection and operation for the EM&M/SEMI 4200.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns The memory cells are loaded or interrogated by simultaneously decoding the X address A_0 through A_5 for the rows (see Block Diagram) and the Y address A_6 through A_{11} for the columns Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output TTL buffer. Each bit or memory cell is a standard flip flop consisting of R_1, R_2, Q2D and Q4D with two access devices Q1D and Q3D (See Figure 1) The load resistors R_1 and R_2 are 60 megohms typical and connect to the V_{DD} supply Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high In the read mode the cell pulls one of the sense lines low from its normally high state. The selected presense circuit detects the differential voltage on the sense lines and amplifies it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines

Chip Select

The Chip Select controls the operation of the memory. When the Chip Select input is high the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements When the Chip Select input is pulled low, the memory is enabled The Chip Select negative going edge clocks the TTL logic level addresses, R/W, and data input into "D" type flip flops, and enables the output stage

Data Output

While Chip Select is high, the output is high impedance to allow "wire-or" connections. When Chip Select goes low, the output data will be presented within the specified access time, and will remain until Chip Select goes high again. The output data signal is specified to drive any TTL series with good noise immunity at a fan-out of 1. Output data is inverted with respect to the input data.

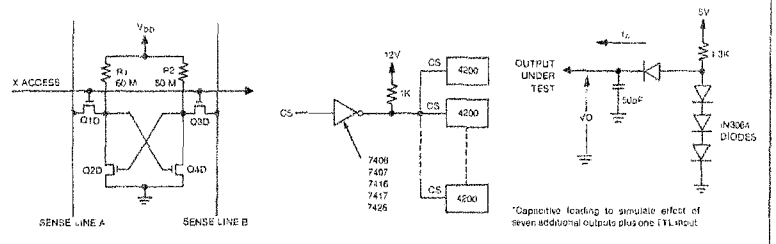


Fig.1 MEMORY CELL Fig.2 TYPICAL CHIP SELECT DRIVER Fig.3 OUTPUT TEST LOAD

Battery Operation/Power Failure Data Retention

The memory cells (because they are cross coupled high impedance static cells) will retain data down to V_{DD} = 4V.

Input Circuits — R/W Select, Data In and Address Input

The input signal is latched by Chip Select and can change after the specified hold time The inputs can be driven from standard TTL open collector outputs with pull-up resistors The input does not put any DC loading on the TTL driver.

Read/Write Mode Select

To WRITE, the R/W input should be high prior to Chip Select To READ, the R/W input should be low prior to Chip Select. When Chip Select goes low, R/W is latched into a register.

Data In

During a WRITE cycle the Data In (either high or low) should be stable prior to Chip Select When Chip Select goes low, R/W is latched into a register

Address

Addresses should be stable prior to Chip Select When Chip Select goes low all addresses are latched into an Address Register.

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ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Sym	Value	Unit
Supply Voltages	V_{DD}	−5 to +15	Vdc
	V_{BB}	+5 to −7	Vdc
	V_{SS}	+5 to −7	Vdc
Input & Output Voltages (Except Chip Select)	V_I, V_O	V_{SS} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SS} to +15	Vdc
Power Dissipation	P_D	1.6 (Note 2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	—	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

NOTE 2: At 25°C ambient Derate 13.8m W/°C

RECOMMENDED OPERATING CONDITIONS T_{AMB} = 0°C to 70°C

Parameter	Sym	Min	Nom	Max	Unit
Supply Voltage	V_{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V_{BB}	4.75	5.0	5.25	Vdc
Substrate Voltage	V_{SS}	−4.5	−5	−5.5	Vdc
Input High Level	V_{IH}	3	—	5.25	Vdc
Input Low Level	V_{IL}	0	—	0.8	Vdc
Chip Select High Level	V_{CH}	V_{DD}−3	V_{DD}	V_{DD}+3	Vdc
Chip Select Low Level	V_{CL}	0	—	0.5	Vdc

DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Input Current	I_{IN}	0	±10	±100	µA	V_{IN} = 0.5V or 5.0V
Chip Select Input Current	I_{CS}	—	±10	±100	µA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	—	0.3	0.5	Vdc	I_O = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.7	3.5	V_{BB}	Vdc	I_O = 500 µA Fig. 5
Output Current (Unselected)	I_{OD}	—	—	−50	µA	V_{IH} = 2.7V, V_{CS} = +12V
Supply Current (Selected and Averaged over one cycle)	I_{DD}	—	36	50	mA	V_{DD} = +12V
CSW = 215 nsec						V_{BB} = +5V
TC = 400 nsec						V_{SS} = −5V
For Other Conditions, See Fig. 3						T_{AMB} = +25°C
Supply Current (Unselected) T_{AMB} = +25°C	I_{DDU}	—	2	5	mA	V_{DD} = +12V
Supply Current (Unselected) T_{AMB} = +70°C	I_{DDU}	—	4.5	15	mA	V_{BB} = +5V
Substrate Current	I_{SS}	—	2.2	−3	mA	V_{SS} = −5V
Reference Supply Current	I_{BB}	—	50	100	µA	V_{CS} = +12V
Standby Current at Reduced Voltages T_{AMB} = +25°C	I_{DDS}	—	0.8	2	mA	V_{CC} = 4V to 15V V_{BB} = 4V V_{SS} = −5V±10% V_{RI} = 0V
Standby Current at Reduced Voltages T_{AMB} = +70°C	I_{DDS}	—	1.8	6	mA	

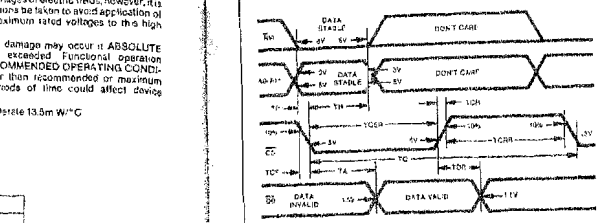
AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Sym	Min	Typ	Max	Unit	Fig
Chip Select Read Pulse Width	T_{CSR}	215ns	—	1ms	—	1
Chip Select Write Pulse Width	T_{CSW}	215ns	—	1ms	—	2
Chip Select Rise and Fall Time	T_{CR}, T_{CF}	—	10	50	ns	1&2
Set Up Time	Tp	0	—	—	ns	1&2
Access Time	T_A	—	—	215	ns	1
Cycle Time, T_{CR} + T_{CF} = 10ns (Read or Write)	T_C	400	—	—	ns	1&2
Data Hold Time	T_H	100	—	—	ns	1&2
Output Recovery Time	T_{OR}	10	15	—	ns	1
Read Recovery Time	T_{CRR}	150	—	—	ns	1
Write Recovery Time	T_{CWR}	150	—	—	ns	2

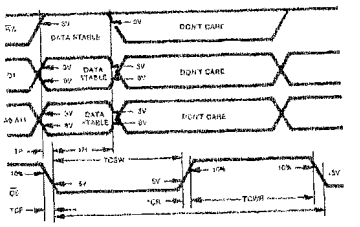
CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

Characteristics	Sym	Min	Typ	Max	Unit	Conditions
Input Capacitance (Except Chip Select)	C_{IN}	—	6	—	pF	V_{IN} = 2.4V
Input Capacitance Chip Select	C_{CS}	—	20	—	pF	V_{CS} = 12V or 0V
Output Capacitance	C_O	—	8	—	pF	V_O = 2V V_{CS} = 12V

TIMING DIAGRAMS

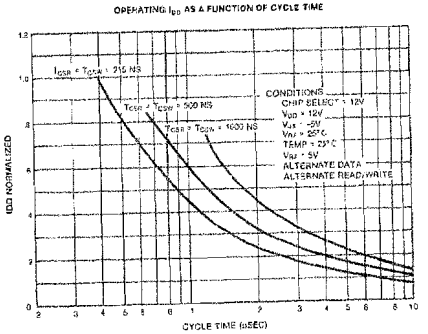


READ CYCLE



WRITE CYCLE

TYPICAL CHARACTERISTIC CURVE



OPERATING I_{DD} AS A FUNCTION OF CYCLE TIME

4096 Bit Static Random Access Memory

FEATURES

- 4096X1 Organization
- Static Memory-no refresh required
- TTL Compatible Inputs (except CS)
- Differential Output-two complementary Data Output signals are provided.
- Wire-Or'able Outputs-under control of a 'Chip Select' input
- High Speed: 200ns access time, 350ns cycle time.
- Low Power typically 400mW

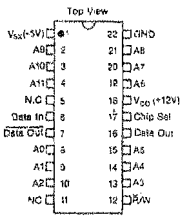
DESCRIPTION

The General Instrument RA-3-4402 is a 4,096 bit static Random Access Memory ideally suited for memory system applications where there is an advantage in utilizing a static memory without sacrificing the high speeds that current dynamic memories offer. The RA-3-4402 is fabricated in GI's advanced GIANT II N-channel ion implant process and features a fully static memory cell to eliminate the need for any refresh or charge-pump circuitry and TTL compatibility except for a +12Volt Chip Select which dynamically accesses the memory.

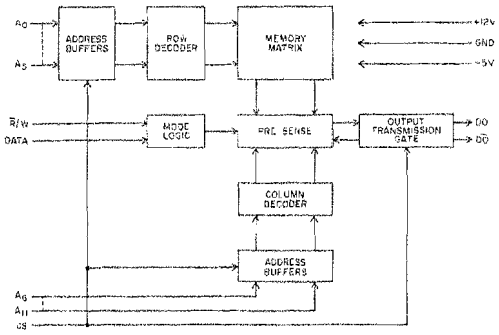
The RA-3-4402 is a direct replacement in pin connection and operation for the EM&M/SEMI 4402.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The 4096 static bits of memory are organized in an array of 64 rows by 64 columns. The memory cells are loaded or interrogated by simultaneously decoding the X address A0 through A5 for the rows (see Block Diagram) and the Y address A6 through A11 for the columns. Each column contains a presense amplifier, the outputs of which are "OR-ed" and connected to the output stage. Each bit or memory cell is a standard flip flop consisting of R1, R2 Q2D, and Q4D with two access devices Q1D and Q3D (See Figure 1). The load resistors R1 and R2 are 60 megohms typical and connect to the V_{DD} supply. Q1D and Q3D are used to connect the cell to the sense lines whenever the X access line is high. In the read mode the cell will pull one of the sense lines low from its normally high state. The selected presense circuit will detect the differential voltage on the sense lines and amplify it. In the write mode one sense line is forced low by the presense circuit and the selected cell assumes the state of the sense lines.

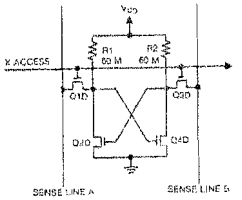


Fig.1 MEMORY CELL

Chip Select
The chip select controls the operation of the memory. When the chip select is low the input address buffers, decoders, sensing circuits and output stages are held in the "off" state and power is supplied only to the memory elements. When the Chip Select goes high the memory is enabled. The Chip Select pulse clocks the TTL logic level addresses, R/W, and data input into "D" type flip flops and enables the output stage.

Data Output
One of the two outputs will source current (DO for data originally input at V_{IH}, $\overline{DO}$ for data originally input as V_{IL}). With the output load as shown in Figure 2, the voltage at the output sourcing current (V_{OH}) will approach a value between 0.35V and 2V (typically 1V) above ground. The voltage at the other output (V_{OL}) will be below 100 mV. A differential amplifier is used to detect the polarity of the signal. A differential output of 25mV (V_{DIF}) or more is considered a valid output.

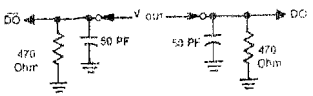


Fig.2 OUTPUT LOAD

Battery Operation/Power Failure Data Retention
The memory cells (because they are cross coupled high impedance static cells) will retain data down to V_{DR} = 4V. At V_{DD} = 4V, the typical power dissipated is 1μw/bit.

Input Circuits — R/W Select, Data In and Address Input
The input signal is latched by Chip Select and can change after Chip Select is high. The inputs can be driven from standard TTL open collector outputs with pull-up resistors. The input does not put any DC loading on the TTL driver.

Read/Write Mode Select
To WRITE, the R/W input should be HIGH prior to Chip Select. To READ, the R/W input should be LOW prior to Chip Select. When Chip Select is high, R/W is latched into a register.

Data In
During a WRITE cycle the Data In (either HIGH or LOW) should be stable prior to Chip Select. When Chip Select is high, Data In is latched into a register.

Address
Addresses should be stable prior to Chip Select. When Chip Select is HIGH all addresses are latched into an Address Register.

ABSOLUTE MAXIMUM RATINGS (See Note 1) (Referenced to GND)

Rating	Sym	Value	Unit
Supply Voltages	V_{DD}	−0.5 to +15	Vdc
	V_{SX}	+0.5 to +7	Vdc
Input & Output Voltages (except Chip Select)	V_I, V_O	V_{SX} to +15	Vdc
Chip Select Input Voltage	V_{CS}	V_{SX} to +15	Vdc
Power Dissipation	P_D	1.6 (Note2)	W
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMEND OPERATING CONDITIONS. Exposure to higher than recommended or maximum voltages for extended periods of time could affect device reliability.

Note 2: At +25° C ambient. Derate 13.5m W/°C

RECOMMENDED OPERATING CONDITIONS T_A = 0°C to +70°C

Parameter	Sym	Min	Nom	Max	Unit
Supply Voltages	V_{DD}	11.4	12	12.6	V
	V_{SX}	4.5	5	5.5	V
Logic Levels*					
Input High Voltage (except Chip Select)	V_{IH}	3	—	6.25	V
Input Low Voltage (except Chip Select	V_{IL}	0	—	0.7	V
Chip Select High Voltage	V_{CH}	V_{DD}	V_{DD}+1V	V_{DD}+2V	V
Chip Select Low Voltage	V_{CL}	0	—	1	V

DC ELECTRICAL CHARACTERISTICS (Full Operating voltage & temperature range unless otherwise noted)

Characteristics		Sym	Min	Typ	Max	Unit
Input Current (except Chip Select)	V_{IH} = 6.0V (V_{CS} = V_{CH})	I_{CI}	—	5	25	μA
	V_{IL} = 0.5V (V_{CS} = V_{CH})	I_{IL}	—	-5	-25	μA
Unselected Input Current (V_{CS} = V_{CL}) V = 2.4V		I_{IH}	—	5	25	μA
Chip Select High Input Current, DC (V_{CS} = 12V)		I_{SH}	—	30	40	mA
Chip Select High Input Current, (Pulse Peak) V_{CS} = 12V T_{CR} = 25ns		I_{CP}	—	70	—	mA
Chip Select Low Input Current (V_{CS} = 1V)		I_{CL}	—	2	3	ma
Supply Current, (T_{AMB} = 25°C, V_{DD}, V_{IL} — nominal; all VI = max V_{IH}. DO, DO terminated as shown in Figure 2)	Unselected (Chip Select = 0 V)	I_{DDU} 25°C	—	1	5	mA
		I_{DDU} 70°C	—	3	15	mA
		I_{SXL}	—	-2	-3	mA
	Selected Chip Select = 12V, 50% duty cycle	I_{DDL}	—	17.5	22.5	mA
		I_{SX}	—	-2	-3	mA
Standby Current at Reduced Voltages	25° C	I_{DDW}	—	5	1.8	mA
V_{DD} = 4V, V_{SX} = 3V, V_{CS} = 0V	70°	I_{DDW}	—	1.5	5.3	mA
Substrate Current at Reduced Voltage	25° C V_{CS} = 0 VSX = −3	I_{SX}	—	-1	1.5	mA
Output Low Voltage Terminated per Figure 2 T_{CSW} = 1μsec		V_{OL}	—	0	1	V
Output High Voltage Terminated per Figure 2 T_{CSW} = 1μsec		V_{OH}	35	1	2	V
Output Disabled Current V_{CI} = 0V, V_{OH} = 2V		I_{OH}	+10	—	−10	μA

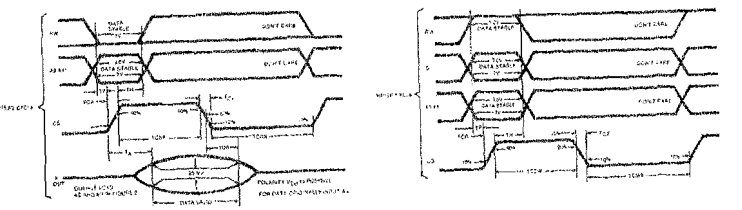
AC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

Characteristics	Sym	Min	Typ	Max	Unit
Chip Select Read Pulse Width	T_{CR}	200	—	∞	ns
Chip Select Read Recovery Time	T_{CRR}	125	—	∞	ns
Chip Select Write Pulse Width	T_{CW}	200	—	∞	ns
Chip Select Write Recovery Time	T_{CWR}	125	—	∞	ns
Chip Select Rise Time	T_{rc}	—	10	50	ns
Chip Select Fall Time	T_{fc}	—	10	50	ns
Set Up Time	T_S	10	—	—	ns
Hold Time (Address and Data)	T_H	60	—	—	ns
Access Time (T_{CR} = 10ns)	T_A	—	—	200	ns
Cycle Time (Read or Write, T_{CR} = 10ns, T_{rc} = 10ns)	T_L	350	—	—	ns
Data Recovery	T_{DR}	10	15	—	ns

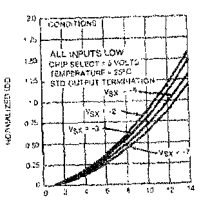
CAPACITANCE (Over Full Temperature Range and Worst Case Voltage Conditions)

Characteristics	Sym	Min	Typ	Max	Unit
Input Capacitance (except Chip Select) V_I = 2.4V, V_{CS} = 12V	C_I	—	6	—	pF
Chip Select Input Capacitance	C_{CS}	—	50	—	pF
Output Capacitance (V_{OH} = 2.0V V_{CS} = 0)	C_O	—	5	—	pF

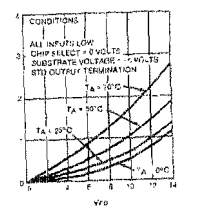
TIMING DIAGRAMS



TYPICAL CHARACTERISTIC CURVES



I_{DD} VS. V_{DD} AT VARIABLE V_{SX}



I_{DD} VS. V_{DD} AT VARIABLE TEMPERATURE

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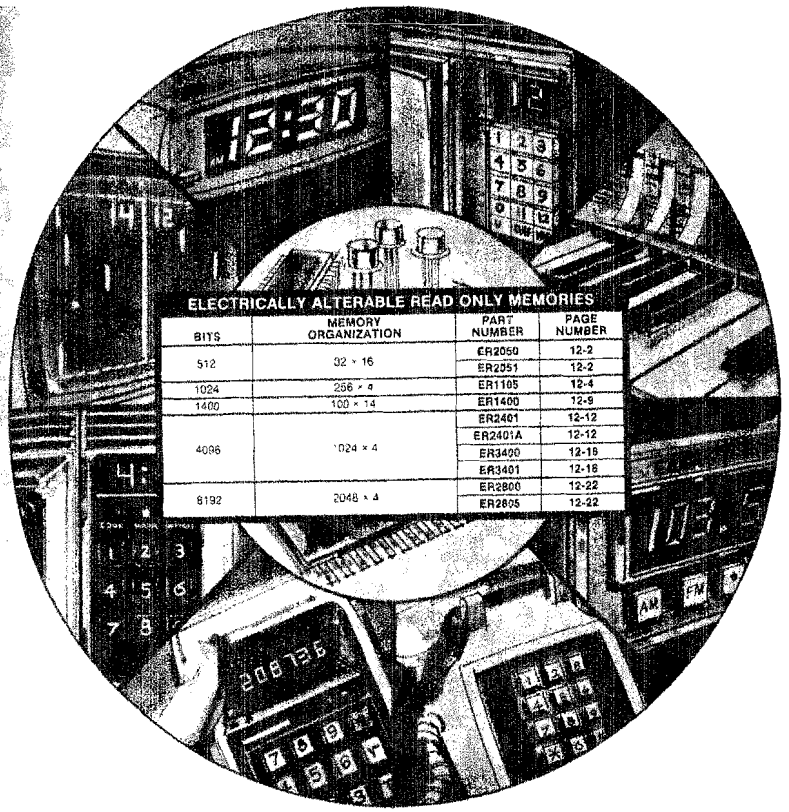

ELECTRICALLY ALTERABLE READ ONLY MEMORIES

BITS	MEMORY ORGANIZATION	PART NUMBER	PAGE NUMBER
512	32 × 16	ER2050	12-2
		ER2051	12-2
1024	256 × 4	ER1105	12-4
1400	100 × 14	ER1400	12-9
4096	1024 × 4	ER2401	12-12
		ER2401A	12-12
		ER3400	12-16
		ER3401	12-16
8192	2048 × 4	ER2800	12-22
		ER2805	12-22

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ELECTRICALLY ALTERABLE READ ONLY MEMORIES

MICRO ELECTRONICS

ER2050 ER2051

512 Bit Electrically Alterable Read Only Memories

FEATURES

- 32x16 Organization
- 5-Bit Addressing
- TTL Compatible
- Chip Select
- Word Alterable
- 10 Year Unpowered Data Storage
- 10 μs Access Time (ER2050)
- 3 μs Access Time (ER2051)
- Write/Erase Time 100ms/word (ER2050), 50ms/word (ER2051)
- +5, -28V Supplies
- No Voltage Switching Required

NOTE. Use ER2051 for all new designs.

DESCRIPTION

The ER2050 and ER2051 are fully decoded 32 × 16 electrically erasable and reprogrammable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Two TTL compatible control pins switch voltages internally for write, read and erase control.

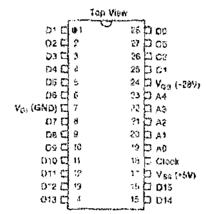
OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which lowers the threshold of both transistors), data is written into one of the transistors lowering its threshold. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending on which transistor is "written".

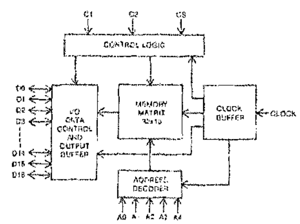
It is important to note two things: first, that an erase is required before a write to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

PIN CONFIGURATION

28 LEAD DUAL IN LINE



BLOCK DIAGRAM



PIN FUNCTIONS

A_0-A_4	5-Bit Word Address
D_0-D_{15}	Data input and output pins
CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced
C1 C2	Mode Control Inputs C1 C2 1 1 Hold Mode: output data from previous read operation stored at output pins. (For the ER2050 only. This code is "read mode" for the ER2051) 0 1 Erase Mode: stored data is erased at addressed location 1 0 Read Mode addressed data read after clock pulse. Output data retained at output pins until next read operation 0 0 Write Mode: Input data written at addressed location Clock not required NOTE Care must be exercised to ensure that CS is held at logic "0" during power up or power down to protect all addresses from spurious write or erase inputs
CLK	Clock Input. Pulse to logic "1" for read operation The clock may be repetitive or may simply be pulsed when data is to be read. When the clock is repetitive the ER2050 should be maintained in the standby mode when data is not being read, as every clock pulse will constitute a read operation. When the clock is not repetitive data will remain valid for 20 to 60 seconds, the outputs will then become open circuit until another clock pulse is received The clock should not be repetitive for the ER2051
V_{SS}	Substrate supply Normally at +5 volts
V_{GI}	Ground Input
V_{GG}	Power Supply Input. Normally at -28 volts

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) .... -35V to +0.3V
Storage temperature .... -65°C to +150°C
Soldering temperature of leads (10 seconds) .... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

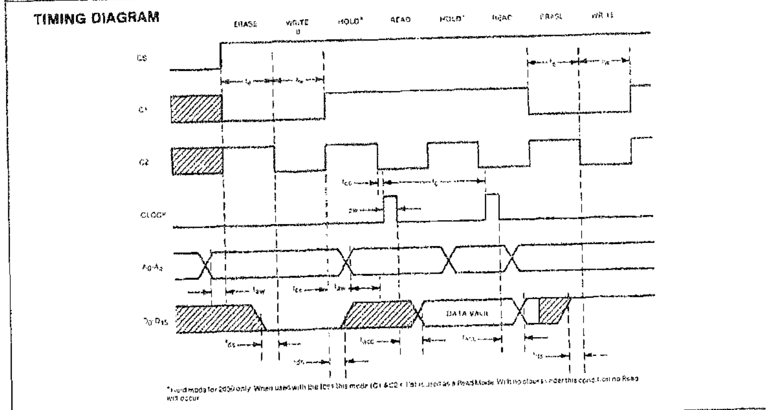
Standard Conditions (unless otherwise noted)

V_{SS} = +5V±5%
V_{GG} = -28V±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70C
Output Load = 100pF, 1 TTL load

Characteristic	Symbol	ER2050 Min	ER2050 Typ**	ER2050 Max	ER2051 Min	ER2051 Typ**	ER2051 Max	Units
DC CHARACTERISTICS								
Input Logic "1"	V_{IH}	V_{SS} -1.5	—	V_{SS} +0.3	V_{SS} -1.5	—	V_{SS} +0.3	Volts
Input Logic "0"	V_{IL}	-10.0	—	+0.8	-10.0	—	+0.8	Volts
Output Logic "1"	V_{OH}	V_{SS} -1.5	—	—	V_{SS} -1.5	—	—	Volts
Output Logic "0" (I_{OL} = 1.5mA)	V_{OL}	—	—	-0.8	—	—	+0.8	Volts
Power Supply Current							-13.8	mA
Read	I_{GG}	—	-7.0	-8.5	—	—	-10.3	mA
Write	I_{GG}	—	-6.0	-7.5	—	—	-10.3	mA
Erase	I_{GG}	—	-4.0	-5.5	—	—		
AC CHARACTERISTICS							3.0	μsec
Access Time	t_{acc}	—	6.0	10.0	—	—	20.0	μsec
Clock Width	t_{pw}	.75	—	20.0	2.0	—	200	msec
Write Time	t_w	100	—	200	50	—	200	msec
Erase Time	t_e	100	—	200	50	—	—	nsec
Address-Clock Time	t_{cc}	100	—	—	100	—	—	μsec
Write/Erase-Address Time	t_{ca}	1	—	—	1	—	—	nsec
Address-Write/Erase Time	t_{aw}	50	—	—	50	—	—	μsec
Clock Period	t_c	10.0	—	—	3.5	—	—	nsec
Data Setup Time	t_{ds}	50	—	—	50	—	—	nsec
Data Hold Time	t_{dh}	50	—	—	50	—	—	
Number of read accesses/ word between refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—	—
Number of times word may be rewritten	N_W	—	—	10^6	—	—	10^6	—

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM



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1024 Bit Electrically Alterable Read Only Memory

FEATURES

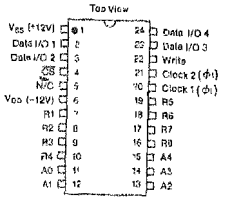
- 256 x 4 Organization
- 5-Bit Binary Column Address
- One of 8 Line Row Address
- Electrically Erasable by Flow
- Electrically Reprogrammable
- 10 ms/4-Bit Word Write Time
- 2 μs Access Time
- Minimum Data Retention: 200×10^9 Read Accesses/Word between Refresh
- Chip Select Input
- Unpowered Nonvolatile Data Storage—10 Years

DESCRIPTION

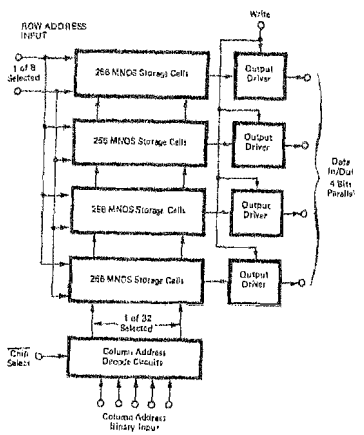
The ER1105 is a 256-word by 4-bit, electrically erasable and reprogrammable ROM that takes advantage of the unique properties of P-channel MNOS technology. Data is written into the device by tunneling a charge into the oxide-nitride interface at the gate insulator of MNOS memory transistors. This is accomplished by applying a -24 V , 10 ms row input pulse The resulting charge trapped in the gate insulator causes a change in the threshold voltage of the memory transistors that is sensed during subsequent readout. Data is erased by applying a -30V, 100ms pulse to the row inputs There are 8 blocks of 32 words×4 bits, each block being separately alterable

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Supply voltage (V_{DD}) relative to V_{SS}	. +0.3 to -30V
Input voltage (except row input) relative to V_{SS}	. +0.3V to -30V
Row input voltage relative to V_{SS}	. +35V to -35V
Operating ambient temperature	. -25°C to +70°C
Storage temperature	-65°C to +150°C
Soldering temperature of leads (10 seconds)	+300°C
Thermal resistance chip to ambient	. 80°C/Watt
Power dissipation	. 500 mW

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

NOTE: This data sheet assumes negative logic.

V_{SS} = +12V±5%
V_{DD} = -12V±5%
Operating Temperature (T_A) = -25°C to +70°C

Characteristic	Symbol	Min.	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input leakage current (all inputs except row inputs)	I_{IN}	--	—	-1	μA	at V_{IN}=-15V, all other pins grounded, T_A=+25°C
Row input leakage current	I_R	—	—	-1	μA	at V_{IN}=±30V, all other pins grounded, T_A=+25°C
Input load current (all inputs except row inputs)	I_{IL}	—	—	-20	μA	at V_{IN}=-27V, all other pins grounded, T_A=+25°C
V_{DD} power supply current	I_{DD}	—	-8	-12	mA	at V_{DD} relative to V_{SS}=-24V, T_A=+25° C
ϕ_1/ϕ_2 input high voltage	$V_{IH}\phi$	V_{SS}—1.5	—	V_{SS}+0.3	V	
ϕ_1/ϕ_2 input low voltage	$V_{IL}\phi$	V_{DD}	—	V_{SS}—22	V	
Read Cycle						
Column address and chip select input high voltage	V_{IH1}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Column address and chip select input low voltage	V_{IL1}	V_{DD}	—	V_{SS}—9.0	V	
Row input high voltage	V_{IH2}	V_{IT}—1.5	—	V_{SS}+0.3	V	
Row input low voltage	V_{IL2}	V_{SS}—13.0	—	V_{SS}—10.0	V	
Data output high voltage	V_{OH}	V_{SS}—1.0	—	V_{SS}—0.5	V	R_{LOAD}=6.8K returned to V_{DD}
Data output low voltage	V_{OL}	V_{DD}	—	—	V	R_{LOAD}=6.8K returned to V_{DL}
Erase Cycle						
Row input high erase voltage	V_{IHP}	V_{SS}+28	—	V_{SS}+32	V	
Write Cycle						
Col. add., $\overline{CS}$, and write input high voltage	V_{IH3}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Col. add., $\overline{CS}$, and write input low voltage	V_{IL3}	V_{DD}	—	V_{SS}—9.0	V	
Row input high write voltage	V_{IH4}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Row input low write voltage	V_{IL4}	V_{SS}—26	—	V_{SS}—22	V	
Data in high voltage	V_{IH5}	V_{SS}—1.5	—	V_{SS}+0.3	V	
Data in low voltage	V_{IL5}	V_{DD}	—	V_{SS}—22	V	

**Typical values are at +25° C and nominal voltages

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
AC CHARACTERISTICS						
Read Cycle						
Access time	t_A	—	—	2.0	μS	R_{LOAD}=6.8K to V_{DD} C_{LOAD}=20pf
Cycle time	t_C	3.5	—	—	μS	
ϕ_1 pulse width	$t_{\phi 1}$	0.5	—	—	μS	Rise and fall times ≤100 ns
ϕ_2 pulse width	$t_{\phi 2}$	0.5	—	—	μS	Rise and fall times ≤100 ns
Column address change to row input rise delay	t_{D1}	0.7	—	—	μS	
ϕ_1 fall to row input rise delay	t_{D2}	0.0	—	—	μS	
Row input rise to ϕ_2 rise delay	t_{D3}	0.3	—	—	μS	
ϕ_2 rise to data output delay	t_{D4}		—	0.4	μS	R_{LOAD}=6.8K to V_{DD}, C_{LOAD}=20pf
Row input fall to ϕ_1 rise delay	t_{D5}	0.0	—	—	μS	
ϕ_2 fall to ϕ_1 rise delay	t_{D6}	0.0	—	—	μS	
Row input fall to column address and/or $\overline{CS}$ change delay	t_{D7}	0.0	—	—	μS	
ϕ1, chip select, and column address overlap	t_{OL1}	0.2	—	—	μS	
ϕ_2 and row input overlap	t_{OL2}	0.2	—	—	μS	
Row input pulse rise time	t_{RP}	0.5	—	—	μS	
Number of read accesses/word subsequent to data being written	N_R	200×10^3	—	—		
Erase Cycle						
Row input erase pulse width	t_E	160	—	—	ms	
Write Cycle						
ϕ_1 pulse width	$t_{\phi 2}$	0.5	—	—	μS	
Row input write pulse width	t_W	5	10	15	ms	
ϕ_1 fall to row input write pulse rise delay	t_{D8}	0.0	—	—	μS	
Column address change to row input write pulse rise delay	t_{D9}	0.7	—	—	μS	
Data input change to row input write pulse rise delay	t_{D10}	0.0	—	—	μS	
Row input write pulse fall to ϕ_1 rise delay	t_{D11}	0.0	—	—	μS	
ϕ_1 and write input overlap	t_{OL3}	0.2	—	—	μS	
Number of times word may be rewritten	N_W	—	—	7×10^4		
Capacitance						
Row input capacitance	C_R	32	37	42	pf	V_{IN}=V_{SS} Volts f=1 MHz All other pins grounded (V_{SS})
Column address capacitance	C_C	—	5	7	pf	
Write input capacitance	C_W	—	3	7	pf	
ϕ_1 capacitance	$C\phi_1$	—	3	7	pf	
ϕ_2 capacitance	$C\phi_2$	—	2	7	pf	
Data In/Out capacitance	C_D	—	4	7	pf	
Chip Select capacitance	C_S	—	5	7	pf	

**Typical values are at +25° C and nominal voltages.

TIMING DIAGRAMS

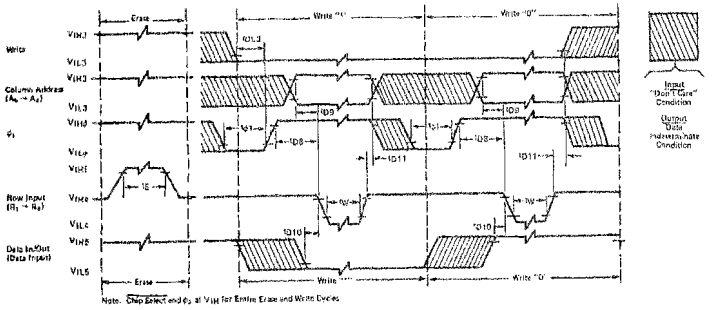


Fig.1 ERASE AND WRITE CYCLE

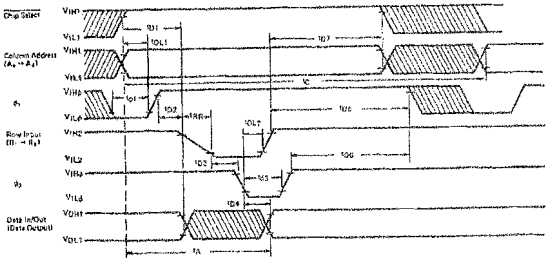


Fig.2 READ CYCLE

APPLICATION EXAMPLE

Figure 4 illustrates a 1024-word by 4-bit memory implementation employing four 1305 EAROM's in a wire-OR'd configuration. Each row input is driven by individual external row driver circuits, shown in figure 5. Erase voltage and write voltage, required as inputs to the row driver circuits, are generated by the circuits shown and need be implemented only once per system (as indicated in figure 4) unless selective erasure by row is desired.

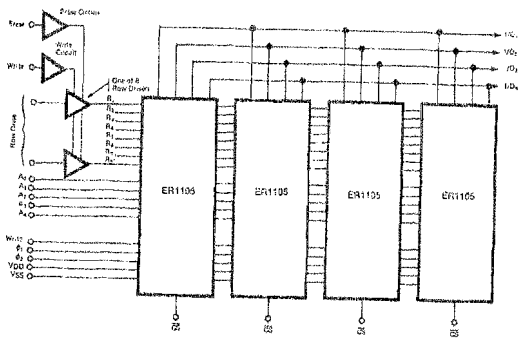


Fig.4 1024 WORD X 4 BIT MEMORY

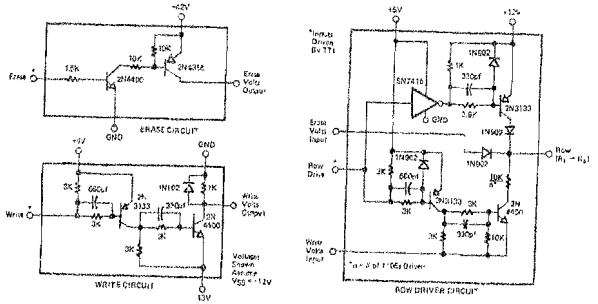


Fig.5 SUGGESTED ROW, ERASE AND WRITE CIRCUITS

1400 Bit Electrically Alterable Read Only Memory

FEATURES

- 100 Word x 14 bit organization
- Word alterable
- 10 years unpowered data storage
- Write/Erase time 100ms/word
- Single -35 volt supply
- No voltage switching required
- MOS compatible signal levels

DESCRIPTION

The ER1400 is a serial input/output 1400 bit electrically erasable and reprogrammable ROM, organized as 100 words of 14 bits each. Data and address are communicated in serial form via a one-pin bidirectional bus.

Addressing is by two consecutive one-of-ten codes.

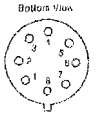
Mode selection is by a 3 bit code applied to C1, C2 and C3.

Data is stored by internal negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 1400 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATION

Standard package
8 LEAD TO-99

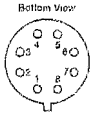
Bottom View



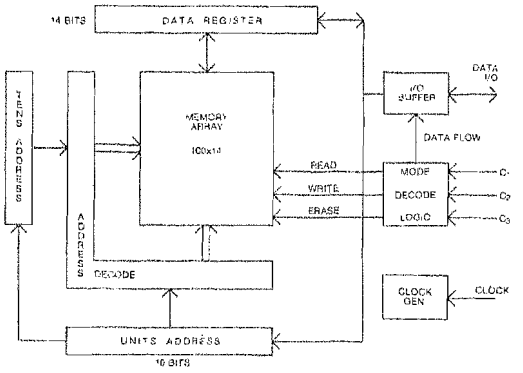
1. Data I/O
2. V_{SS}
3. V_{DD}
4. V_{GG}
5. Clock
6. C1
7. C2
8. C3

Special order package
8 LEAD TO-8

Bottom View



BLOCK DIAGRAM



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PIN FUNCTIONS

Pin No.	Name	Function
1	Data	In the Accept Address and Accept Data modes, this pin is an input pin for address and data respectively. In the Shift Data Out mode this pin is an output pin designed to drive MOS. In Standby, Read, Erase and Write, this pin is left floating.
2	V_M	Used for testing purposes only. Must be left unconnected for normal operation.
3	V_{SS}	Chip substrate. Normally connected to ground.
4	V_{GG}	DC supply. Normally connected to -35 volt supply.
5	Clock	14KHz timing reference. Required for all operations. May be left at logic zero when device is in standby.
6,7,8	C1, C2, C3	Mode control pins. Their operation is as follows.

C1	C2	C3	Function
0	0	0	Standby - contents of Address and Data Register remains unchanged. Output buffer is left floating.
0	1	1	Accept Address - Data presented at the I/O pin is shifted into the Address Register with each clock pulse
1	0	0	Read - The address word is read from memory into the data register.
1	0	1	Shift Data Out - The output driver is enabled and the contents of the Data Register are shifted out one bit with each clock pulse
0	1	0	Erase - The word stored at the addressed location is erased to all zeros.
1	1	1	Accept Data - The data register accepts serial data presented at the I/O pin. The Address Register remains unchanged
1	1	0	Write - The word contained in the Data Register is written into the location designated by the Address Register.
0	0	1	Not Used

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs
(except V_{GG}) with respect to V_{SS} ..... -20V to +0.3V
V_{GG} with respect to V_{SS} ..... +0V
Storage temperature (No Data Retention) ..... -65°C to +150°C
Storage temperature (with Data Retention)
Operating ..... -25° to +75°C
Unpowered ..... -65°C to +80°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)
V_{SS} = GND
V_{GG} = -35V ± 6%
Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Symbol	Min	Typ**	Max	Units
DC CHARACTERISTICS					
Input logic "1"	VIL	V_{SS} -15.0	—	V_{SS} -6	Volts
Input logic "0"	VIH	V_{SS} -1.0	—	V_{SS} +0.3	Volts
Output logic "1" (1 meg, 100 pf load)	VOL	—	—	V_{SS} -12.0	Volts
Output logic "0"	VOH	V_{SS} -1.0	—	V_{SS} +0.3	Volts
Power		—	—	300	mW
AC CHARACTERISTICS					
Clock Frequency	fØ	11.2	14.0	16.8	KHz
Write time	tw	16.0	20.0	24.0	ms
Erase	te	16.6	20.0	24.0	ms
Rise, fall time	tr, tf	—	—	1.0	µs
Propagation delay	tpw	—	—	20.0	µs
Unpowered non-volatile data storage	T_S	10	—	—	Years
Number of erase/write cycles	N_W	—	—	10^5	—
Number of read accesses between writes	N_{RA}	10^6	—	—	—

**Typical values are at +25° C and nominal voltages

TIMING DIAGRAMS

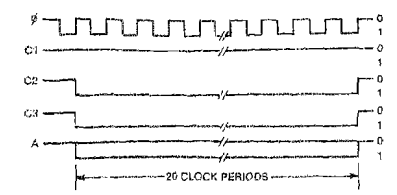

Fig.1 ACCEPT ADDRESS*

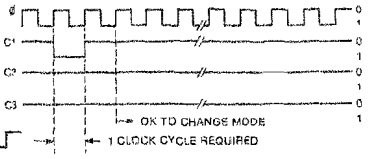

Fig.2 READ

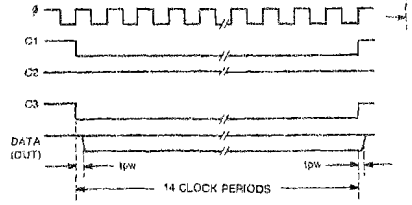

Fig.3 SHIFT DATA OUT*

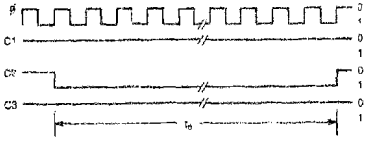

Fig.4 ERASE

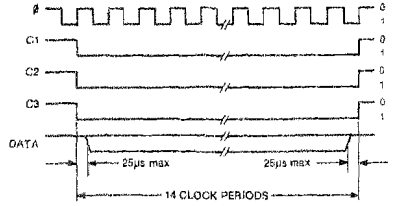

Fig.5 ACCEPT DATA*

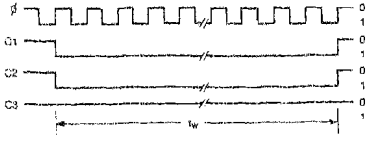

Fig.6 WRITE

*Output data changes on the positive-going clock edge. Data and address inputs are shifted on the negative-going clock edge.

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4096 Bit Electrically Alterable Read Only Memories

FEATURES

- 1024 x 4 Organization
- 10-Bit Binary Addressing
- 2 Chip Select Inputs
- Electrically Reprogrammable
- 2 μs Access Time (ER2401A), 2.4 μs (ER2401)
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2×10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs (Strobed on ER2401)
- Unpowered, Nonvolatile Data Storage—10 Years at +70° C
- Control, Address and Data Inputs TTL Compatible

NOTE: Use ER2401A for all new designs

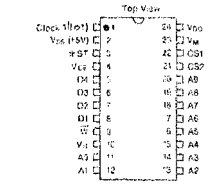
DESCRIPTION

The ER2401 and ER2401A are fully decoded 1024 × 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 4096 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

PIN CONFIGURATION

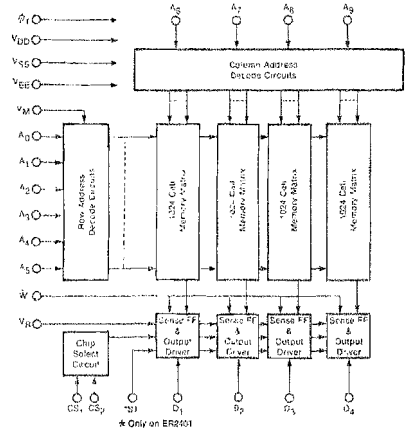
24 LEAD DUAL IN LINE



* NC on ER2401A

Stored data may be accessed a minimum of 2×10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}-28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^5 times. All outputs are at logic high when the device is in the erased state.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS}	+0.3V to −30V
Operating ambient temperature	0° C to +70° C
Storage temperature	−65° C to +150° C
Soldering temperature of leads (10 seconds)	+300° C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

RECOMMENDED OPERATING CONDITIONS, T_A = 0° C to +70° C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}+0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{SS}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	—	V_{SS}	—	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	—	V_{SS}	—	V_{SS}	V_{SS}	V_{SS}	V_{GG}-20	V_{SS}-19	V_{SS}-18	V
V_{EEH}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{EEL}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{WL}	Write control input low	V_{SS}-29	—	V_{SS}-4.4	V_{SS}-29	—	V_{SS}-4.4	Not Applicable			V
$V\phi_H$	ϕ_1 input high voltage	—	V_{SS}	—	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V\phi_L$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
*V_{STH}	Strobe input high voltage	—	V_{SS}	—	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
*V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	—	V_{SS}-4.4	V_{DD}	—	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	—	V_{SS}-4.4	Not Applicable			V

*Strobe only on ER2401.

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0° C to +70° C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{IN}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1 = V_{DD} = V_{SS}$-20	—	—	-2.0	μA
$I_{\phi 1}$	ϕ_1 leakage current at V_{SS}-29V	*$V_{DD} = V_{SS}$-29, $ST = \overline{W} = V_{SS}$-25	—	—	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	—	—	-10.0	μA
I_{EEL}	Erase substrate leakage current at V_{SS}-28V	*W=ST=V_{SS}-25	—	—	-200	μA
I_{DD1}	V_{DD} supply current - read mode at V_{SS}-19V	Outputs open (See Figure 6)	—	8.5	12	mA
I_{DD2}	V_{DD} supply current - write mode at V_{SS}-28V	Outputs open (See Figure 6)	—	18	25	mA
I_{OH}	Data output high current - TTL load	One Series 7400 TTL load with R_E=2KΩ, $V_{CC} = V_{TH}$ (See TTL Notes)	-2.0	—	—	mA
I_{OL}	Data output low current - TTL load		+3.2	—	—	mA
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	—	—	V
V_{OL}	Data Output low voltage — MOS	C_L=100 pF	—	—	V_{SS}-10	V
T_S	Unpowered nonvolatile data storage	Typical write conditions	10	—	—	Years

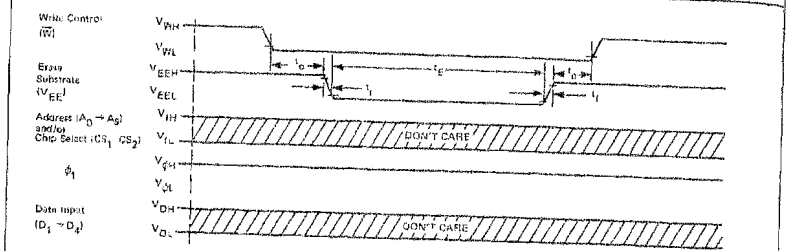
*Strobe only on ER2401

CAPACITANCE AT $V_{IN} = V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	—	5	7	pf
C_W	Write control input capacitance	—	10	20	pf
*C_{ST}	Strobe input capacitance	—	10	15	pf
$C\phi_1$	ϕ_1 Input Capacitance	—	40	50	pf
C_{EE}	Erase substrate capacitance	—	500	700	pf
C_D	Data input/output capacitance	—	6	10	pf

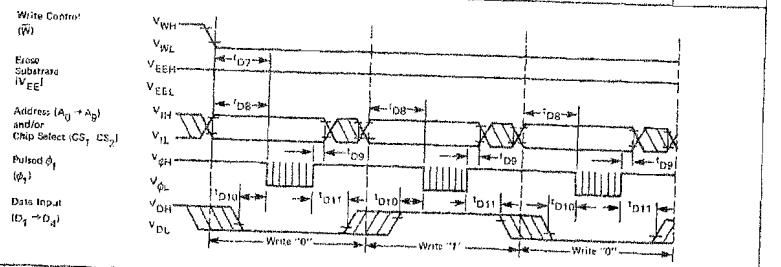
*Strobe only on ER2401.

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_o	Write-erase overlap	10	—	—	μs



WRITE CYCLE CHARACTERISTICS, T_A = 0°C to +70°C ($ST = V_{DD}$ for ER2401) (SEE NOTE 3)

Symbol	Parameter	Min	Typ	Max	Units
$N_{\phi w}$	Number of ϕ_1 write pulses at 100 μs ±10%, 5 μs min. dead time between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	μs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	μs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	μs
N_W	Number of times word may be rewritten	—	—	10^5	—

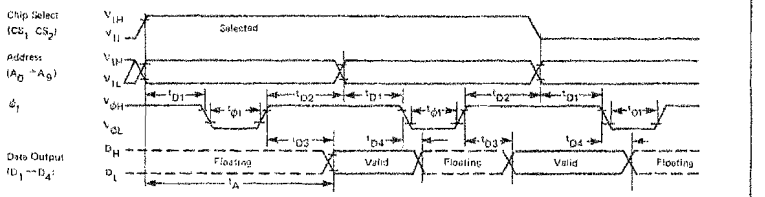


NOTES:

1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 μsec. may result in a floated output condition. Consequently data must be resampled with a 40 μsec. time period following the fall of ϕ_1 to ensure its validity
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes.
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected
4. All typical values are at +25°C and nominal voltages.

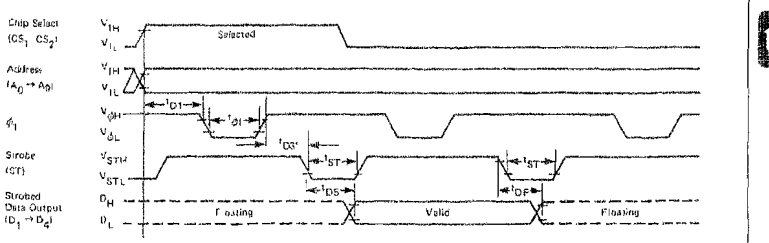
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, T_A = 0°C to +70°C ($ST = V_{DD}$ for ER2401)

Symbol	Parameter (See Figures 1 through 4)	Min	Typ	Max	Units
T_A	Access time (ER2401A)	—	—	2.0	μs
T_A	Access time (Strobe = V_{DD} for ER2401)	—	—	2.4	μs
$t_{\phi 1}$	Pulse width (rise and fall times ≤50 ns) (See Note 1)	850	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	400	—	—	ns
t_{D2}	ϕ_1 Fall to address and chip select change delay	0.0	—	—	μs
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)	—	—	750	ns
t_{D4}	ϕ_1 Rise to floated output delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION (ER2401 only) T_A = 0°C to +70°C

Symbol	Parameter (See Figure 1 through 4)	Min	Typ	Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ≤50 ns) (See Note 1)	850	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	400	—	—	ns
t_{D2}	ϕ_1 Fall to strobe rise delay	0.75	—	—	μs
t_{ST}	Strobe pulse width (rise and fall ≤50 ns)	500	—	—	ns
t_{D5}	Strobe rise to strobed data output valid delay (see notes 1 and 2)	—	—	500	ns
t_{D6}	Strobe rise to strobed floated output on deselect delay	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	—



TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C, R_L = 2K Ohms, V_{SS} = 0V

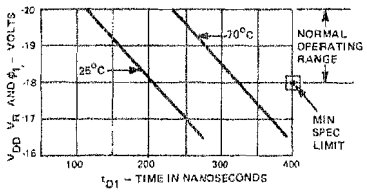


Fig.1 TYPICAL ϕ1 DELAY IN NANOSECONDS VS. POWER SUPPLY VOLTAGE

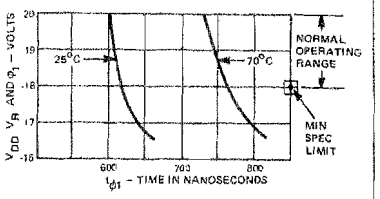


Fig.2 TYPICAL ϕ1 WIDTH IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

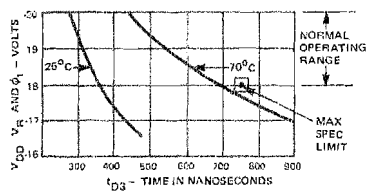


Fig.3 TYPICAL DATA SETUP TIME IN NANOSECONDS VS. POWER SUPPLY VOLTAGES

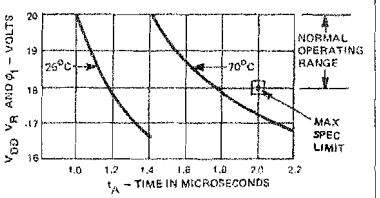


Fig.4 TYPICAL ACCESS TIME IN MICROSECONDS VS. POWER SUPPLY VOLTAGES

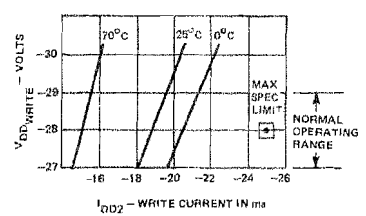


Fig.5 TYPICAL WRITE CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGES (For deselected, I_{DD2} = ½ Graph I_{DD2})

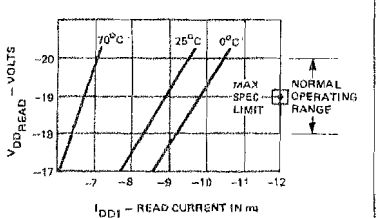


Fig.6 TYPICAL READ CURRENT IN MILLIAMPS VS. POWER SUPPLY VOLTAGE (Chip selected or deselected)

PIN FUNCTIONS

Chip Select (CS1, CS2)
Both must be in the high state to enable the data output terminals or write data into the device.

Data Input/Output (D1—D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition.

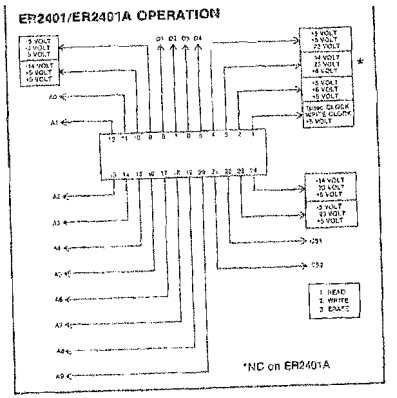
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device.

Strobe (ST) ER2401 only
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle. The ST input is high-level and not TTL-compatible.

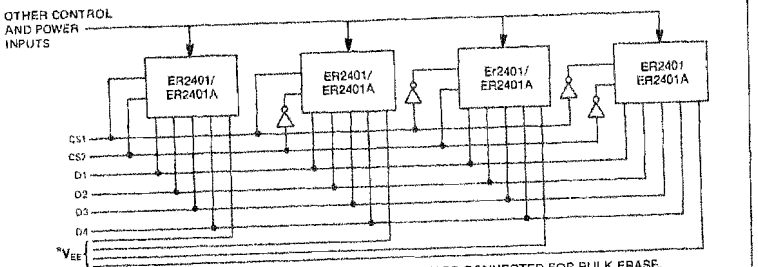
Phase One (ϕ1)
During the write operation, multiple 100µs pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltge to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible.

NOTE. All control, address and data inputs are TTL-compatible with pull-up resistors.

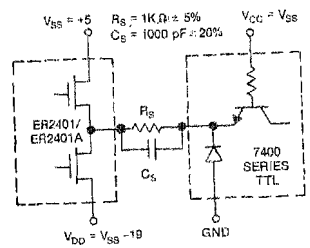
ER2401/ER2401A OPERATION



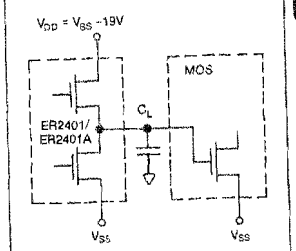
A 4096 × 4 EAROM SUBSYSTEM ORGANIZATION



TTL INTERFACE



MOS INTERFACE



12

4096 Bit High Speed Electrically Alterable Read Only Memories

FEATURES

- 1024 x 4 Organization, Fully Decoded
- Single Word or Block Electrically Erasable
- TTL Compatible with Resistor Pull-ups
- Three State Output
- ER3400: 650ns Access Time
- ER3401: 950ns Access Time
- 1.8 us Cycle Time
- 10 ms Word or Block Erase Time
- 1 ms Write Time
- 22 Pin DIP
- P-Channel Metal Gate MNOS Technology
- 0°C to 70°C Operation
- +5, -12, -30V Power Supplies
- 10^5 Erase-Write Cycles per Word
- 2×10^{11} Read Cycles per Word
- 10 Year Unpowered Nonvolatile Data Storage — 10 Years

DESCRIPTION

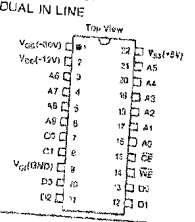
The ER3400 and ER3401 are word alterable ROMs intended for use as read-mostly memories. Each operates with one clock, CHIP ENABLE ($\overline{CE}$), which also serves for chip selection. All other pins of each device can be paralleled with other EAROMs.

Any one of four possible operating modes can be selected by setting the proper binary code on the C0-C1 control lines and pulsing the device with $\overline{CE}$. The four modes are Read, Write, Word Erase and Block Erase. The ER3400/3401 will sense the control lines and change modes only when pulsed by $\overline{CE}$. When in the Read mode, data is read during each $\overline{CE}$ pulse. Writing or erasing of a word continues for as long as the device is in the Write or Erase mode. Each write or erase word cycle must be ended by a dummy read operation.

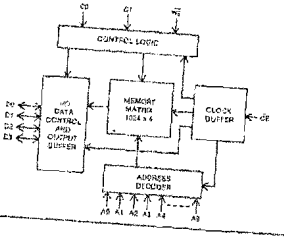
A WRITE ENABLE ($\overline{WE}$) input pulse indicates to the ER3400/3401 that the data on the D_0-D_3 data input/output lines is valid input data. This data is then stored internally for use during the write operation.

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



No particular order of power supply sequencing on or off is required for the ER3400. Circuits are provided to force the device into the read mode during power turn on. Erasing and writing are inhibited if V_{DD} or V_{GG} are not at proper operating levels.

For the ER3401, V_{GG} must be turned on after V_{CC} is stable and removed before V_{CC} is turned off.

PIN FUNCTIONS

A_0-A_9	10-Bit Word Address
D_0-D_3	Data input and output pins
$\overline{CE}$	Chip Enable. Chip selected when $\overline{CE}$ is pulsed to logic "0".
C_0, C_1	Mode Control Inputs C0 C1 0 1 Block Erase Mode: erase operation performed on all words 1 1 Word Erase Mode: stored data is erased at addressed location. 0 0 Read Mode: addressed data read after leading edge of $\overline{CE}$ pulse 1 0 Write Mode: input data written at addressed location.
$\overline{WE}$	Write Enable. Input data read when $\overline{WE}$ is pulsed to logic "0".
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input
V_{DD}	Power Supply Input. Normally at -12 volts
V_{GG}	Power Supply Input. Normally at -30 volts

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs (with respect to V_{SS}) ..... +40V to +0.3V
Storage temperature (with data retention) ..... -40°C to +70°C
Storage temperature (without data retention) ..... -65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{SS} = +5V ±5%
V_{DD} = -12V ±5%
V_{GG} = -30V ±5%
V_{GI} = GND
Operating Temperature (T_A) = 0°C to +70°C

Characteristic	Symbol	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Input Logic "1"	V_{IH}	V_{SS}-1.5	—	V_{SS}+0.3	Volts	
Input Logic "0"	V_{IL}	-10	—	0.8	Volts	
Output Logic "1"	V_{OH}	V_{SS}-1.5	—	—	Volts	I_{OH} = -2mA
Output Logic "0"	V_{OL}	—	—	0.4	Volts	I_{OL} = 2mA
Control Input Leakage	I_{LC}	—	—	-2.0	µA	V_{IN} = V_{SS} -15 Volts
Data Input Leakage	I_{LD}	—	—	-10.0	µA	V_{IN} = V_{SS} -15 Volts
Power Supply Current						
V_{DD} Supply Current: Chip selected	I_{DD}	—	—	-25.0	mA	V_{DD} = V_{SS} -17 Volts
Chip de-selected	I_{DD}	—	—	-7.0	mA	V_{DD} = V_{SS} -17 Volts
V_{GG} Supply Current	I_{GG}	—	—	-3.0	mA	V_{GG} = V_{SS} -35 Volts
V_{SS} Supply Current: Chip selected	I_{SS}	—	—	-29.0	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
Chip de-selected	I_{SS}	—	—	-11.5	mA	V_{DD} = V_{SS} -17V, V_{GG} = V_{SS} -35V
AC CHARACTERISTICS						
Input capacitance - control inputs	C_I	—	6	8	pf	
Input capacitance - data inputs	C_D	—	6	10	pf	
Read Mode Characteristics						
Address and control to $\overline{CE}$	t_{D1}	0	—	—	ns	
Address and control hold time	t_{D2}	250	—	—	ns	
$\overline{CE}$ to Data I/O Off	t_{D3}	50	—	200	ns	
$\overline{CE}$ high	t_{D4}	900	—	—	ns	
Access time: ER3400	t_A	—	—	650	ns	RL = 2K to V_{SS}, CL = 100pf
ER3401	t_A	—	—	950	ns	
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
Read cycle time	t_{CY}	1550+t_r+t_f	—	—	—	
$\overline{CE}$ rise, fall time	t_r, t_f	0	—	100	ns	
Write/Erase Mode Characteristics						
Address and control to $\overline{CE}$	t_{D11}	0	—	—	ns	
Address and control hold time	t_{D12}	250	—	—	ns	
$\overline{CE}$ fall to $\overline{WE}$ fall delay	t_{D13}	0	—	—	ns	$\overline{WE}$ rise may overlap $\overline{CE}$ rise by a maximum of 50ns
$\overline{WE}$ rise to $\overline{CE}$ rise delay	t_{D14}	-50	—	—	ns	
Data stable to $\overline{WE}$	t_{D15}	0	—	—	ns	
$\overline{WE}$ rise to End of Data Stable	t_{D16}	50	—	—	ns	
$\overline{CE}$ pulse width: ER3400	$t_{\overline{CE}}$	650	—	100000	ns	
ER3401	$t_{\overline{CE}}$	950	—	100000	ns	
WE pulse width	$t_{\overline{WE}}$	400	—	—	ns	
Write time	t_W	1	—	2	ms	
Erase time	t_E	10	—	20	ms	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

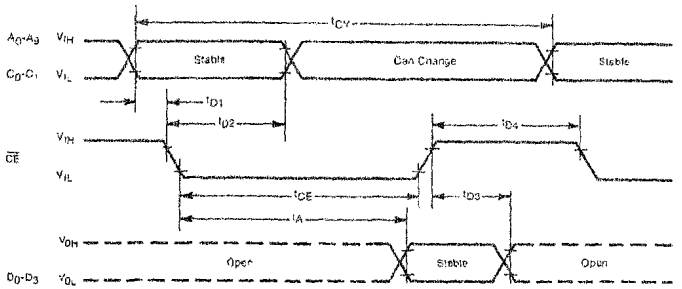


Fig.1: READ MODE TIMING

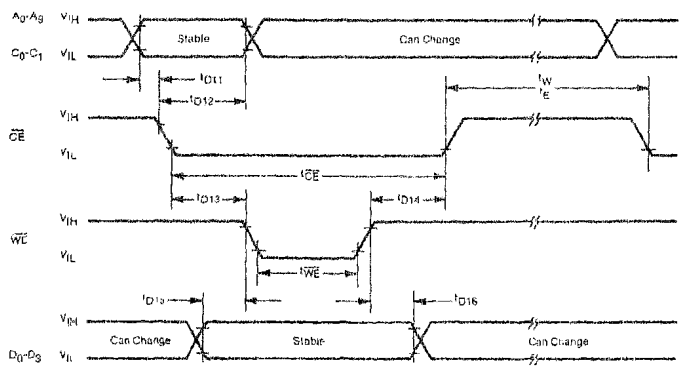


Fig.2: WRITE AND ERASE MODE TIMING

TYPICAL CHARACTERISTIC CURVES

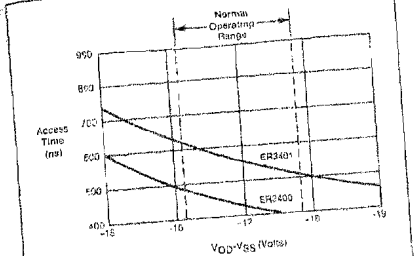


Fig.3: TYPICAL ACCESS TIME vs. POWER SUPPLY VOLTAGE @ 25° C

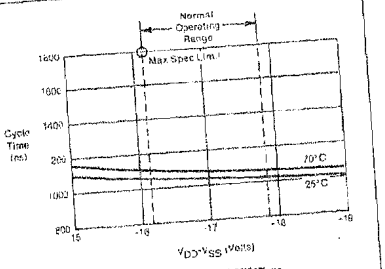


Fig.4: TYPICAL CYCLE TIME vs. POWER SUPPLY VOLTAGE

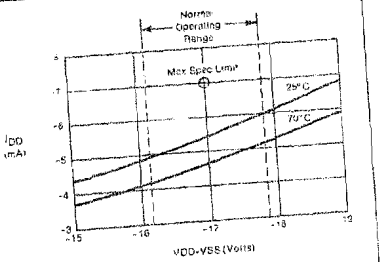


Fig.5: I_{DD} vs. V_{DD}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

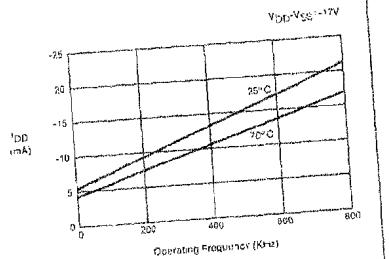


Fig.6: I_{DD} vs. OPERATING FREQUENCY IN READ MODE AND SELECTED

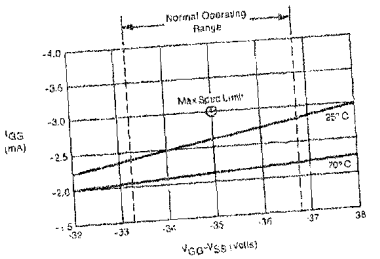


Fig.7: I_{GG} vs. V_{GG}-V_{SS} POWER SUPPLY VOLTAGE IN READ MODE AND NOT SELECTED

12

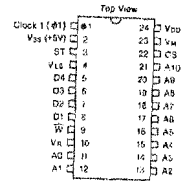
8192 Bit Electrically Alterable Read Only Memories

FEATURES

- 2048 x 4 Organization
- 11-Bit Binary Addressing
- Chip Select Input
- Electrically Reprogrammable
- 2.8 μs Access Time (ER2800)
- 1.65 μs Access Time (ER2805)
- 20 ms/4-bit Word Write Time
- 100 ms Simultaneous Erasure of All Data
- Minimum Data Retention—2 x 10^{11} Read Accesses/Word Between Refresh
- Three-State Outputs
- Unpowered, Nonvolatile Data Storage—10 Years at +70°C
- Control, Address and Data Inputs TTL Compatible.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



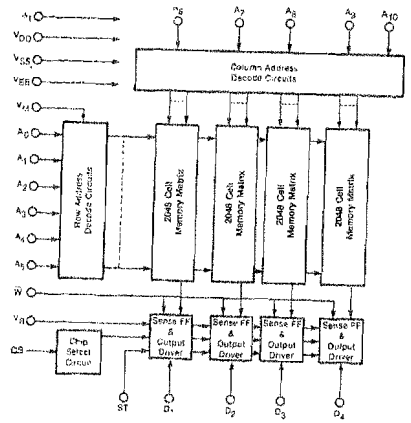
DESCRIPTION

The ER2800 and ER2805 are fully decoded 2048 × 4-bit electrically erasable and reprogrammable ROMs utilizing second-generation MNOS epitaxial processing technology.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface at the gate insulator of the 8192 MNOS memory transistors. When the writing voltage is removed, the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

Stored data may be accessed a minimum of 2×10^{11} times without refresh and is non-volatile in the unpowered state in excess of ten years. Data is erased by applying a V_{SS}+28V pulse to the erase substrate of the device. Data can be erased and rewritten up to a maximum of 10^5 times. All outputs are at logic high when the device is in the erased state

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs or outputs relative to V_{SS}	+0.3V to -30V
Operating ambient temperature	0°C to +70°C
Storage temperature	-65°C to +150°C
Soldering temperature of leads (10 seconds)	+300°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

RECOMMENDED OPERATING CONDITIONS, T_A = 0°C to +70°C

Symbol	Parameter	Erase Mode			Write Mode			Read Mode			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{DD}	Supply Voltage	4.75	V_{SS}	V_{SS}-0.3	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{BB}	Substrate supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_M	Memory voltage	--	V_{SS}	--	V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-10.5	V_{SS}-10	V_{SS}-9.5	V
V_R	Reference voltage	--	V_{SS}	--	V_{SS}	V_{SS}	V_{SS}	V_{SS}-20	V_{SS}-19	V_{SS}-18	V
V_{LS}	Erase substrate input high	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V_{SS}-0.4	V_{SS}	V_{SS}+0.3	V
V_{LS}	Erase substrate input low	V_{SS}-29	V_{SS}-28	V_{SS}-27	Not Applicable			Not Applicable			V
V_{WH}	Write control input high	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_W	Write control input low	V_{SS}-29	--	V_{SS}-4.4	V_{SS}-29	--	V_{SS}-4.4	Not Applicable			V
$V_{\phi 1}$	ϕ_1 input high voltage	--	V_{SS}	--	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V_{SS}-0.8	V_{SS}	V_{SS}+0.3	V
$V_{\phi L}$	ϕ_1 input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{STH}	Strobe input high voltage	--	V_{SS}	--	Not Applicable			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{STL}	Strobe input low voltage	Not Applicable			V_{SS}-29	V_{SS}-28	V_{SS}-27	V_{SS}-25	V_{SS}-19	V_{SS}-18	V
V_{IH}	Address and CS input high	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V_{SS}-1.5	V_{SS}	V_{SS}+0.3	V
V_{IL}	Address and CS input low	Don't Care			V_{DD}	--	V_{SS}-4.4	V_{DD}	--	V_{SS}-4.4	V
V_{DH}	Data input high voltage	Don't Care			V_{SS}-1.5	V_{SS}	V_{SS}+0.3	Not Applicable			V
V_{DL}	Data input low voltage	Don't Care			V_{DD}	--	V_{SS}-4.4	Not Applicable			V

STATIC ELECTRICAL CHARACTERISTICS, T_A = 0°C to +70°C (NO EXTERNAL LOADS EXCEPT AS NOTED)

Symbol	Parameter	Conditions All Pins at V_{SS} Unless Noted	Min	Typ	Max	Unit
I_{LI}	Input leakage current (except pins 1, 2, 4, 5, 6, 7, 8, and 24) at V_{SS}-15V	$\phi 1 = V_{DD} = V_{SS}$-20	--	--	-2.0	μA
$I_{\phi 1}$	ϕ_1 leakage current at V_{SS}-29V	$V_{DD} = V_{SS}$-29, ST=W=V_{SS}-25	--	--	-200	μA
I_O	Output leakage current at V_{SS}-15V	Chip deselected	--	--	-10.0	μA
I_{LLS}	Erase substrate leakage current at V_{SS}-28V	W=ST=V_{SS}-25	--	--	-200	μA
I_{DD_1}	V_{DD} supply current - read mode at V_{SS}-19V	ER2800	--	6.5	12	mA
		ER2805	--	11	13	mA
I_{DD_2}	V_{DD} supply current - V_{SS} = -28V	ER2800	--	18	25	mA
		ER2805	--	24	27	mA
I_{OH}	Data output high voltage - TTL load	One Series 7400 TTL load with R_S = 1KΩ, V_{CC}=V_{SS} (See TTL Notes)	V_{SS}-1.5	--	--	V
I_{OL}	Data output low voltage - TTL load		--	--	V_{SS}-6.6	V
V_{OH}	Data Output high voltage - MOS		V_{SS}-1.5	--	--	V
V_{OL}	Data Output low voltage -- MOS	C_L=100 pF	--	--	V_{SS} -7	V
T_r	Unpowered nonvolatile data storage	Typical write conditions	10	--	--	Years

CAPACITANCE AT $V_{IN} = V_{SS}$, ALL OTHER PINS GROUNDED (V_{SS}), f=1 MHz

Symbol	Parameter	Min	Typ	Max	Unit
C_I	Address and chip select input capacitance	--	5	7	pf
C_W	Write control input capacitance	--	10	20	pf
C_{ST}	Strobe input capacitance	--	10	15	pf
$C_{\phi 1}$	ϕ_1 Input Capacitance	--	40	50	pf
C_{LS}	Erase substrate capacitance	--	600	700	pf
C_D	Data input/output capacitance	--	6	10	pf

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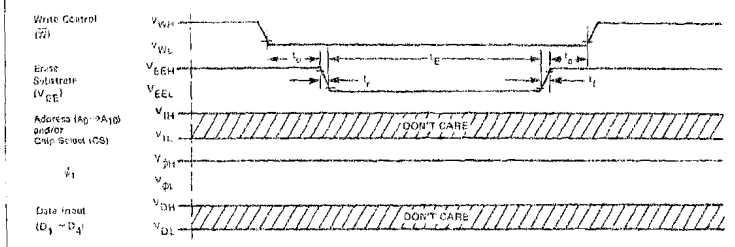
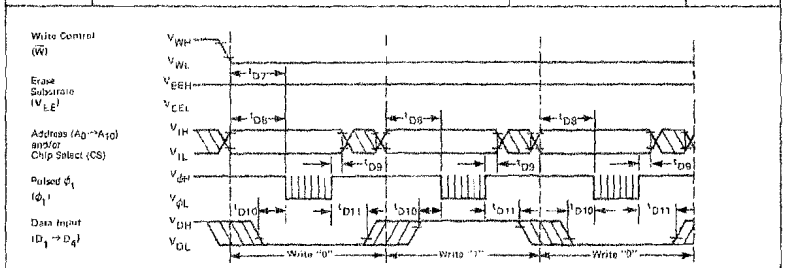
CHARACTERISTICS, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_E	V_{EE} erase pulse width	100	—	1000	ms
t_r, t_f	V_{EE} rise time, V_{EE} fall time	0.01	—	1.0	ms
t_c	Write-erase overlap	10	—	—	µs



WRITE CYCLE CHARACTERISTICS, T_A=0°C to +70°C ($\overline{ST}$=V_{DD}) (SEE NOTE 3)

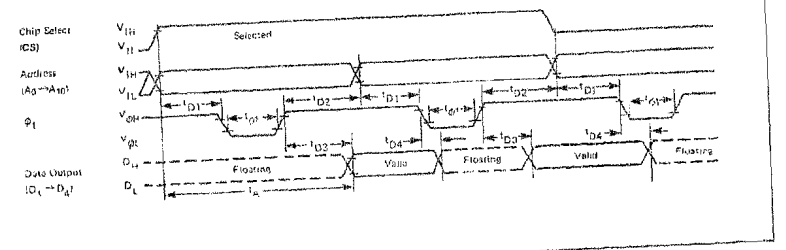
Symbol	Parameter	Min	Typ	Max	Units
$N_{\phi W}$	Number of ϕ_1 write pulses at 100 µs ±10%, 5 µs min. deadtime between pulses)	100	200	300	Pulses
t_{D7}	Write control rise to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D8}	Address change and chip select fall to pulsed ϕ_1 rise delay	500	—	—	ns
t_{D9}	Pulsed ϕ_1 fall to address and chip select change delay	0.0	—	—	µs
t_{D10}	Data input change to pulsed ϕ_1 rise delay	0.0	—	—	µs
t_{D11}	Pulsed ϕ_1 fall to data input change delay	0.0	—	—	µs
N_W	Number of times word may be rewritten	—	—	10[3]	—



NOTES
1. Due to the dynamic nature of the circuit a "ϕ_1 NOT" time in excess of 40 µsec may result in a floated output condition. Consequently data must be resampled with a 40 µsec. time period following the fall of ϕ to ensure its validity
2. Several seconds may be required following a programming operation for the circuit to become operable in the read mode. If data is to be verified immediately following programming, a forward current of +1 mA ±10% may be forced into the erase substrate junction (Pin 4, V_{EE}), for a period not to exceed 10 milliseconds, to quickly dissipate charge trapped at internal circuit nodes
3. Maximum power dissipation occurs during programming. When programming multichip systems where the application of programming voltages is required for several minutes, forced air cooling is recommended to reduce package temperature. Power is not reduced when chip is deselected
4. All typical values are at +25°C and nominal voltages

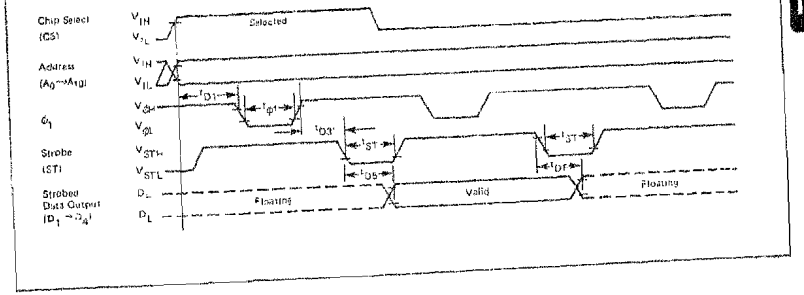
READ CYCLE CHARACTERISTICS FOR NON-STROBED OPERATION, T_A=0°C to +70°C ($\overline{ST}$ = V_{DD})

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
T_A	Access time (strobe=V_{DD})	—	2.0	2.6	—	—	1.65	µs
$t_{\phi 1}$	Pulse width (rise and fall times ⩽50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
t_{D2}	ϕ_1 Fall to address and chip select change delay	0.0	—	—	0.0	—	—	µs
t_{D3}	ϕ_1 Fall to data output valid delay (See Notes 1 and 2)	—	—	950	—	—	550	ns
t_{D4}	ϕ_1 Rise to floated output delay	—	—	900	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



READ CYCLE CHARACTERISTICS FOR STROBED OPERATION, T_A=0°C to +70°C

Symbol	Parameter (See Figures 1 through 4)	ER2800 Min	ER2800 Typ	ER2800 Max	ER2805 Min	ER2805 Typ	ER2805 Max	Units
$t_{\phi 1}$	ϕ_1 Pulse width (rise and fall times ⩽ 50ns) (See Note 1)	950	—	2000	700	—	2000	ns
t_{D1}	Address and chip select change to ϕ_1 rise delay	600	—	—	400	—	—	ns
t_{D3}	ϕ_1 Fall to strobe rise delay	0.75	—	—	0.75	—	—	µs
t_{ST}	Strobe pulse width (rise and fall ⩽50 ns)	500	—	—	500	—	—	ns
t_{D5}	Strobe rise to strobed data output valid delay (See Notes 1 and 2)	—	—	950	—	—	500	ns
t_{DF}	Strobe rise to strobed floated output on deselect delay	—	—	300	—	—	300	ns
N_{RA}	Number of read accesses/word between refresh	2×10^{11}	—	—	2×10^{11}	—	—	—



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ER2800 TYPICAL OPERATING CHARACTERISTICS, T_A = +25°C and +70°C. R_S = 2K Ohms, V_{BS} = OV

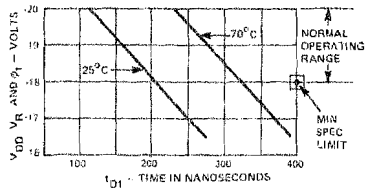


Fig. 1 TYPICAL ϕ1 DELAY IN NANOSECONDS vs. POWER SUPPLY VOLTAGE (ER2800)

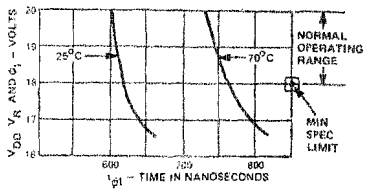


Fig. 2 TYPICAL ϕ1 WIDTH IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

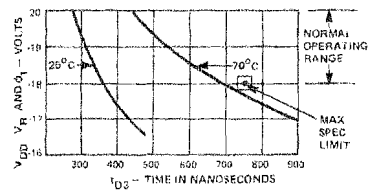


Fig. 3 TYPICAL DATA SETUP TIME IN NANOSECONDS vs. POWER SUPPLY VOLTAGES (ER2800)

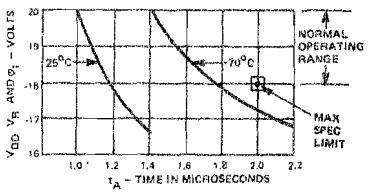


Fig. 4 TYPICAL ACCESS TIME IN MICROSECONDS vs. POWER SUPPLY IN VOLTAGES (ER2800)

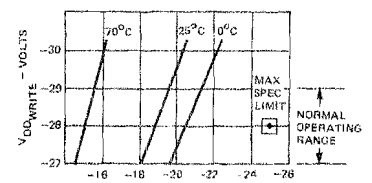


Fig. 5 TYPICAL WRITE CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGES (ER2800) (Deselected I_{DD2} = ¼ Graph I_{DD2})

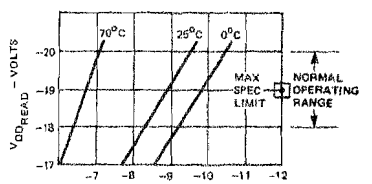


Fig. 6 TYPICAL READ CURRENT IN MILLIAMPS vs. POWER SUPPLY VOLTAGE (ER2800) (Chip selected or deselected)

PIN FUNCTIONS

Chip Select (CS)
Must be in the high state to enable the data output terminals or write data into the device

Data Input/Output (D1–D4)
D1 through D4 are bidirectional data terminals. Data are entered on these terminals during the write cycle and read out during the read cycle. When deselected, these terminals are in a floating condition

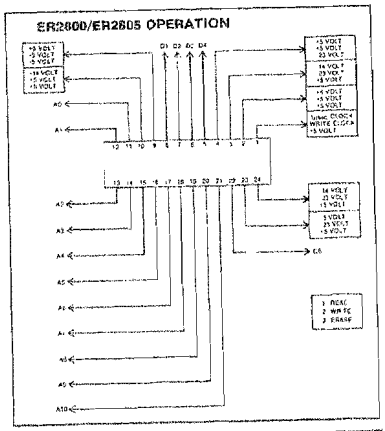
Write Control ($\overline{W}$)
The write control terminal must be in the low state in order to write data into the device

Strobe (ST)
A strobe input is provided for delayed data clockout. In applications where this feature is not desired, the strobe terminal should be maintained at VDD throughout the entire read cyle The ST input is high-level and not TTL-compatible

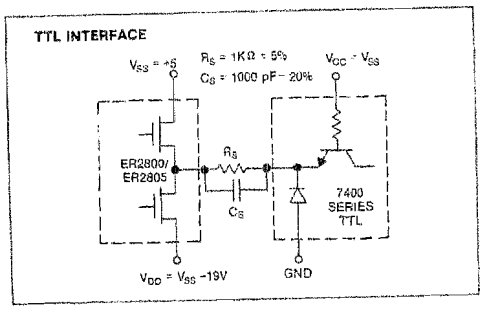
Phase One (ϕ1)
During the write operation, multiple 100µs pulses must be applied to the ϕ1 terminal to fully shift the memory transistor threshold voltge to its most negative state. This is required for voltage bootstrapping in the row-selection circuitry. The ϕ1 input is high level and not TTL-compatible

NOTE All control, address and data inputs are TTL-compatible with pull-up resistors

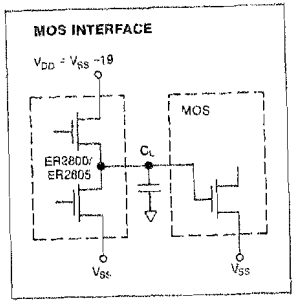
ER2800/ER2805 OPERATION



TTL INTERFACE



MOS INTERFACE



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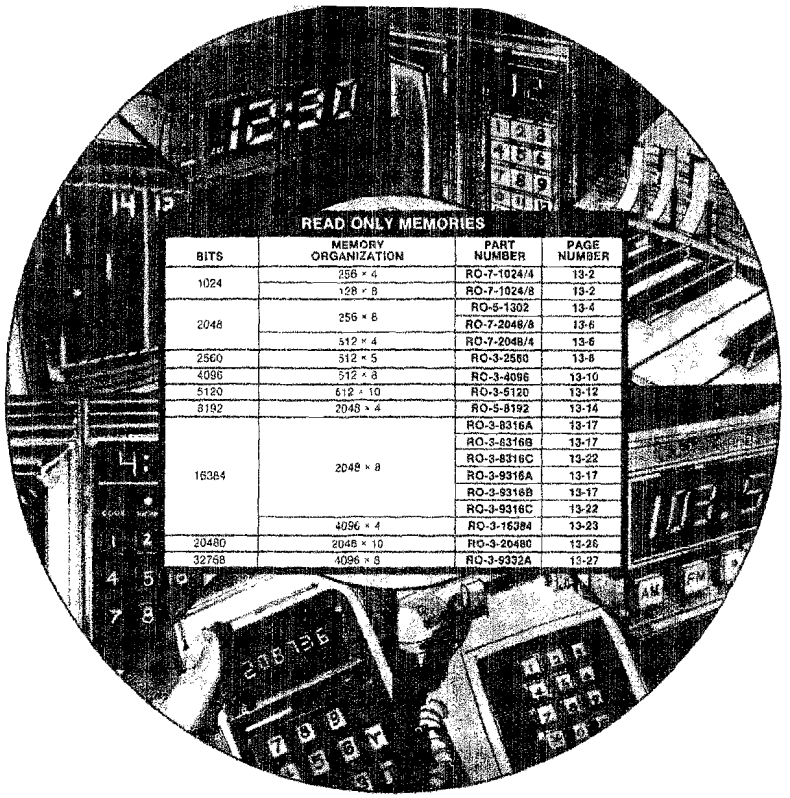

READ ONLY MEMORIES

BITS	MEMORY ORGANIZATION	PART NUMBER	PAGE NUMBER
1024	256 × 4	RO-7-1024/4	13-2
	128 × 8	RO-7-1024/8	13-2
2048	256 × 8	RO-5-1302	13-4
		RO-7-2048/8	13-6
	512 × 4	RO-7-2048/4	13-6
2560	512 × 5	RO-3-2560	13-8
4096	512 × 8	RO-3-4096	13-10
5120	512 × 10	RO-3-5120	13-12
8192	2048 × 4	RO-5-8192	13-14
16384	2048 × 8	RO-3-8316A	13-17
		RO-3-8316B	13-17
		RO-3-8316C	13-22
		RO-3-9316A	13-17
		RO-3-9316B	13-17
		RO-3-9316C	13-22
	4096 × 4	RO-3-16384	13-23
20480	2048 × 10	RO-3-20480	13-26
32768	4096 × 8	RO-3-9332A	13-27

READ ONLY MEMORIES

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MICRO ELECTRONICS

1024 Bit Static Read Only Memories

FEATURES

- Static operation. No clock required.
- Access time typically 1 μsec.
- Three-State output for wired AND capability.
- Chip enable control.
- Input, Output directly interface with DTL/TTL.
- Choice of Operating Temperature Ranges—
  RO-7: 0°C to +70 °C
  RO-6: -55°C to +125°C

DESCRIPTION

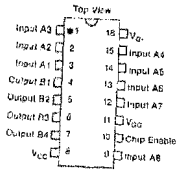
The RO-6-1024/4, RO-7-1024/4, RO-6-1024/8 and RO-7-1024/8 are 1024 bit static Read Only Memories belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect transistors.

The RO-6-1024/4 is packaged in a 16 lead ceramic Dual In Line. The RO-7-1024/4 is the plastic version of this device. The memory organization is 256×4 bit words.

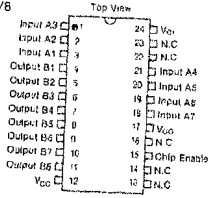
The RO-6-1024/8 is packaged in a 24 lead ceramic Dual In Line. The RO-7-1024/8 is the plastic version of this device. The memory organization is 128×8 bit words.

PIN CONFIGURATIONS

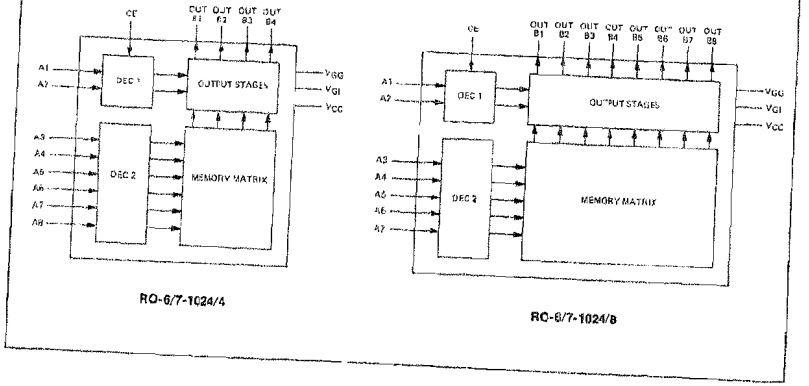
16 LEAD DUAL IN LINE
RO-6/7-1024/4



24 LEAD DUAL IN LINE
RO-6/7-1024/8



BLOCK DIAGRAMS



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} & V_{GG} (with respect to V_{CC})	−20V to +0.3V
Clock & logic inputs (with respect to V_{CC})	−20V to +0.3V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +125°C (RO-6-1024/4/8)
	0°C to +70°C (RO-7-1024/4/8)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

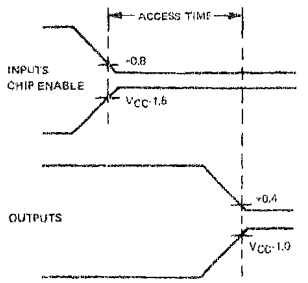
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 1V
V_{GI} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = −55°C to +125°C (RO-6-1024/4/8)
= 0°C to +70°C (RO-7-1024/4/8)

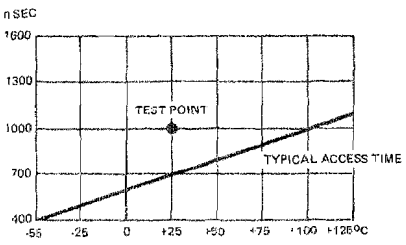
Characteristics	Min.	Typ.**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise Immunity	0.4	—	—	V	
Input Leakage	—	—	1.0	μA	Measured at $V_{IN} = V_{GG}$ at 25°C
Input capacitance	—	5	—	pF	Measured at $V_{IN} = V_{CC}$
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 μA
Access Time					
Address	—	—	1.0***	μs	Measured at 25°C
Chip enable	—	—	1.0***	μs	Measured at 25°C

**Typical values are at +25° C and nominal voltages
*** Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

RO-5-1302

2048 Bit Static Read Only Memory

FEATURES

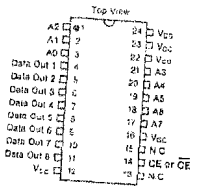
- Static Operation. No clock required.
- Access time typically 1.2 usec.
- Three-state output for wired AND capability.
- Chip enable control.
- Input, Output directly interface with DTL/TTL.

DESCRIPTION

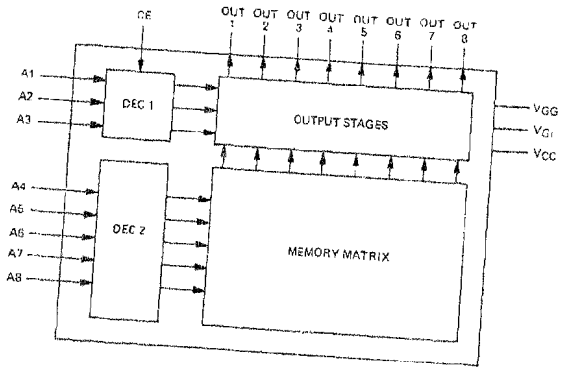
The RO-5-1302 is a 2048 bit fully static Read Only Memory belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect transistors. The RO-5-1302 is packaged in a 24 lead Dual In Line. The memory organization is 256×8 bit words.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{BB} & V_{DD} (with respect to V_{CC}).	−20V to +0.3V
Clock & logic inputs (with respect to V_{CC})	−20V to +0.3V
Storage Temperature.	−55°C to +150°C
Operating Temperature.	0° to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

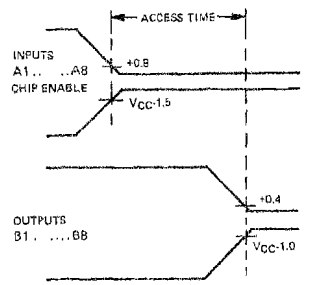
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{DD} = −12V ± 1V
V_{BB} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = 0°C to +70°C

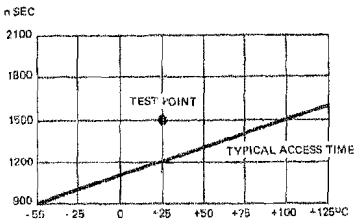
Characteristics	Min	Typ**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise Immunity	0.4	—	—	V	
Input leakage	—	—	1.0	µA	Measured at V_{IN} = V_{DD} at 25°C
Input capacitance	—	5	—	pF	Measured at V_{IN} = V_{CC}
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 µA
Access Time					
Address	—	1.2	1.5***	µs	Measured at 25°C
Chip enable	—	0.8	1.5***	µs	Measured at 25°C

**Typical values are at +25°C and nominal voltages
***Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

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RO-6-2048/4 RO-6-2048/8
RO-7-2048/4 RO-7-2048/8

2048 Bit Static Read Only Memories

FEATURES

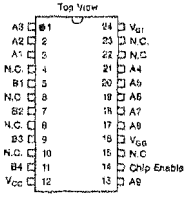
- Static Operation. No clock required
- Access time typically 1.2 usec.
- Three-state output for wired AND capability
- Chip enable control
- Input, Output directly interface with DTL/TLL.
- Choice of Operating Temperature Ranges—
  RO-7: 0° C to +70° C
  RO-6: −55° to +125° C

DESCRIPTION

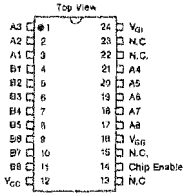
The RO-6-2048/4, RO-7-2048/4, RO-6-2048/8 and RO-7-2048/8 are 2048 bit fully static Read Only Memories belonging to a standard family of DTL/TTL compatible circuits which are constructed using low threshold silicon nitride passivated P-channel enhancement mode field effect ransistors. The RO-6-2048/4 is packaged in a 24 lead ceramic Dual In Line. The RO-7-2048/4 is the plastic version of this device. The memory organization is 512×4 bit words.
The RO-6-2048/8 is packaged in a 24 lead ceramic Duel In Line. The RO-7-2048/8 is the plastic version of this device. The memory organization is 256×8 bit words.

PIN CONFIGURATIONS

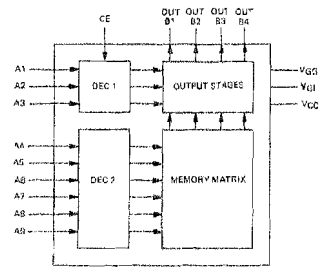
24 LEAD DUAL IN LINE
RO-6/7-2048/4



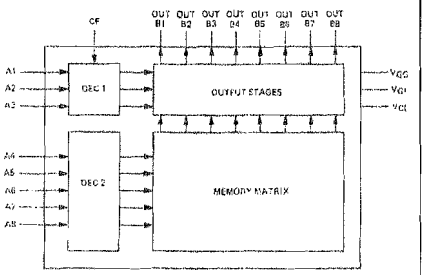
24 LEAD DUAL IN LINE
RO-6/7-2048/8



BLOCK DIAGRAM



RO-6/7-2048/4



RO-6/7-2048/8

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GI} & V_{GG} (with respect to V_{CC})	−20V to +0.3V
Clock & logic inputs (with respect to V_{CC})	−20V to +0.3V
Storage Temperature.	−55°C to +150° C
Operating Temperature.	−55°C to +125° C (RO-6-2048/4/8)
	0° C to +70° C (RO-7-2048/4/8)

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below.

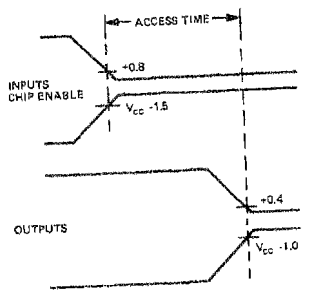
Standard Conditions (unless otherwise noted)

V_{CC} = +5V ± 0.5V
V_{GG} = −12V ± 1V
V_{GI} = GND
(Substrate at V_{CC})
Operating Temperature (T_A) = −55°C to +125° C (RO-6-2048/4/8)
= 0°C to +70° C (RO-7-2048/4/8)

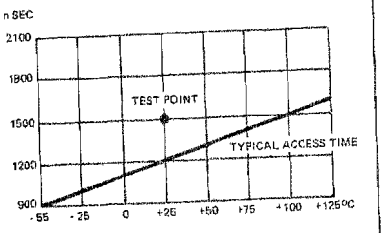
Characteristics	Min	Typ**	Max	Units	Conditions
Data Inputs					
Logic "0" level	—	—	+0.8	V	
Logic "1" level	V_{CC}−1.5	—	—	V	
Noise immunity	0.4	—	—	V	
Input leakage	—	—	1.0	μA	Measured at $V_{IN} = V_{GG}$ at 25°C
Input capacitance	—	5	—	pF	Measured at $V_{IN} = V_{CC}$
Data Outputs					
Logic "0" level	—	—	+0.4	V	I_{OL} = 1.6 mA
Logic "1" level	V_{CC}−1.0	—	—	V	I_{OH} = 100 μA
Access Time					
Address	—	1.2	1.5***	μs	Measured at 25°C
Chip enable	—	0.8	1.5***	μs	Measured at 25°C

**Typical values are at +25°C and nominal voltages
***Testing Conditions

TIMING DIAGRAM



TYPICAL CHARACTERISTIC CURVE



ACCESS TIME VS. TEMPERATURE

13

2560 Bit Static Read Only Memory

FEATURES

- 512×5 Organization—ideal for many general purpose applications.
- Single +5 Volt Supply.
- TTL Compatible—all inputs and outputs.
- Static Operation—no clocks required.
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs—under the control of an 'Output Inhibit' input to simplify memory expansion.
- Totally Automated Custom Programming.
- Zener Protected Inputs
- Glass Passivation Protection

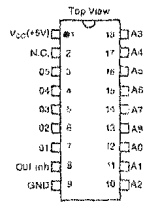
DESCRIPTION

The General Instrument RO-3-2560 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for many general purpose memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2560 can store a full 512 words of 5 bits each.

The RO-3-2560 is one of a family of 512 word Read-Only Memories offered by General Instrument; two others are the RO-3-4096, with a 512×8 memory organization, and the RO-3-5120, with a 512×10 memory organization.

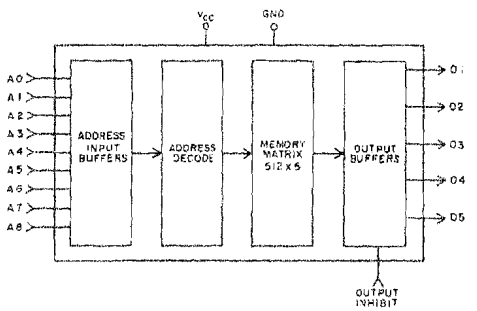
PIN CONFIGURATION

18 LEAD DUAL IN LINE



A separate publication "RO-3-2560 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2560 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND)	−0.3V to −8.0V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

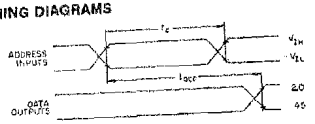
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF

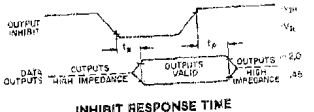
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs					V	
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65		
Leakage	I_{LI}	—	—	10	μA	
Data Outputs					V	I_{OH} = 100μA
Logic "1"	V_{OH}	2.2	—	—	V	I_{OL} = 1.6mA
Logic "0"	V_{OL}	—	—	0.45	μA	
Leakage	I_{LO}	—	—	10		
Power					mA	Outputs Open
I_{CC}	—	—	25	33		
AC CHARACTERISTICS						
Inputs					ns	
Cycle Time	t_C	400	—	—	pF	f = 1MHz
Capacitance	C_I	—	5	8		
Data Outputs					ns	
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_D	—	150	200	pF	f = 1MHz
Capacitance	C_O	—	8	10		

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

13

4096 Bit Static Read Only Memory

FEATURES

- 512×8 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns. Maximum Access Time
- 150 mW Typical Power
- Tri-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

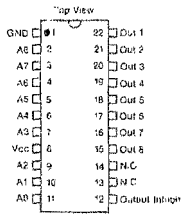
DESCRIPTION

The General Instrument RO-3-4096 is a 4096 bit static Read-Only-Memory. It is organized as 512 eight bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-4096 is constructed on a single monolithic chip utilizing low-voltage N-channel Ion Implant technology.

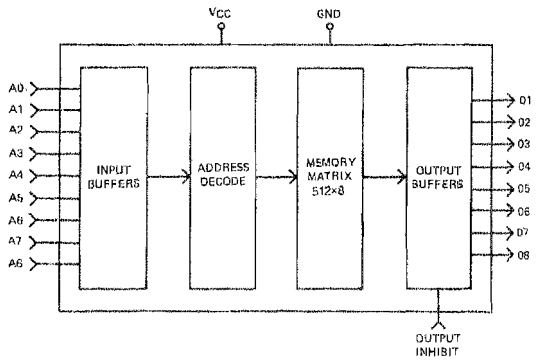
A separate publication, 'RO-3-4096 Custom Coding Information,' available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-4096 memory

PIN CONFIGURATION

22 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND)	−0.3V to +8.0V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A).	0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below

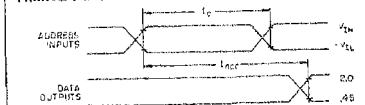
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load. C_L total = 50 pF

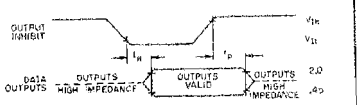
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH}=100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL}=1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power						
I_{CC}	—	—	30	45	mA	
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_L	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25° C and nominal voltages.

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC "0")



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

5120 Bit Static Read Only Memory

FEATURES

- 512x10 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- 500ns Maximum Access Time
- 150mW Typical Power
- Three-State Outputs—under control of 'Output Inhibit' signal
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

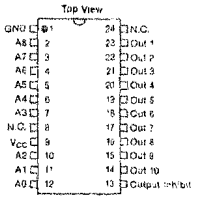
DESCRIPTION

The General Instrument RO-3-5120 is a 5120 bit static Read-Only-Memory. It is organized as 512 ten bit words and requires 9 bits of addressing. An 'Output Inhibit' function is provided to simplify the connection of several ROMs to a common bus. The RO-3-5120 is constructed on a single monolithic chip utilizing low-voltage N-channel ion implant technology.

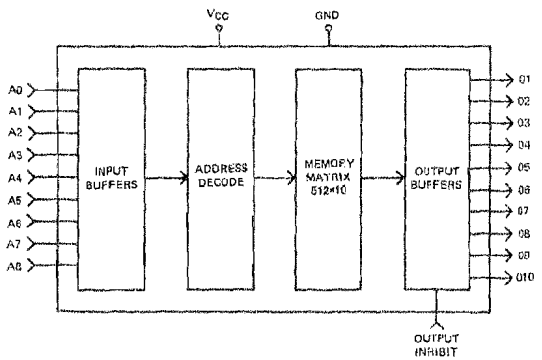
A separate publication, "RO-3-5120 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-5120 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND)	−0.3V to +8.0V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

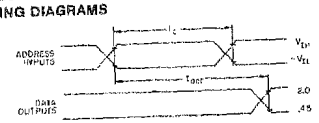
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL Load, $C_{L\ TOTAL}$ = 50pF.

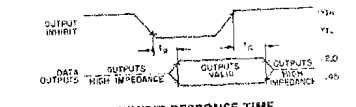
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	30	45	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	500	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	500	ns	
Inhibit Response Time	t_R	—	—	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—OUTPUT INHIBIT AT LOGIC '0')



INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

13

8192 Bit Read Only Memory

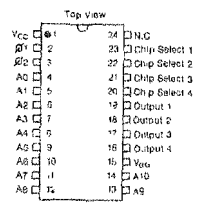
FEATURES

- 2048×4 Organization
- 1.2μs Typical Access Time
- TTL/DTL Compatibility—Inputs and clocks TTL/DTL compatible without external interfacing components.
- Programmable Chip Select—Simplifies design of large memory systems.
- Totally Automated Mask Generation—"RO-5-8192/Custom Coding Information", describing punched card and truth table data specification, is available from GI Sales Offices
- Zener Protected Inputs
- Glass Passivation Protection

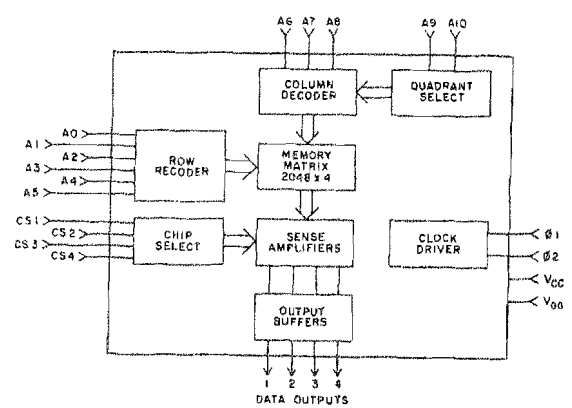
DESCRIPTION

The General Instrument RO-5-8192 is an 8192-bit dynamic Read Only Memory. It is organized as 2048 four bit words and requires 11 bits of addressing. Additional features such as programmable chip select are provided for greater system flexibility. The RO-5-8192 is constructed on a single monolithic chip utilizing MTNS P-channel enhancement mode transistors. The RO-5-8192 is available pre-programmed as a 4 bit random number generator.

PIN CONFIGURATION
24 LEAD DUAL IN LINE



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG}, clock and input voltages (with respect to V_{CC})	+0.3V to −20V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
V_{GG} = −12 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: R_L = 6.8K to V_{CC}, C_L TOTAL = 100pf.

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
Logic "1"	$V_{\phi H}$	V_{CC}−1.5	—	—	V	
Logic "0"	$V_{\phi L}$	—	—	+0.8	V	
Leakage	$I_{L\phi}$	—	—	1.0	μA	V_{IN} = V_{GG}−9V, T_A = +25°C
Address, Chip Select Inputs						
Logic "1"	V_{IH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{IL}	—	—	+0.8	V	
Leakage	I_{LI}	—	—	1.0	μA	V_{IN} = V_{GG}−9V T_A = +25°C
Quadrant Enable Inputs[2]						
Logic "1"	V_{QH}	V_{CC}−1.5	—	—	V	
Logic "0"	V_{QL}	—	—	+0.8	V	
Data Outputs						
Logic "1"	V_{OH}	V_{CC}−1.5	—	—	V	ONE TTL LOAD
Logic "0"	V_{OL}	—	—	V_{CC}−4.5	V	ONE TTL LOAD
Power						
I_{GG}	—	—	275	400	mW	
AC CHARACTERISTICS						
Clock Inputs						
Cycle Time	$t_{\phi c}$	2	—	100	μs	
ϕ1 Pulse Width	$t_{\phi 1pw}$	800	—	—	ns	$t_{\phi 1pw}$+$t_{\phi 2pd}$≥400ns
ϕ_1 Pulse Separation	$t_{\phi 1ps}$	1200	—	—	ns	
ϕ_2 Lead Time	$t_{\phi 2ld}$	400	—	—	nS	
ϕ_2 Lag Time	$t_{\phi 2lg}$	400	—	—	nS	
Rise and Fall Times	t_R,t_F	—	—	50	nS	
Capacitance	C_ϕ	—	8	10	pF	1MHz, T_A = +25°C
Inputs						
Set Up Time	t_{IS}	200	—	—	nS	
Hold Time	t_{IH}	200	—	—	nS	
Capacitance	C_I	—	5	7.5	pF	1MHz, T_A = +25°C
Data Outputs						
Propagation Delay	t_{PD}	—	0.6	1	μS	
Access Time	t_{ACC}	—	1.2	1.6	μS	(See Note)
Capacitance	C_O	—	3	5	pF	1MHz, T_A = +25°C

**Typical values are at +25°C and nominal voltages.

NOTE
Access Time is defined as t_{DS} (min.) + $t_{\phi 2lg}$ (min.) + t_{PD} (max.)

13

Logic "1" = +5V DC or the more positive voltage
Logic "0" = 0V DC or the more negative voltage

CHIP SELECT

The RO-5-8192 is provided with four programmable bits of chip select. Constructing large memory systems with more than one 8K ROM simply requires wire-working the ROM outputs and assigning different chip select codes to each ROM chip (when a chip is *not* selected, its outputs are at a logic "0"—the output device is off). In addition, cascading ROMs with the same chip select code provides additional bits per word.

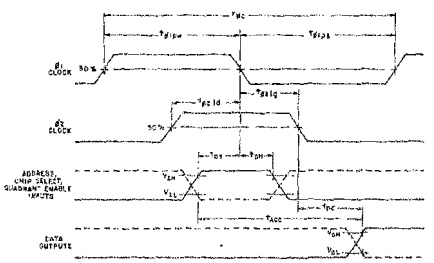
The four chip select bits are permanently programmed into the ROM at the same time as the custom data pattern. 31 different chip select codes are possible—16 unique codes and 15 additional with "don't care" variations (In the following x = 0 or 1):

CS1	CS2	CS3	CS4		
X	X	X	X	—	16 codes
DC	X	X	X	—	8 codes
DC	DC	X	X	—	4 codes
DC	DC	DC	X	—	2 codes
DC	DC	DC	DC	—	1 code

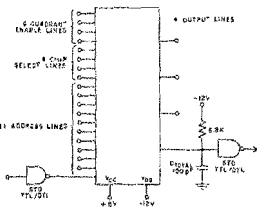
CUSTOM BIT PATTERNS

General Instrument makes use of proven computer techniques to provide fast and accurate generation of custom bit patterns. All necessary material, including the data pattern mask, test data and check lists (for customer verification), as computer-generated and cross-checked. For the full details on data specification, request the booklet "RO-5-8192/Custom Coding Information" from any GI Sales Office.

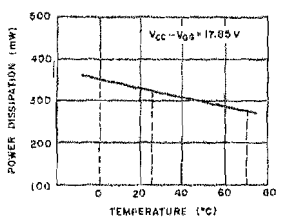
TIMING DIAGRAM



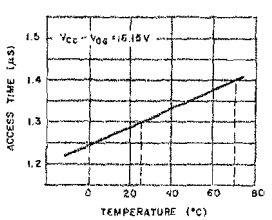
INTERFACE CIRCUIT—TTL/DTL



TYPICAL CHARACTERISTIC CURVES



POWER DISSIPATION vs. TEMPERATURE



ACCESS TIME vs. TEMPERATURE

16384 Bit Static Read Only Memories

FEATURES

- 2048×8 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 450ns Maximum Access Time RO-3-8316B/9316B
- 850ns Maximum Access Time RO-3-8316A/9316A
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The General Instrument RO-3-8316A/8316B and RO-3-9316A/9316B are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel ion-implant process to enable operation from a single +5 Volt power supply, the RO-3-8316A/8316B and RO-3-9316A/8316B offer the best combination of high performance large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

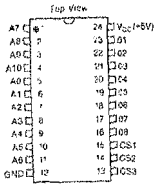
The RO-3-8316A/8316B are direct replacements in pin connection and operation for the Intel 8316A and 2316A

The RO-3-9316A/9316B pin configuration is identical to that of the Intel 2708 8K EPROM

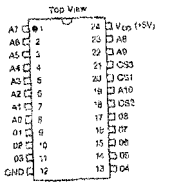
A separate publication, "RO-3-8316/9316 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming

PIN CONFIGURATION

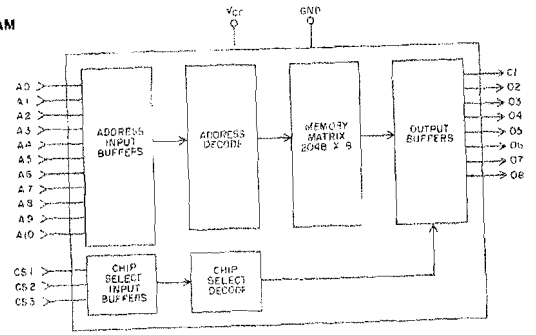
24 LEAD DUAL IN LINE
RO-3-8316A/8316B



RO-3-9316A/9316B



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND)	−0.3V to +8.0V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied—operating ranges are specified below

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L(MAX)}$ = 100pF.

RO-3-8316A/9316A and RO-3-8316B/9316B

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select, Latch Inputs						
Logic "1"	V_{IH}	2.0	—	—	V	
Logic "0"	V_{IL}	—	—	0.8	V	
Leakage	I_{LI}	—	—	10	µA	
Data Outputs						
Logic "1"	V_{OH}	2.4	—	—	V	I_{OH} = 100µA
Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	µA	
Power Supply Current						
I_{CC}	—	—	50	85	mA	Outputs open (RO-3-8316A/9316A)
	—	—	65	95	mA	Outputs open (RO-3-8316B/9316B)

RO-3-8316A/9316A

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	800	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	600	850	ns	
Chip Select Response Time	t_R	—	200	300	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

RO-3-8316B/9316B

AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f=1MHz
Data Outputs						
Access Time	t_{ACC}	—	350	450	ns	
Chip Select Response Time	t_R	—	100	200	ns	
Capacitance	C_O	—	8	10	pF	f=1MHz

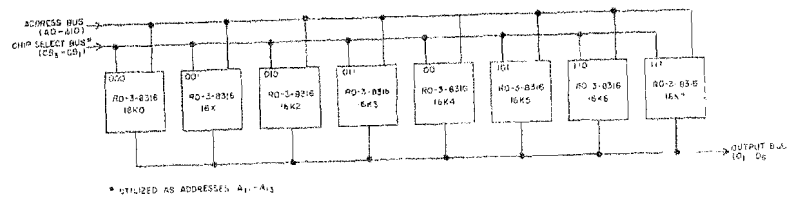
**Typical values are at +25° C and nominal voltages

TYPICAL SYSTEM APPLICATION

A complete system of 16K words of ROM (8 bits/word) is easily obtained without any external address decoding by making use of programmable chip select features and by wiring the outputs of eight different RO-3-8316's as shown in the figure below

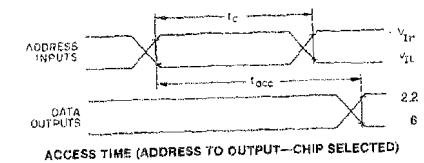
CHIP SELECT TABLE

CS 3	CS 2	CS 1	DEVICE SELECTED
0	0	0	16K0
0	0	1	16K1
0	1	0	16K2
0	1	1	16K3
1	0	0	16K4
1	0	1	16K5
1	1	0	16K6
1	1	1	16K7

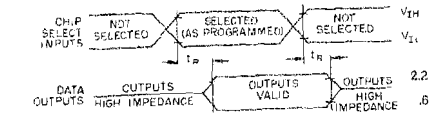


* UTILIZED AS ADDRESSES A_{11} - A_{13}

TIMING DIAGRAMS



ACCESS TIME (ADDRESS TO OUTPUT—CHIP SELECTED)



CHIP SELECT RESPONSE TIME (ADDRESS INPUTS STABLE)

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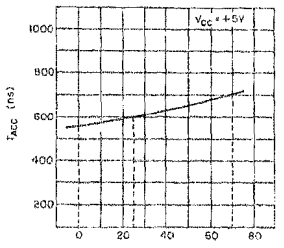
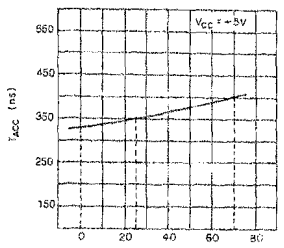
TYPICAL CHARACTERISTIC CURVES

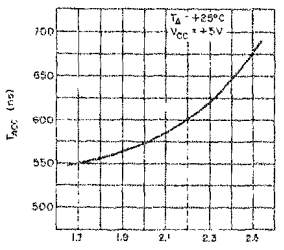


RO-3-8316A/9316A

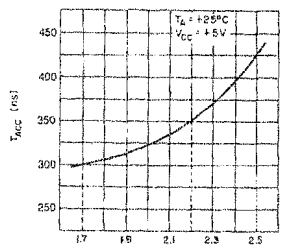


RO-3-8316B/9316B

Fig.1 ACCESS TIME VS. TEMPERATURE

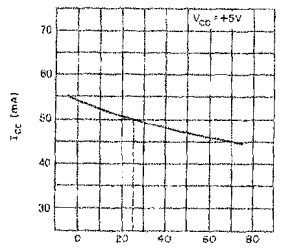


RO-3-8316A/9316A

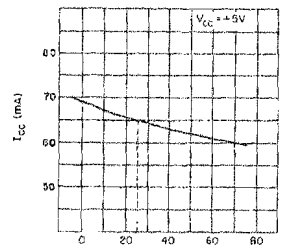


RO-3-8316B/9316B

Fig.2 ACCESS TIME VS. OUTPUT VOLTAGE



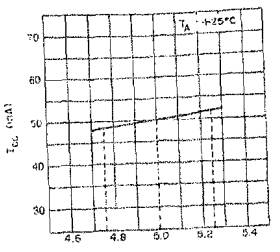
RO-3-8316A/9316A



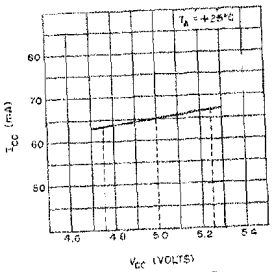
RO-3-8316B/9316B

Fig.3 POWER SUPPLY CURRENT VS. TEMPERATURE

TYPICAL CHARACTERISTIC CURVES

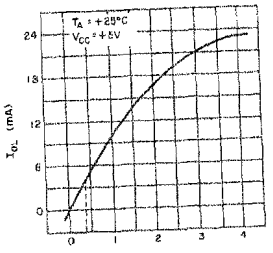


RO-3-8316A/9316A



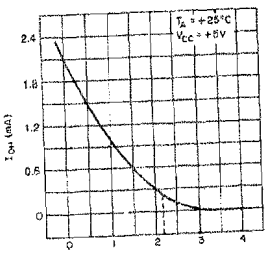
RO-3-8316B/9316B

Fig.4 POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.5 OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



RO-3-8316A/8316B, RO-3-9316A/9316B

Fig.6 OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE

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16384 Bit Static Read Only Memories

FEATURES

- 2048x8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required.
- 350ns Maximum Access Time
- Three-Stage Outputs—under the control of three mask-programmable Chip Select inputs to simplify memory expansion
- Totally Automated Custom Programming.
- Zener Protected Inputs
- Glass Passivation Protection

DESCRIPTION

The General Instrument RO-3-8316C/9316C are 16,384 static Read Only Memories organized as 2048 eight bit words and are ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel ion-implant process to enable operation from a single +5 Volt power supply, the RO-3-8316C/9316C offer the best combination of high performance, large bit storage, and simple interfacing of any MOS Read-Only Memories available today.

The RO-3-8316C is a direct replacement in pin connection and operation for the Intel 8316A and 2316A.

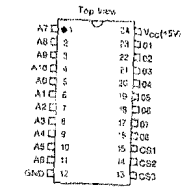
The RO-3-9316C pin configuration is identical to that of the Intel 2708 8K EPROM.

A separate publication, "RO-3-8316/9316 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming.

PIN CONFIGURATION

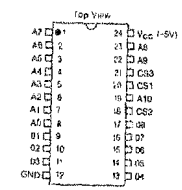
24 LEAD DUAL IN LINE

RO-3-8316C

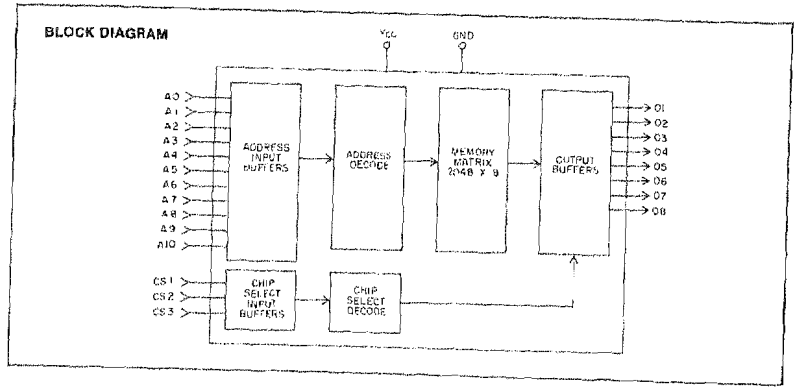


24 LEAD DUAL IN LINE

RO-3-9316C



BLOCK DIAGRAM



16384 Bit Static Read Only Memory

FEATURES

- 4096x4 Organization
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks required
- Address/Chip Select Latch Input—may be used to gate in new Address or Chip Select Inputs
- 1 μs Maximum Access Time
- 250 mW Typical Power
- Three-State Outputs—under control of 3 programmable Chip Select inputs
- Totally Automated Custom Programming
- Zener Protected Inputs
- Glass Passivation Protection

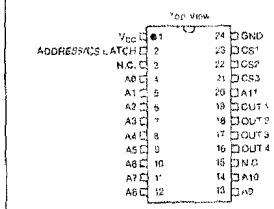
DESCRIPTION

The General Instrument RO-3-16384 is a 16,384 bit static Read-Only-Memory. It is organized as 4096 four bit words and requires 12 bits of addressing. Three programmable Chip Select inputs are provided to simplify the connection of several ROMs to a common bus. The RO-3-16384 is constructed on a single monolithic chip utilizing low-voltage N-channel ion implant technology.

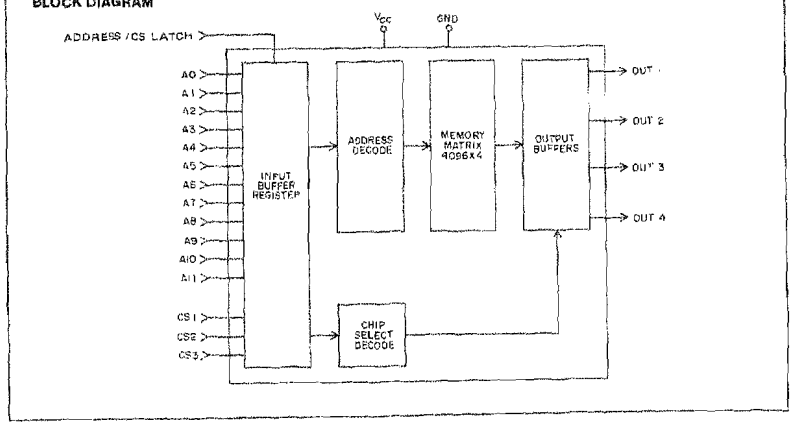
A separate publication, "RO-3-16384 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table data format for custom programming of the RO-3-16384 memory.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND)	−0.3V to +6.0V
Storage Temperature	−65°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

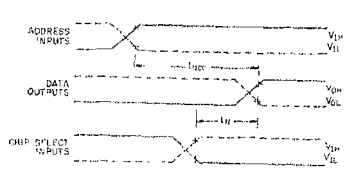
Standard Conditions: (unless otherwise noted)

V_{CC} = +5 volts ± 5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, C_L total = 50 pF

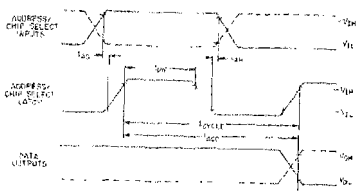
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Chip Select, Latch Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	µA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100µA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	µA	
Power Supply Current						
	I_{CC}	—	60	65	mA	Outputs open
AC CHARACTERISTICS						
Address, Chip Select Inputs						
Cycle Time	t_c	1.0	—	—	µs	
Set-up Time	t_{AS}	0	—	—	ns	
Hold Time	t_{AH}	200	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Latch Input						
Pulse Width	t_{PW}	200	—	—	ns	
Data Outputs						
Access Time	t_{ACC}	—	0.7	1.0	µs	
Chip Select Response Time	t_R	—	200	300	ns	Latch at +5V
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages

TIMING DIAGRAMS

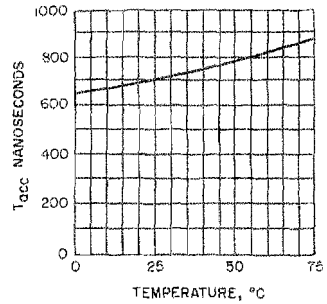


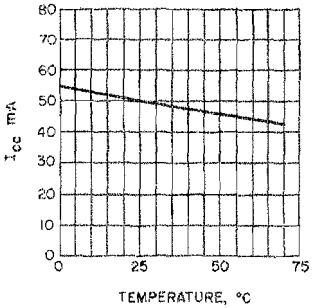
WITH LATCH INPUT HELD AT +5V

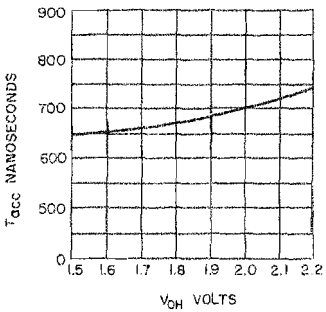


WITH LATCH INPUT UTILIZED

TYPICAL CHARACTERISTIC CURVES







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RO-3-20480

PRELIMINARY INFORMATION

20480 Bit Static Read Only Memory

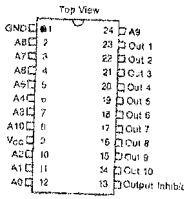
FEATURES

- 2048×10 Organization—ideal for microprocessor memory systems
- Single +5 Volt Supply
- TTL/DTL Compatible
- Static Operation—no clocks.
- 500ns Maximum Access Time
- 250mW Typical Power
- Three-State Outputs—under control of Output Inhibit

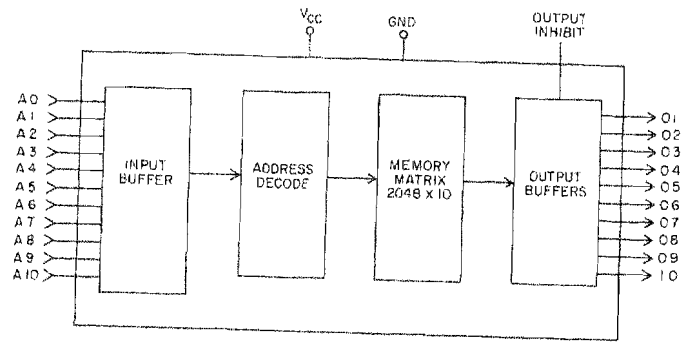
DESCRIPTION

The General Instrument RO-3-20480 is a 20,480 bit static Read Only Memory ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-20480 offers high performance, large bit storage, and simple interfacing.

PIN CONFIGURATION
24 LEAD DUAL IN LINE



BLOCK DIAGRAM



RO-3-9332A

PRELIMINARY INFORMATION

32768 Bit Static Read Only Memory

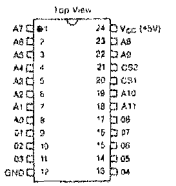
FEATURES

- 4096×8 Organization—ideal for microprocessor memory systems.
- Single +5 Volt Supply
- TTL Compatible—all inputs and outputs
- Static Operation—no clocks required
- 650ns Maximum Access Time
- Three-State Outputs—under the control of two mask-programmable Chip Select inputs to simplify memory expansion.
- Totally Automated Custom Programming
- Zener Protected Inputs.
- Glass Passivation Protection

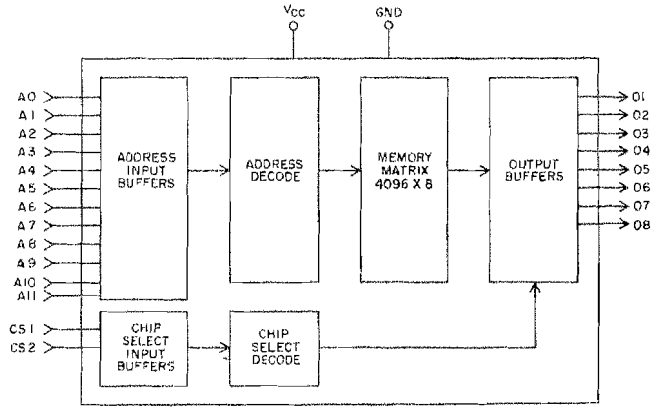
DESCRIPTION

The General Instrument RO-3-9332A is a 32,768 bit static Read Only Memory organized as 4096 eight bit words and is ideally suited for microprocessor memory applications. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-9332A offers the best combination of high performance, large bit storage, and simple interfacing.

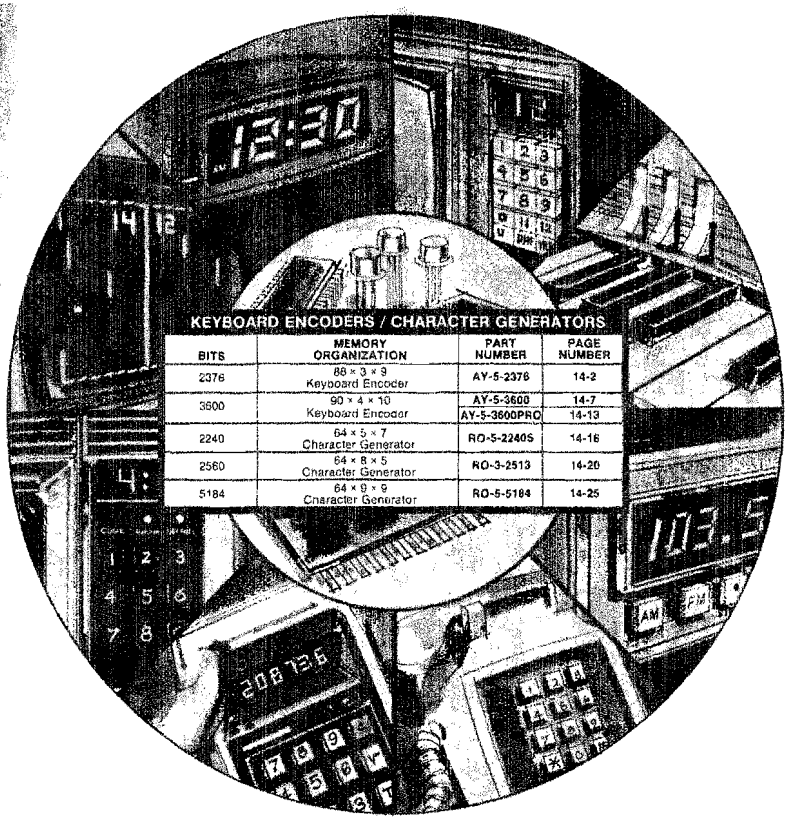
PIN CONFIGURATION
24 LEAD DUAL IN LINE



BLOCK DIAGRAM



13



KEYBOARD ENCODERS / CHARACTER GENERATORS

BITS	MEMORY ORGANIZATION	PART NUMBER	PAGE NUMBER
2376	88 × 3 × 9 Keyboard Encoder	AY-5-2376	14-2
3600	90 × 4 × 10 Keyboard Encoder	AY-5-3600	14-7
		AY-5-3600PRO	14-13
2240	64 × 5 × 7 Character Generator	RO-5-2240S	14-16
2560	64 × 8 × 5 Character Generator	RO-3-2513	14-20
5184	64 × 9 × 9 Character Generator	RO-5-5184	14-25

KEYBOARD ENCODERS/ CHARACTER GENERATORS

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MICRO ELECTRONICS

Keyboard Encoder

FEATURES

- One integrated circuit required for complete keyboard assembly.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- External control provided for output polarity selection.
- External control provided for selection of odd or even parity.
- Two key roll-over operation.
- N-key lockout.
- Programmable coding with a single mask change.
- Self-contained oscillator circuit.
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

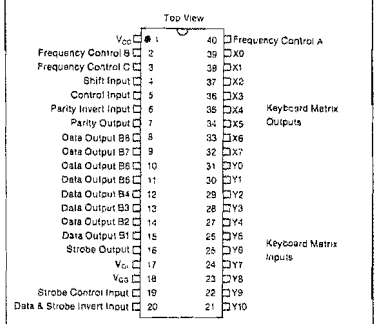
DESCRIPTION

The General Instrument AY-5-2376 is a 2376 Bit Read Only Memory with all the logic necessary to encode single pole single throw keyboard closures into a usable 9-bit code. Data and strobe outputs are directly compatible with TTL/DTL or MOS logic arrays without the use of any special interface components.

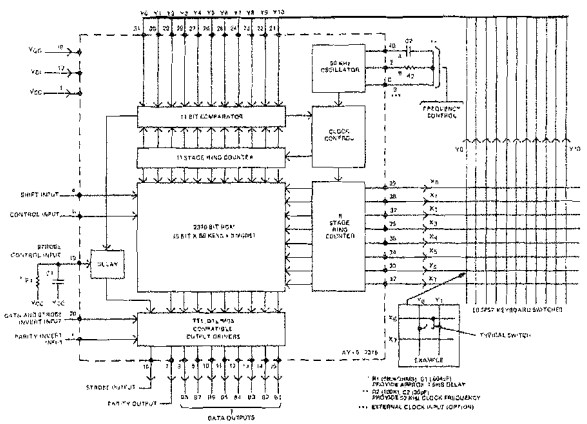
The AY-5-2376 is fabricated with MTNS technology and contains 2942 P-channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION

40 LEAD DUAL IN LINE



BLOCK DIAGRAM



OPERATION

The AY-5-2376 contains (see Block Diagram), a 2376-bit ROM, 8-stage and 11-stage ring counters, an 11-bit comparator, an oscillator circuit, an externally controllable delay network for eliminating the effect of contact bounce, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 264 by 9 bit memory arranged into three 88-word by 9-bit groups. The appropriate levels on the Shift and Control inputs selects one of the three 88-word groups; the 88-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control inputs with the two ring counters.

The external outputs of the 8-stage ring counter and the external inputs to the 11-bit comparator are wired to the keyboard to form an X-Y matrix with the 88-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM; the absence of a Strobe Output indicates that the Data Outputs are 'not valid' at this time.

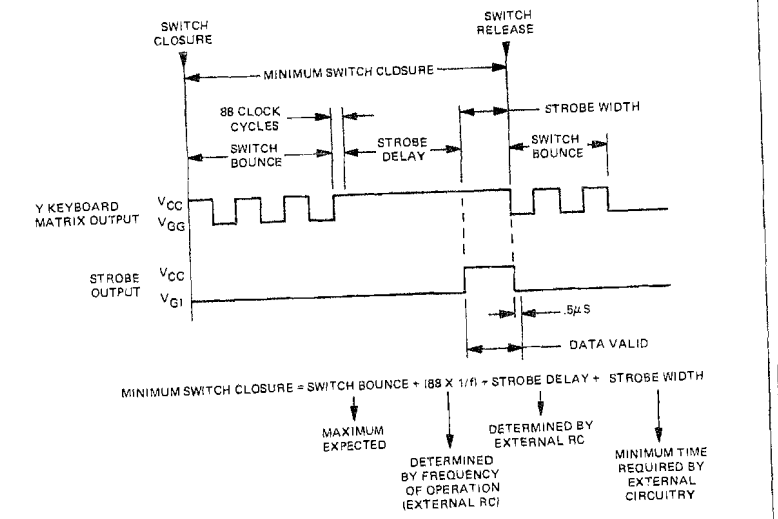
When a key is depressed, a single path is completed between one output of the 8-stage ring counter (X0 thru X7) and one input of the 11-bit comparator (Y0-Y10). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 11-stage ring counter. When this occurs, the comparator generates a signal to the clock control and to the Strobe Output (via the delay network). The clock control stops the clocks to the ring counters and the Data Outputs (B1-B9) stabilize with the selected 9-bit code, indicated by a 'valid' signal on the Strobe Output. The Data Outputs remain stable until the key is released.

As an added feature two inputs are provided for external polarity control of the Data Outputs. Parity Invert (pin 6) provides polarity control of the Parity Output (pin 7) while the Data and Strobe Invert Input (pin 20) provides for polarity control of Data Outputs B1 thru B8 (pins 8 thru 15) and the Strobe Output (pin 16).

SPECIAL PATTERNS

Since the selected coding of each key is defined during the manufacture of the chip, the coding can be changed to fit any particular application of the keyboard. Up to 264 codes of up to 8 bits (plus one parity bit) can be programmed into the AY-5-2376 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code is available as a standard pattern.

TIMING DIAGRAM



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ELECTRICAL CHARACTERISTICS

Maximum Ratings

V_{GI} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

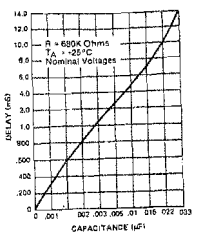
V_{CC} = +5 Volts ± 0.5 Volts, V_{GG} = −12 Volts ± 1.0 Volts, V_{GI} = GND. | (V_{CC} = Substrate Voltage) Operating Temperature (T_A) = 0°C to +70°C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote** for typical R - C values
Data Input (Shift, Control, Parity invert, data & strobe invert).						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
			—			
Shift & Control Input Current	$I_{INS,C}$	15	36	80	µA	V_I=+5V
		8	16	30	µA	V_I= 0V
Data, Parity Invert Input Current	$I_{IND,P}$	—	.01	1	µA	V_I=−5V to +5V
X Output (X_0-X_7)						
Logic "1" Output Current	I_{X1}	—	0	—	µA	V_{OUT} = V_{CC}
		80	150	400	µA	V_{OUT} = V_{CC} −1.3V
		140	300	800	µA	V_{OUT} = V_{CC} −2.0V
		250	700	1500	µA	V_{OUT} = V_{CC} −5V
		500	1500	3000	µA	V_{OUT} = V_{CC} — 10V
Logic "0" Output Current	I_{X0}	15	30	80	µA	V_{OUT} = V_{CC}
		13	27	65	µA	V_{OUT} = V_{CC} −1.3V
		12	25	60	µA	V_{OUT} = V_{CC} −2.0V
		5	10	40	µA	V_{OUT} = V_{CC} −5V
		—	1	20	µA	V_{OUT} = V_{CC} −10V
Y Input (Y_0-Y_{10})						
Trip Level	V_Y	V_{CC} −5	V_{CC} −3	V_{CC}−2	V	Y Input Going Positive
Hysteresis	ΔV_Y	.5	.9	1.4	V	Note 1
						Note 2
Selected Y Input Current	I_{YS}	30	60	160	µA	V_{IN} = V_{CC}
		25	54	130	µA	V_{IN} = V_{CC} −1.3V
		24	50	120	µA	V_{IN} = V_{CC} −2.0V
		10	20	80	µA	V_{IN} = V_{CC} −5V
		—	2	20	µA	V_{IN} = V_{CC} −10V
Unselected Y Input Current	I_{YU}	15	30	80	µA	V_{IN} = V_{CC}
		13	27	65	µA	V_{IN} = V_{CC} −1.3V
		12	25	60	µA	V_{IN} = V_{CC} −2.0V
		5	10	40	µA	V_{IN} = V_{CC} −10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1X10⁷	—	—	Ω	
Strobe Delay						
Trip Level (Pin 19)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	.5	.9	1.4	V	See Note 1
Quiescent Voltage (Pin 19)		−3	−5	−8	V	With 680KΩ to V_{SS}
Data Output (B_1-B_8)						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6ma
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH}=100µa
Power						
I_{CC}	—	—	5	10	mA	V_{CC} = +5V
I_{GG}	—	—	5	10	mA	V_{GG} = −12V

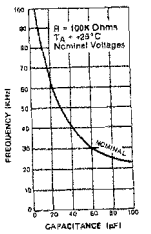
**Typical values at +25° C and nominal voltages.

NOTE 1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Guaranteed number of X & Y loads which may be applied to an X output = eleven.

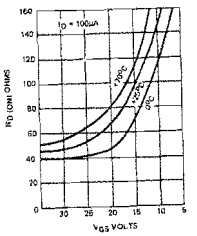
TYPICAL CHARACTERISTIC CURVES



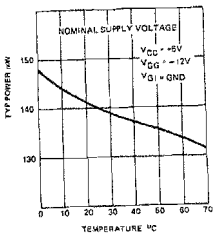
STROBE DELAY VS. C1



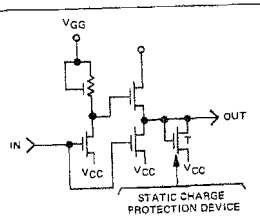
OSCILLATOR FREQUENCY VS. C2



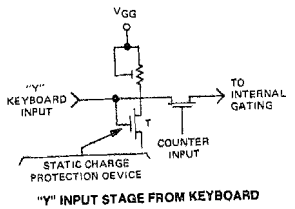
TYPICAL OUTPUT ON RESISTANCE (R_{DON}) VS. GATE BIAS VOLTAGE (V_{GS})



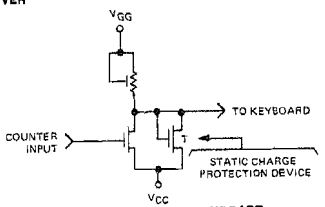
TYPICAL POWER CONSUMPTION (mW) VS. TEMP (C°)



OUTPUT DRIVER



"Y" INPUT STAGE FROM KEYBOARD



"X" OUTPUT STAGE TO KEYBOARD

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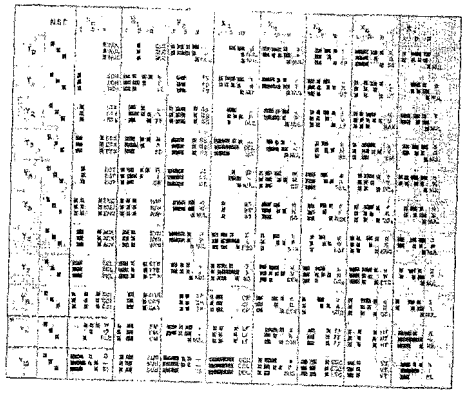
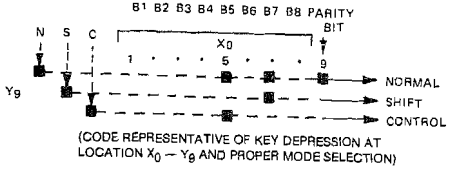
STANDARD CODE ASSIGNMENT CHART



Illustrated using a Logic "0" on the Data and Strobe Invert Input (Pin 20) and the Parity Invert Input (Pin 6).

NOTE 1: This code is an 8 bit ASCII code (B1-B6). Output B8 is included as an odd parity bit operating on outputs B1-B7

*EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION $X_0 - Y_8$ AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
■ = OUTPUT LOGIC "1": (SEE DATA B1 – B8)
LOGIC "1" = +5V
LOGIC "0" = GND

TRUTH TABLES

DATA (B1-B8) INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	CODE ASSIGNMENT CHART	DATA OUTPUTS (B1-B8)
1	1	0
0	1	1
1	0	1
0	0	0

PARITY INVERT TRUTH TABLE

PARITY INVERT INPUT (PIN 6)	CODE ASSIGNMENT CHART	PARITY OUTPUT (PIN 7)
1	1	0
0	1	1
1	0	1
0	0	0

STROBE INVERT TRUTH TABLE

DATA AND STROBE INVERT INPUT (PIN 20)	INTERNAL STROBE	STROBE OUTPUT (PIN 16)
1	1	0
0	0	0
1	0	1
0	1	1

MODE SELECTION

$\overline{S}$	$\overline{C}$	=
$\overline{S}$	C	= S
S	$\overline{C}$	= C
S	C	= C

Keyboard Encoder

FEATURES

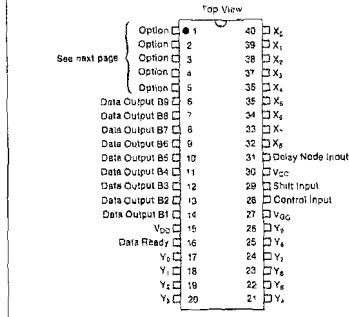
- One integrated circuit required for complete keyboard assembly.
- N key rollover or lock out operation
- Quad mode operation
- Lock out/rollover selection under external control (option)
- Self-contained or slave oscillator circuit.
- 10 output data bits available.
- Outputs directly compatible with TTL/DTL or MOS logic arrays.
- Output data buffer register included
- Output enable provided (option).
- External data complement control provided (option).
- Pulse or level data ready output signal provided (option).
- "Any Key Down" output provided (option).
- Externally controlled delay network provided to eliminate the effect of contact bounce.
- Programmable coding with a single mask change.
- Static charge protection on all input and output terminals.
- Entire circuit protected by a layer of glass passivation.

DESCRIPTION

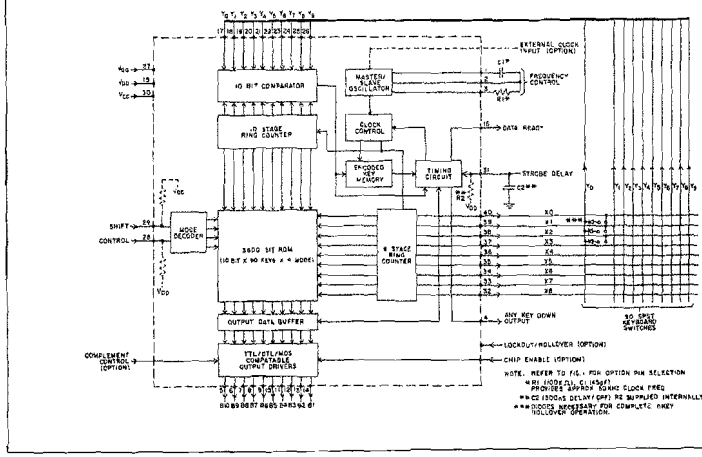
The General Instrument AY-5-3600 is a Keyboard Encoder containing a 3600 bit Read Only Memory and all the logic necessary to encode single pole single throw keyboard closures into a usable 10 bit code. Data, Any Key Down and Data Ready outputs are directly compatible with TTL/DTL or MOS logic arrays without the need for any special interface components.

The AY-5-3600 is fabricated with MTNS technology and contains 5000 P channel enhancement mode transistors on a single monolithic chip.

PIN CONFIGURATION
40 LEAD DUAL IN LINE



BLOCK DIAGRAM



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CUSTOM CODING INFORMATION

The custom coding information for General Instrument's AY-5-3600 Keyboard Encoder ROM should be transmitted to General Instrument in the form of 80 column punched cards. Each ROM pattern requires 92 cards (1 title card, 1 circuit option card and 90 ROM pattern cards). (See Note 1)

If it is not possible to supply punched cards, then the Truth Table should be completed (See Note 1). However, there would be a substantial savings in both the coding charge and turn-around time if punched cards were used. Upon receipt of the punched cards or the Truth Table, General Instrument will prepare a computer-generated Truth Table which will be returned to the user for verification.

NOTE 1: Card and Truth Table format available upon request.

PIN OPTIONS

Pins 6-40 of the AY-5-3600 are permanently assigned. The functions assigned to pins 1-5 depend on which functional options are selected from the following:

External Clock
—requires one package pin to input an external clock source.
Internal Oscillator
—requires three package pins interconnected with an external RC network to develop the clock required.
Lockout/Rollover (LO/RO)
—requires one package pin to externally select N-Key Lockout or N-Key Rollover. LO = +5V, RO = GND.
Complement Control (CC)
—requires one package pin to externally control the logic state of the data bits (B1-B10) and, if required, the Data Ready output.
Chip Enable (CE)
—requires one package in to control the data bits (B1-B10) and, if required, the Data Ready and Any Key Output.
Any Key Output (AKO)
—requires one package pin to indicate a key depression.
Output Data Bit 10 (B10)
—requires one package pin when ten data bits are required to encode each key.

Select the pin options desired:
External Clock + 4 of the following functions
OR
Internal Oscillator + 2 of the following functions
LO/RO, CC, CE, AKO, BIO

The following chart lists the pin assignments according to the functions selected above:

PIN 1	PIN 2	PIN 3	PIN 4	PIN 5
External Clock	LO/RO	CC	CE	AKO
External Clock	LO/RO	CC	CE	BIO
External Clock	LO/RO	CC	AKO	BIO
External Clock	LO/RO	CE	AKO	BIO
External Clock	CC	CE	AKO	BIO
Internal Oscillator			LO/RO	CC
			LO/RO	CE
			LO/RO	AKO
			LO/RO	BIO
			CC	CE
			CC	AKO
			CC	BIO
			CE	AKO
			CE	BIO
			AKO	BIO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD} and V_{GG} (with respect to V_{CC}) . . . . . −20V to +0.3V
Logic input voltages (with respect to V_{CC}) . . . . −20V to +0.3V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature Range. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.5 Volts
V_{GG} = −12 Volts ±1.0 Volts, V_{DD} = GND
(V_{CC} = Substrate Voltage)
Operating Temperature (T_A) = 0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
Clock Frequency	f	10	50	100	KHz	See Block diagram footnote* for typical R-C values
External Clock Width		7	—	—	μs	
Data & Clock Input (Shift, Control, Complement Control, Lockout/Rollover, Chip Enable & External Clock)						
Logic "0" Level	V_{I0}	V_{GG}	—	+0.8	V	
Logic "1" Level	V_{I1}	V_{CC}−1.5	—	V_{CC}+0.3	V	
Shift & Control Input Current	I_{MSC}	75	95	120	μA	V_I = +5V
X Output (X_0-X_9)						
Logic "1" Output Current	I_{X1}	40	170	400	μA	$V_{OUT} = V_{CC}$ (See Note 2)
		600	1300	2500	μA	$V_{OUT} = V_{CC}$−1.3V
		900	1600	3500	μA	$V_{OUT} = V_{CC}$−2.0V
		1500	3800	6000	μA	$V_{OUT} = V_{CC}$−5V
		3000	6000	10000	μA	$V_{OUT} = V_{CC}$−10V
Logic "0" Output Current	I_{X0}	8	15	50	μA	$V_{OUT} = V_{CC}$
		6	11	35	μA	$V_{OUT} = V_{CC}$−1.3V
		5	10	30	μA	$V_{OUT} = V_{CC}$−2.0V
		2	5	15	μA	$V_{OUT} = V_{CC}$−5V
		—	0.5	5	μA	$V_{OUT} = V_{CC}$−10V
Y Input (Y_0-Y_9)						
Trip Level	V_Y	V_{CC}−5	V_{CC}−3	V_{CC}−2	V	Y Input Going Positive (See Note 2)
Hysteresis	ΔV_Y	0.5	0.9	1.4	V	(See Note 1)
Selected Y Input Current	I_{YS}	18	36	100	μA	$V_{IN} = V_{CC}$
		14	28	90	μA	$V_{IN} = V_{CC}$−1.3V
		13	25	80	μA	$V_{IN} = V_{CC}$−2.0V
		6	12	60	μA	$V_{IN} = V_{CC}$−5V
		—	1	30	μA	$V_{IN} = V_{CC}$−10V
Unselected Y Input Current	I_{YU}	9	18	50	μA	$V_{IN} = V_{CC}$
		7	14	45	μA	$V_{IN} = V_{CC}$−1.3V
		6	13	40	μA	$V_{IN} = V_{CC}$−2.0V
		3	6	30	μA	$V_{IN} = V_{CC}$−5V
		—	0.5	15	μA	$V_{IN} = V_{CC}$−10V
Input Capacitance	C_{IN}	—	3	10	pF	at 0V (All Inputs)
X-Y Precharge Characteristics	ϕP	1500	3500	5000	μA	V = V_{CC}
		200	600	1500	μA	V = V_{CC}−5 (See Note 2)
Switch Characteristics						
Minimum Switch Closure	—	—	—	—	—	See Timing Diagram
Contact Closure Resistance	Z_{CC}	—	—	300	Ω	
	Z_{CO}	1 × 10⁷	—	—	Ω	
Strobe Delay						
Trip Level (Pin 31)	V_{SD}	V_{CC}−4	V_{CC}−3	V_{CC}−2	V	
Hysteresis	V_{SD}	0.5	0.9	1.4	V	(See Note 1)
Quiescent Voltage (Pin 31)		−3	−5	−9	V	With Internal Switched Resistor
Data Output (B1-B10), Any Key Down Output, Data Ready						
Logic "0"	—	—	—	0.4	V	I_{OL} = 1.6m A
Logic "1"	—	V_{CC}−1	—	—	V	I_{OH} = 1.0m A
	—	V_{CC}−2	—	—	V	I_{OH} = 2.2m A
Power						
I_{CC}	—	—	8	12	mA	V_{CC} = +5V
I_{GG}	—	—	8	12	mA	V_{GG} = −12V

**Typical values are at +25°C and nominal voltages.

NOTE
1. Hysteresis is defined as the amount of return required to unlatch an input.
2. Precharge of X outputs and Y inputs occurs during each scanned clock cycle.

The AY-5-3600 contains (see Block Diagram), a 3600 bit ROM, 9-stage and 10-stage ring counters, a 10 bit comparator, timing circuitry, a 90 bit memory to store the location of encoded keys for n key rollover operation, an externally controllable delay network for eliminating the effect of contact bounce, an output data buffer, and TTL/DTL/MOS compatible output drivers.

The ROM portion of the chip is a 360 by 10 bit memory arranged into four 90-word by 10-bit groups. The appropriate levels on the Shift and Control inputs selects one of the four 90-word groups; the 90-individual word locations are addressed by the two ring counters. Thus, the ROM address is formed by combining the Shift and Control inputs with the two ring counters.

The external outputs of the 9-stage ring counter and the external inputs to the 10-bit comparator are wired to the keyboard to form an X-Y matrix with the 90-keyboard switches as the crosspoints. In the standby condition, when no key is depressed, the two ring counters are clocked and sequentially address the ROM, thereby scanning the key switches for key closures.

When a key is depressed, a single path is completed between one output of the 9-stage ring counter (X0 thru X8) and one input of the 10-bit comparator (Y_0-Y_9). After a number of clock cycles, a condition will occur where a level on the selected path to the comparator matches a level on the corresponding comparator input from the 10-stage ring counter.

N KEY ROLLOVER

— When a match occurs, and the key has not been encoded, the switch bounce delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears, a one is stored in the encoded key memory and the scan aequence is resumed. If a match occurs at another key location, the sequence is repeated thus encoding the next key. If the match occurs for an already encoded key, the match is not recognized. The code of the last key encoded remains in the output data buffer.

N KEY LOCKOUT

— When a match occurs, the delay network is enabled. If the key is still depressed at the end of the selected delay time, the code for the depressed key is transferred to the output data buffer, the data ready signal appears and the remaining keys are locked out by halting the scan sequence. The scan sequence is resumed upon key release. The output data buffer stores the code of the last key encoded.

SPECIAL PATTERNS

— Since the selected coding of each key and all the options are defined during the manufacture of the chip, the coding and options can be changed to fit any particular application of the keyboard. Up to 360 codes of up to 10 bits can be programmed into the AY-5-3600 ROM covering most popular codes such as ASCII, EBCDIC, Selectric, etc., as well as many specialized codes. The ASCII code in conjunction with internal oscillator, 10 data outputs and any key down output, is available as a standard pattern (See Figure 2).

TIMING DIAGRAM

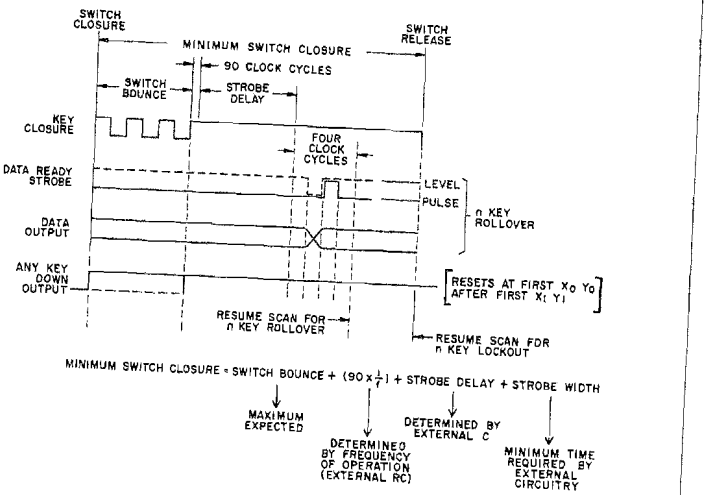
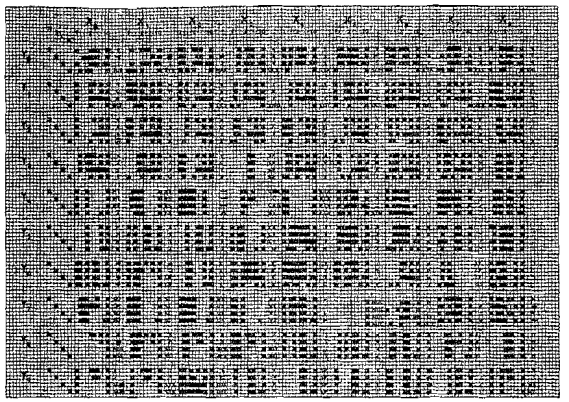


Fig.1

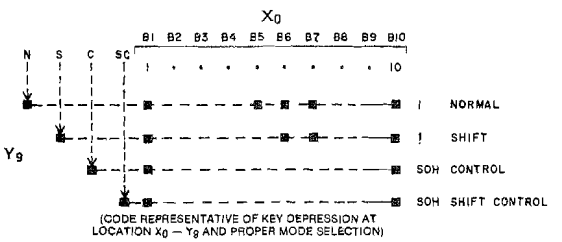
Fig.2 CONFIGURATION & CODE OF STANDARD ENCODER



OPTIONS PROVIDED WITH STANDARD ENCODER

- Device Marking: AY-5-3600
- Internal Oscillator on Pin Nos. 1, 2, 3.
- Any Key Output on Pin No. 4.
  Any Key Output True (Logic 1) During Key Depression.
- Output Data Bit B10 on Pin No. 5.
- N-Key Rollover Only.
- True Outputs Only.
- Pulse Data Ready Signal.
- Internal Resistor to V_{DD} on Shift/Control Pin.
- Plastic Package.

EXAMPLE



(CODE REPRESENTATIVE OF KEY DEPRESSION AT LOCATION X_0 — Y_9 AND PROPER MODE SELECTION)

N = NORMAL MODE
S = SHIFT MODE
C = CONTROL MODE
SC = SHIFT CONTROL
■ = OUTPUT LOGIC "1" (SEE DATA B1-B10)
LOGIC "1" = V_{CC}
LOGIC "0" = V_{DD}
TRUE OUTPUTS

MODE SELECTION			
$\bar{S}$	$\bar{C}$	=	N
S	$\bar{C}$	=	S
$\bar{S}$	C	=	C
S	C	=	SC

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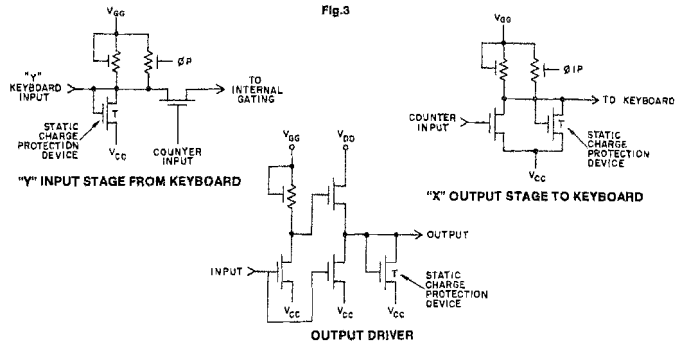
Fig.3



NOTE: Output driver capable of driving one TTL load with no external resistor.
Capable of driving two TTL loads using an external 6.8KΩ resistor to V_{GG}.

TYPICAL CHARACTERISTIC CURVES

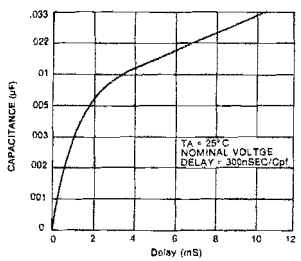


Fig.4 STROBE DELAY vs. C_1

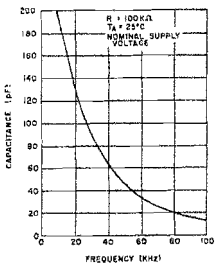


Fig.5 OSCILLATOR FREQUENCY vs. C_2

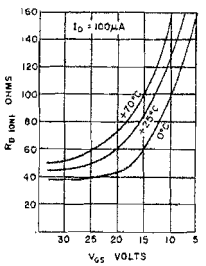


Fig.6 TYPICAL OUTPUT ON RESISTANCE (R_{DON}) vs. GATE BIAS VOLTAGE (V_{GS})

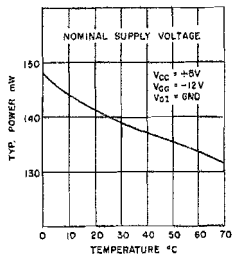
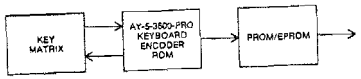


Fig.7 TYPICAL POWER CONSUMPTION (mW)

Keyboard Encoder and PROM/EPROM Application

The AY-5-3600-PRO is pre-programmed during manufacture to provide specific yet simple binary coded outputs thus allowing the purchase of off-the-shelf devices (distributors, etc.). To enhance the device flexibility, the binary outputs have been organized to provide direct interface with a PROM/EPROM.



The PROM (Programmable Read Only Memory) permits the programming of the required output code in the factory or the field within minutes, thus making it extremely suitable for small quantity, fast turnaround keyboard requirements. The EPROM (Erasable Programmable Read Only Memory) is ideally suited for prototyping, where patterns are quite variable, allowing the EPROM to be erased and reprogrammed repeatedly. Similar advantages are realized in the field where pattern changes are necessary in order to respond to redefined requirements or to subtle system peculiarities not previously encountered.

Technical Description

The AY-5-3600-PRO is a binary coded MOS-LSI device programmed to furnish 360 unique 9-bit codes (90 keys × 4 modes × 9 bits). Option selections include such popular functions as Internal Oscillator, Lockout/Rollover and an Any Key Down output. For further, more explicit device characteristics refer to the preceding pages. The internal oscillator is a self contained (on-chip) circuit option which eliminates the need for any external clock source. For applications necessitating an external clock source the internal oscillator input pins may be utilized to function in the slave mode of operation. Lockout or Rollover is selectable via an input pin, thus allowing the versatility required on various keyboard applications. The Any Key Down output performs the function of a gating signal by acknowledging both a key depression and release, making it a convanient signal for use in a repeat application.

For ease of translation, each key is assigned an X-Y coordinate and, in turn, each X-Y coordinate has been identified with a specific yet simple binary coded output. Two formats are described: the first for application with a 64 key 4 mode keyboard and the second for a 90 key 4 mode keyboard.

The 64 key 4 mode application as illustrated in Fig. 8 utilized keyboard encoder addresses X0 Y0 thru X6 Y3. A unique combination of one input (Y) and one output (X) is assigned to each key, for a total coverage of 64 keys. Binary coded outputs B2-B9 have been arranged to provide the necessary 8-bit address inputs to the PROM/EPROM, with B2 and B3 representing the variable mode identification and B4-B9 each specific key closure.

When a key is depressed a path is completed between one X line and one Y line thus addressing that specific X-Y ROM coordinate in the AY-5-3600-PRO. The 8-bit binary code for that X-Y location (ref. Truth Table page 14-15) is transferred into a one character 8-bit output latch (B2-B9) thus providing the appropriate 8-bit address to the 256×8 PROM/EPROM.

Expansion to a 90 key 4 mode operation (see Fig. 9) is identical to the 64 key 4 mode except: the 90 key 4 mode version utilizes the full complement of addresses X0 Y0 thru X8 Y9 (90 keys). The 8-bit binary code (B2-B9) previously produced to address the 256×8 PROM/EPROM is now expanded to a 9-bit binary code (B1-B9) for addressing to a 512×8 PROM/EPROM. With expansion to a 90 key 4 mode application outputs B1-B3 now serve as the variable mode identification.

The interface to a PROM/EPROM enables the custom programming of the required output date in the PROM/EPROM to directly coincide to the specific address inputs from the AY-5-3600-PRO. Any PROM whether it be bipolar, ultraviolet erasable or electrically alterable, may be employed to provide a wide variety of "off-the-shelf" keyboards. Once the keyboard assembly has gone beyond the prototyping stage, and assuming the quantity/cost permit, the PROM/EPROM data can be converted to the standard AY-5-3600 data format (ref. AY-5-3600 Custom Coding Information sheet) and produced in production quantities. This eliminates the PROM/EPROM expense while assuring the absence of undefined coding changes.

Summary of Important Features

- Ability to deliver complete keyboard assemblies within days without sacrificing the features offered in the AY-5-3600 Keyboard Encoder.
- Ability to buy off-the-shelf devices (distributor, etc.)
- Ability to verify the specific pattern format using a PROM/EPROM prior to a 'custom' encoder commitment.

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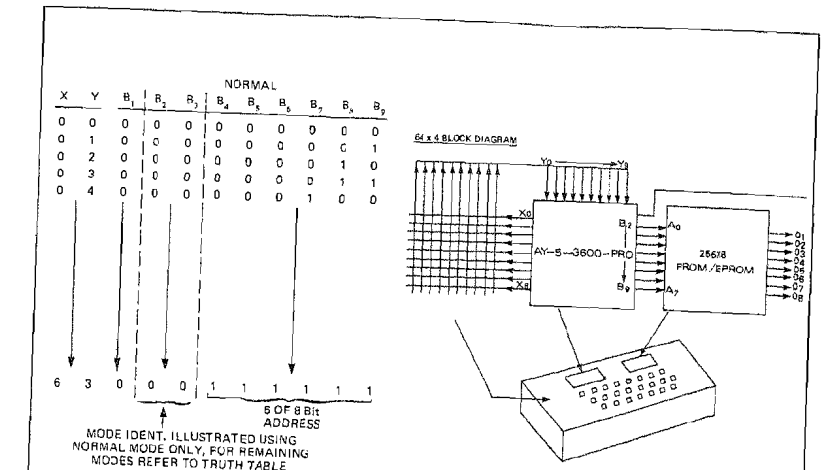


Fig.8 64 KEY 4 MODE KEYBOARD APPLICATION

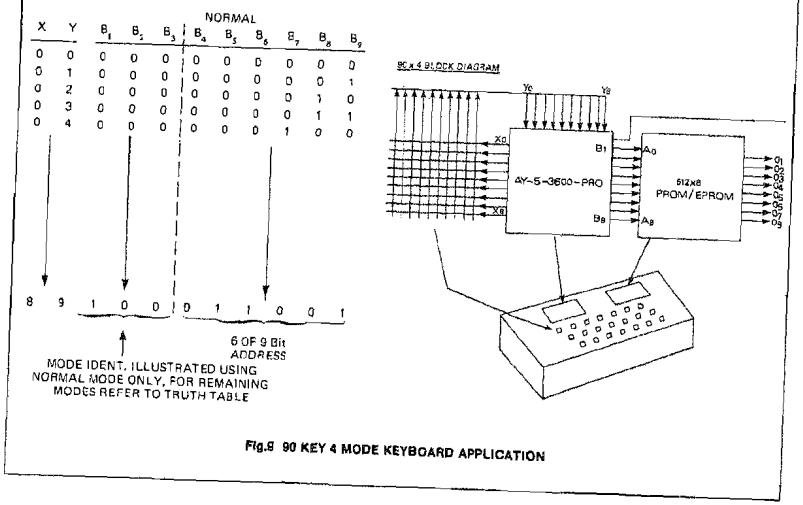


Fig.9 90 KEY 4 MODE KEYBOARD APPLICATION

OPTIONS

- Device Marking: AY-5-3600-PRO
- Internal Oscillator on Pin Nos. 1, 2, 3
- Lockout/Rollover on Pin No. 4
  Internal Resistor to V_{DD} on Lockout/Rollover Pin
- True Outputs Only
- Any Key Output on Pin No. 5.
  Any Key Output True (Logic 1) During Key Depression
- Pulse Data Ready Signal
- Plastic Package
- Internal Resistor to V_{GG} on Shift/Control Pin

XY	NORMAL	SHIFT	CONTROL	SHFT/CTR	XY	NORMAL	SHIFT	CONTROL	SHFT/CTR
0	000000000	001000000	010000000	011000000	45	000101101	001101101	010101101	011101101
1	000000001	001000001	010000001	011000001	46	000101110	001101110	010101110	011101110
2	000000010	001000010	010000010	011000010	47	000101111	001101111	010101111	011101111
3	000000011	001000011	010000011	011000011	48	000110000	001110000	010110000	011110000
4	000000100	001000100	010000100	011000100	49	000110001	001110001	010110001	011110001
5	000000101	001000101	010000101	011000101	50	000110010	001110010	010110010	011110010
6	000000110	001000110	010000110	011000110	51	000110011	001110011	010110011	011110011
7	000000111	001000111	010000111	011000111	52	000110100	001110100	010110100	011110100
8	000001000	001001000	010001000	011001000	53	000110101	001110101	010110101	011110101
9	000001001	001001001	010001001	011001001	54	000110110	001110110	010110110	011110110
10	000001010	001001010	010001010	011001010	55	000110111	001110111	010110111	011110111
11	000001011	001001011	010001011	011001011	56	000111000	001111000	010111000	011111000
12	000001100	001001100	010001100	011001100	57	000111001	001111001	010111001	011111001
13	000001101	001001101	010001101	011001101	58	000111010	001111010	010111010	011111010
14	000001110	001001110	010001110	011001110	59	000111011	001111011	010111011	011111011
15	000001111	001001111	010001111	011001111	60	000111100	001111100	010111100	011111100
16	000010000	001010000	010010000	011010000	61	000111101	001111101	010111101	011111101
17	000010001	001010001	010010001	011010001	62	000111110	001111110	010111110	011111110
18	000010010	001010010	010010010	011010010	63	000111111	001111111	010111111	011111111
19	000010011	001010011	010010011	011010011	64	100000000	101000000	110000000	111000000
20	000010100	001010100	010010100	011010100	65	100000001	101000001	110000001	111000001
21	000010101	001010101	010010101	011010101	66	100000010	101000010	110000010	111000010
22	000010110	001010110	010010110	011010110	67	100000011	101000011	110000011	111000011
23	000010111	001010111	010010111	011010111	68	100000100	101000100	110000100	111000100
24	000011000	001011000	010011000	011011000	69	100000101	101000101	110000101	111000101
25	000011001	001011001	010011001	011011001	70	100000110	101000110	110000110	111000110
26	000011010	001011010	010011010	011011010	71	100000111	101000111	110000111	111000111
27	000011011	001011011	010011011	011011011	72	100001000	101001000	110001000	111001000
28	000011100	001011100	010011100	011011100	73	100001001	101001001	110001001	111001001
29	000011101	001011101	010011101	011011101	74	100001010	101001010	110001010	111001010
30	000011110	001011110	010011110	011011110	75	100001011	101001011	110001011	111001011
31	000011111	001011111	010011111	011011111	76	100001100	101001100	110001100	111001100
32	000100000	001100000	010100000	011100000	77	100001101	101001101	110001101	111001101
33	000100001	001100001	010100001	011100001	78	100001110	101001110	110001110	111001110
34	000100010	001100010	010100010	011100010	79	100001111	101001111	110001111	111001111
35	000100011	001100011	010100011	011100011	80	100010000	101010000	110010000	111010000
36	000100100	001100100	010100100	011100100	81	100010001	101010001	110010001	111010001
37	000100101	001100101	010100101	011100101	82	100010010	101010010	110010010	111010010
38	000100110	001100110	010100110	011100110	83	100010011	101010011	110010011	111010011
39	000100111	001100111	010100111	011100111	84	100010100	101010100	110010100	111010100
40	000101000	001101000	010101000	011101000	85	100010101	101010101	110010101	111010101
41	000101001	001101001	010101001	011101001	86	100010110	101010110	110010110	111010110
42	000101010	001101010	010101010	011101010	87	100010111	101010111	110010111	111010111
43	000101011	001101011	010101011	011101011	88	100011000	101011000	110011000	111011000
44	000101100	001101100	010101100	011101100	89	100011001	101011001	110011001	111011001

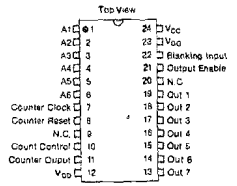
Character Generator

FEATURES

- FULL TTL/DTL COMPATIBILITY
  No external interfacing components required.
- 1 μs TYP. ACCESS TIME/STATIC OPERATION
  The output date remains valid as long as the input data/internal counter remain unchanged.
- COLUMN OUTPUT
  2240 bits of storage organized as 64 5X7 dot matrix characters with column by column output.
- INTERNAL COUNTER
  Provides sequential column selection from a single counter clock input.
- COUNT CONTROL
  Allows the selection of either one or two column intercharacter spacing.
- COUNTER OUTPUT
  Provides an "update" signal for external character address registers.
- BLANKING AND OUTPUT ENABLE
  Provide full output control without affecting any other ROM function.
- ZENER PROTECTED INPUTS
- GLASS PASSIVATION PROTECTION

PIN CONFIGURATION

24 LEAD DUAL IN-LINE

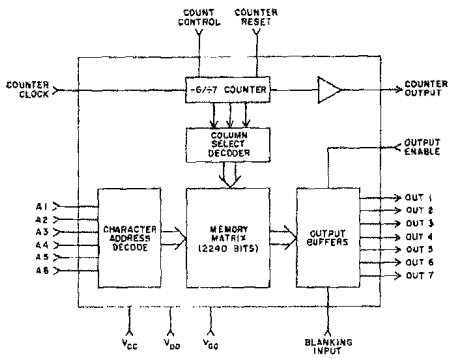


DESCRIPTION

The General Instrument RO-5-2240S is a 2240 bit Read Only Memory organized as a 320 words X 7 bits character generator (64 characters, each having 5 columns of 7 bits). Column by column character data is provided for vertical scan display applications. An internal counter and a full complement of control signals allow for the greatest system design flexibility. The RO-5-2240S is constructed on a single monolithic chip utilizing P-channel enhancement mode transistors.

The memory is available with custom character coding or pre-programmed with ASCII encoded characters having the fonts shown on Page 2 of this data sheet.

BLOCK DIAGRAM



OPERATING DESCRIPTION

Character selection is achieved by presenting a six-bit binary word at the Character Address inputs. Column selection is achieved by clocking an internal counter from the Counter Clock input. Column information appears sequentially at the seven Data Outputs, beginning with the left-most column.

Two additional column positions, aside from the five required for character presentation, are available for spacing between adjacent characters. The Count Control input is used to determine whether one or both positions will be used. Between characters, the Data Outputs are high (+5V), the "no-dot" condition. The Counter Reset input is available to reset the counter into the last (sixth or seventh) state.

The Counter Output is provided to synchronize other system components to the ROM internal counter. An output appears corresponding to the last (sixth or seventh) counter state and can be conveniently used to clock an external input data register.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM function. Data Outputs can also be open-circuited for wire-ORed operation by use of the Output Enable input.

Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.

OPERATING NOTES

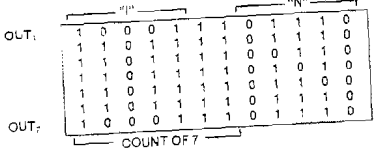
The following table summarizes the RO-2240S input control states and corresponding drive levels:

Count Control	
– 6	-12
– 7	+5V
Counter Reset	
Operate	+5V
Reset	OV
Blanking Input	
Unblank	+5V
Blank*	OV
Output Enable	
Enable	+5V
Disable**	OV

* All data outputs high (+5V)
** All data outputs open-circuited

TIMING DIAGRAMS

Timing diagram (1) shows the time relationships between character address, data output, counter clock and counter output during typical operation of an RO-5-2240S character generator. An output sequence from the RO-5-2240S-001 is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".



All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control, +5V
Counter Reset, +5V
Blanking Input, +5V
Output Enable, +5V

Had the Count Control input been at –12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

Timing diagrams (3) through (5) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

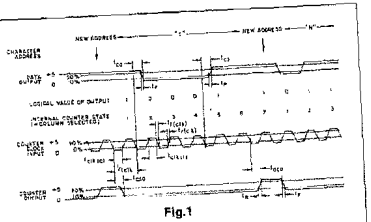


Fig.1


Fig.2

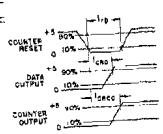


Fig.3

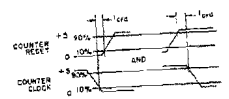


Fig.4

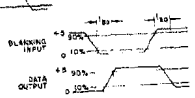


Fig.5

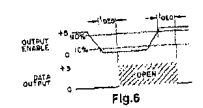


Fig.6

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{GG} and V_{DD} with respect to V_{CC}	−20V to +0.3V
Inputs with respect to V_{CC}	−20V to +0.3V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±0.25 Volts (V_{CC} is the substrate voltage)
V_{GG} = −12 Volts ±0.6 Volts
V_{DD} = GND
Operating Temperature (T_A) = 0°C to +70°C
One TTL load (C_L total = 15 pF)

Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Inputs (Note 1)						
Logic 1 Level	V_{IH}	V_{CC}−1.5	—	—	Volts	
Logic 0 Level	V_{IL}	—	—	+0.8	Volts	
Leakage	I_{LI}	—	—	10	µA	$V_{in} = V_{CC}$−6V, T_A = 25°C
Count Control						
÷6 Operation	V_{ICC}	−12.6	−12.0	−11.4	Volts	Returned to V_{DD} for ÷ 6 operation.
÷ 7 Operation	V_{ICC}	+4.75	+5.0	+5.25	Volts	Returned to V_{CC} for ÷ 7 operation
Leakage	I_{LCC}	—	—	10	µA	$V_{in} = V_{CC}$ − 6V, T_A = 25°C
Outputs (Note 2)						
Logic 1 Level	V_{OH}	2.8	—	—	Volts	I_{OH} = 100 µA
Logic 0 Level	V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6 mA
Power						
Supply Current	I_{GG}	—	20	40	mA	Outputs unconnected,
Supply Current	I_{SS}	—	20	40	mA	f_{clk} = 200 KHz
AC CHARACTERISTICS						
Counter Clock						
Frequency	f_{clk}	DC	—	200	KHz	
Pulse Width	$t_{clk(0)}$	2.0	—	—	µs	
Pulse Delay	$t_{clk(1)}$,	2.0	—	—	µs	
Rise and Fall Times	$t_{r(clk)}$, $t_{f(clk)}$	—	—	100	ns	$t_{r(clk)} + t_{clk(0)} + t_{f(clk)}$
Counter Reset						$+t_{ck}(0) \geq 5\mu$sec
Pulse Width	t_{cp}	1.0	—	—	µs	
Pulse Delay	t_{cd}	0.4	—	—	µs	
Capacitance (Note 1)	C_{in}	—	—	10	pF	Note (3)
Outputs						1 MHz, T_A = +25°C
Address to Output Delay	t_{AO}	—	1.0	1.5	µs	
Clock to Output Delay	t_{CO}	—	1.0	1.5	µs	
Clock to Counter Output Delay	t_{CCO}	—	1.0	1.5	µs	
Blanking/Unblanking Delay	t_{BO}	—	1.0	1.5	µs	
Output Enable/Disable Delay	t_{OEO}	—	1.0	1.5	µs	
Counter Reset Delay	t_{CRO}	—	1.0	1.5	µs	
Reset to Counter Output Delay	t_{CRCO}	—	1.0	1.5	µs	
Output Rise and Fall Time	t_r, t_f	—	—	0.3	µs	

**Typical values are at +25°C and nominal voltages.

NOTES:
1. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
2. These parameters apply to both the date outputs and counter output.
3. The counter clock must not make a negative transition within the period t_{cs}, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

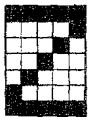
CODING AND CHARACTER FONTS

The RO-5-2240S-001 is a pre-programmed member of the RO-5-2240S series with ASCII encoding and the character fonts shown on the right. A logic "1" represents an input or output voltage equal to V_{SS} (+5V) and a logic "0" represents a voltage equal to V_{DD} (0V).

An example demonstrating the correspondence of device outputs and sequence to the 5x7 dot matrix fonts is shown below:

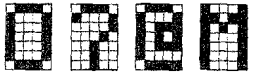
	1	2	3	4	5
OUT_1 →	0	0	0	0	0
OUT_2 →	1	1	1	1	0
OUT_3 →	1	1	1	0	1
OUT_4 →	1	1	0	1	1
OUT_5 →	1	0	1	1	1
OUT_6 →	0	1	1	1	1
OUT_7 →	0	0	0	0	0

output sequence



The RO-5-2240S-002 is pre-programmed with a character font identical to the font for the RO-5-2240S-001 below with the exception of the characters '0', '7', '@', and 'M'.

The RO-5-2240S-002 font for these characters is shown below:



RO-5-2240S-001				A_6 / A_5	1 / 0	1 / 1	0 / 0	0 / 1
A_4	A_3	A_2	A_1	COL / ROW	2	3	4	5
0	0	0	0	0				
0	0	0	1	1				
0	0	1	0	2				
0	0	1	1	3				
0	1	0	0	4				
0	1	0	1	5				
0	1	1	0	6				
0	1	1	1	7				
1	0	0	0	8				
1	0	0	1	9				
1	0	1	0	10				
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13				
1	1	1	0	14				
1	1	1	1	15				

14

Character Generator

FEATURES

- 64X8X5 Organization — ideal for systems requiring a row scan 5x7 dot matrix character generator
- Single +5 Volt Supply
- TTL Compatible — all inputs and outputs
- Static Operation — no clocks required
- 450ns Maximum Access Time
- 175mW Maximum Power
- Three-State Outputs — under the control of an 'Output Inhibit' input to simplify memory expansion
- Standard ASCII (RO-3-2513/CGR-001) or Totally Automated Custom Programming Available
- Zener Protected Inputs
- Glass Passivation Protection

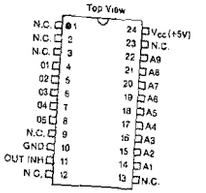
DESCRIPTION

The General Instrument RO-3-2513 is a 2560 bit static Read-Only Memory organized as 512 five bit words and is ideally suited for use as a Character Generator. Fabricated in GI's advanced GIANT II N-channel Ion-Implant process to enable operation from a single +5 Volt power supply, the RO-3-2513 can store, for high speed raster scan CRT displays, a full 64 characters in a standard 5x7 dot matrix format.

The RO-3-2513 is available pre-programmed with ASCII encoded 5x7 characters (GI part no. RO-3-2513/CGR-001) a direct replacement in pin connection, operation, and character font for the Signetics 2513/CM2140. The RO-3-2513 is also available pre-programmed with lower case ASCII encoded 5x7 characters (GI part no. RO-3-2513/CGR-005), a direct replacement for the Signetics 2513/CM3021.

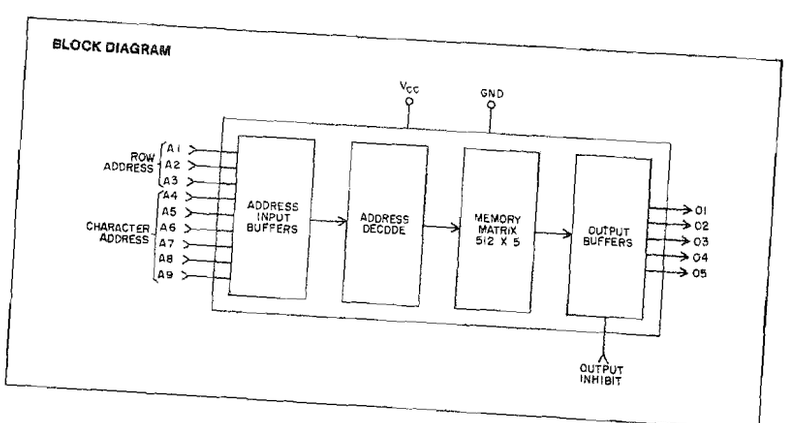
PIN CONFIGURATION

24 LEAD DUAL IN LINE



A separate publication, "RO-3-2513 Custom Coding Information," available from GI Sales Offices, describes the punched card and truth table format for custom programming of the RO-3-2513 memory.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} and input voltages (with respect to GND) . . . −0.3V to +8.0V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature (T_A) . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied—operating conditions are specified below.

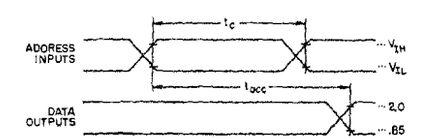
Standard Conditions (unless otherwise noted)

V_{CC} = +5 Volts ±5%
Operating Temperature (T_A) = 0°C to +70°C
Output Loading: One TTL load, $C_{L\ TOTAL}$ = 50pF.

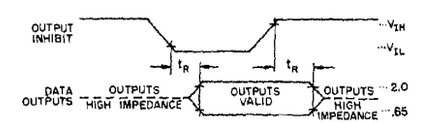
Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Address, Output Inhibit Inputs						
Logic "1"	V_{IH}	2.2	—	—	V	
Logic "0"	V_{IL}	—	—	0.65	V	
Leakage	I_{LI}	—	—	10	μA	
Data Outputs						
Logic "1"	V_{OH}	2.2	—	—	V	I_{OH} = 100μA
Logic "0"	V_{OL}	—	—	0.45	V	I_{OL} = 1.6mA
Leakage	I_{LO}	—	—	10	μA	
Power Supply Current						
I_{CC}	—	—	25	33	mA	Outputs open
AC CHARACTERISTICS						
Inputs						
Cycle Time	t_C	400	—	—	ns	
Capacitance	C_I	—	5	8	pF	f = 1MHz
Data Outputs						
Access Time	t_{ACC}	75	250	450	ns	
Inhibit Response Time	t_{IR}	—	150	200	ns	
Capacitance	C_O	—	8	10	pF	f = 1MHz

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS



A. ACCESS TIME (ADDRESS TO OUTPUT-OUTPUT INHIBIT AT LOGIC '0')



B. INHIBIT RESPONSE TIME (ADDRESS INPUTS STABLE)

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RO-3-2513-001 STANDARD PATTERN CHARACTER FORMAT (Upper Case ASCII)

The RO-3-2513/CGR-001 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5×7 dot matrix font is shown below:

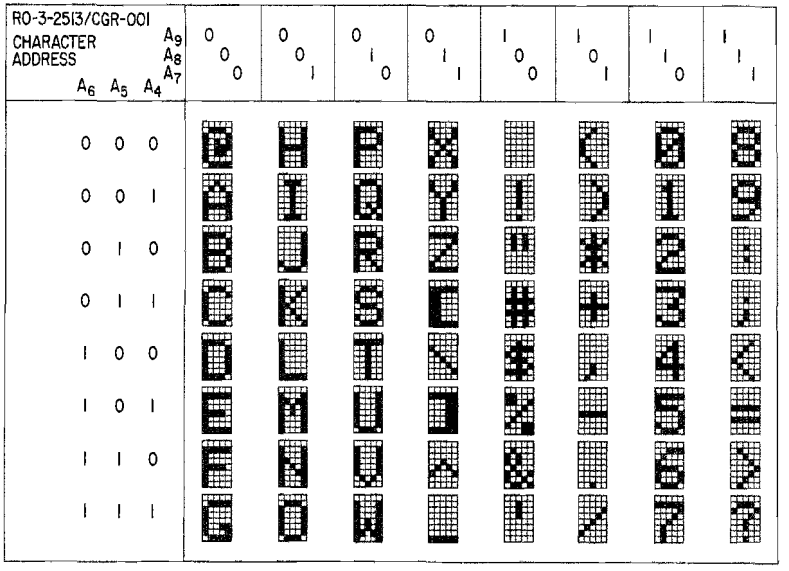
	CHARACTER ADDRESS					
RO-3-2513/CGR-001 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII upper case "S" Character	0	1	0	0	1	1

ROW ADDRESS

A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	0	0	0	1
0	1	1	1	0



RO-3-2513-005 STANDARD PATTERN CHARACTER FORMAT (Lower Case ASCII)

The RO-3-2513/CGR-005 is a pre-programmed version of the RO-3-2513 series with ASCII encoding and the character font shown below. A logic "1" represents an input or output voltage nominally equal to Vcc (+5V) and a logic "0" represents a voltage nominally equal to GND (0V).

An example demonstrating the correspondence of device outputs and addressing sequence to the 5×7 dot matrix font is shown below.

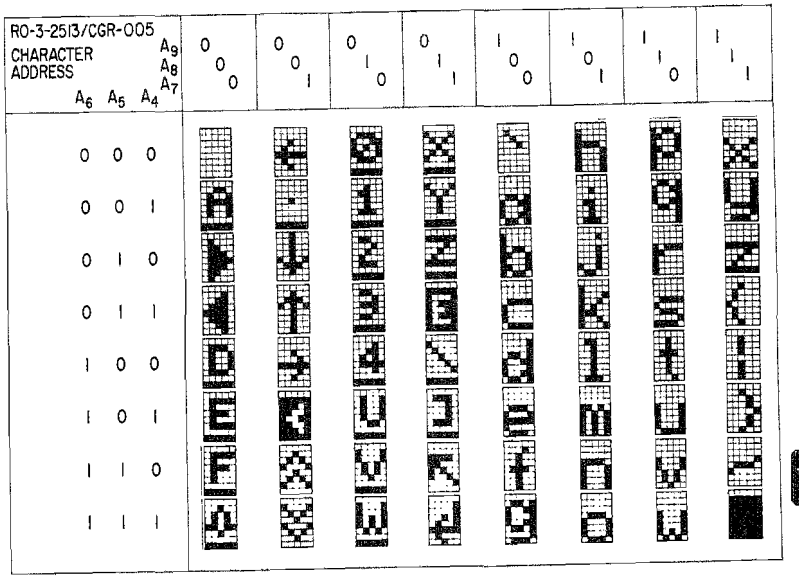
	CHARACTER ADDRESS					
RO-3-2513/CGR-005 Address Bit	A9	A8	A7	A6	A5	A4
ASCII Bit	6	5	4	3	2	1
ASCII lower case 's' Character	1	1	0	0	1	1

ROW ADDRESS

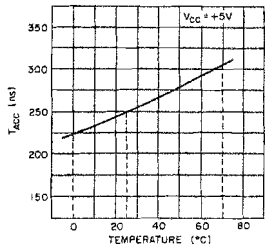
A_3	A_2	A_1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS

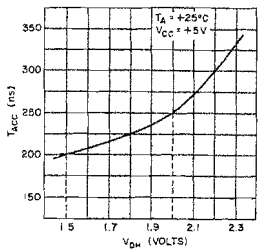
O_5	O_4	O_3	O_2	O_1
0	0	0	0	0
0	0	0	0	0
0	0	0	0	0
0	1	1	1	0
1	0	0	0	0
0	1	1	1	0
0	0	0	0	1
1	1	1	1	0



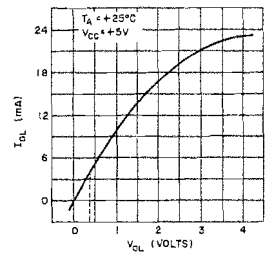
TYPICAL CHARACTERISTIC CURVES



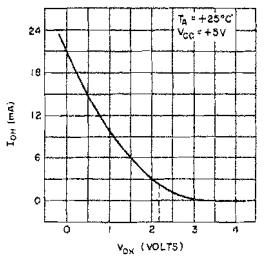
ACCESS TIME vs. TEMPERATURE



ACCESS TIME vs. OUTPUT VOLTAGE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

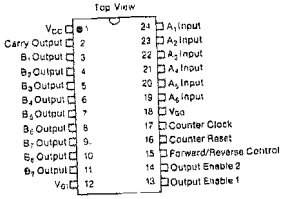
Character Generator

FEATURES

- Designed to drive Needle Printers.
- Internal counter provides sequential column scanning.
- Forward/Reverse Control for left to right and right to left printing capability.
- Carry Output available for synchronization.
- Three-State output configuration.
- Two mask programmable Output Enable pins to allow memory expansion.
- ASC II coded standard part, RO-5-5184-3000.
- Mask programmable counter length to allow flexibility in character organization.

PIN CONFIGURATION

24 LEAD DUAL IN LINE



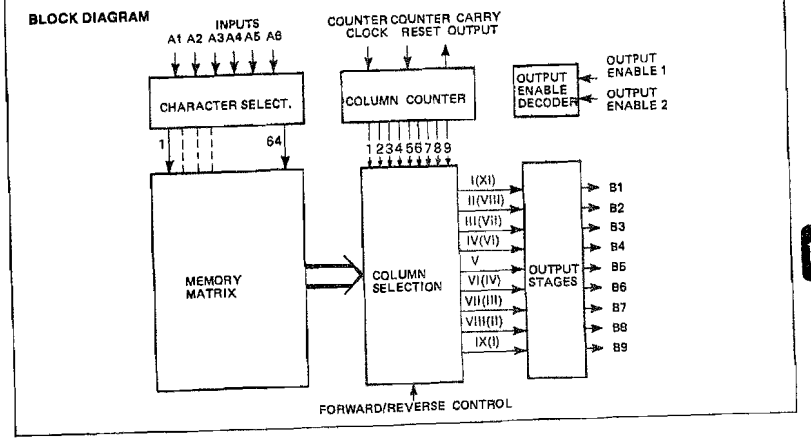
DESCRIPTION

The RO-5-5184 is a 5184 bit Static Read Only Memory organized as 64 permanent storage locations of 81 bits each (9×9 character matrix). Six address lines are used for the selection of 64 different characters. An internal ring counter is provided for column scanning; column information appears sequentially on the 9 output lines. A Counter Reset Input is available to initialize the sequential scanning. A Carry Output is provided to synchronize external circuitry to the internal column counter. The Forward/Reverse Control allows scanning from left to right or from right to left.

The 9 output lines have tri-state configuration. Two mask programmable Output Enable pins are provided for expansion up to a 5184 × 4 bit system without external logic.

Low threshold P-channel enhancement mode metal gate technology is used for input/output direct TTL compatibility. All inputs are zener protected

BLOCK DIAGRAM



14

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{CC}	−20V to +0.3V
Temperature Range	−55° C to +125°C
Operating Temperature	0°C to +70°C

*Exceeding these ratings could cause permanent damage to this device. Functional operation at these conditions is not implied — operating conditions are specified below.

Standard Conditions (unless otherwise noted)

V_{CC} = +5V ±0.5V
V_{DI} = GND
V_{GG} = −12V ±1V

Characteristics apply over temperature range unless otherwise stated.

Characteristic	Min	Typ**	Max	Units	Conditions
Counter Clock Input					
Repetition Rate	D.C.	350	200	KHz	
Pulse Width, ϕw	1.2	—	—	μs	At a logic '1' level
Pulse Separation, ϕs	1.2	—	—	μs	At a logic '0' level
Rise & Fall Times, tr, tf	—	—	1.0	μs	
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Logic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f = 1MHz
Address Inputs					
Logic '0' Level, V_{IL}	—	—	+0.8	Volts	
Logic '1' Level, V_{IH}	V_{CC}−1.5	—	—	Volts	
Input Leakage, I_{IN}	—	—	10	μA	Measured at $V_{IN} = V_{CC}$−10V at 25°C
Input Capacitance, C_{IN}	—	10	—	pF	$V_{IN} = V_{CC}$, f= 1MHz
Reset Input					
Counter Clock to Reset					
Pulse delay, t_{CRD}	1.0	—	—	μs	Fig.1
Reset pulse width	3.0	—	—	μs	Fig.2
Data Outputs					
Logic '0' Level, V_{OL}	—	—	0.4	Volts	I_{OL} = 1.6mA
Logic '1' Level, V_{OH}	V_{CC}−1.0	—	—	Volts	I_{OH} = 100 μA
Clock to Output delay time, t_{CO}	—	2.5	3.5	μs	
Clock to Carry Output delay time t_{CC}	—	1.5	2.5	μs	Figs. 3,4,5,6,7, & 8
Address to Output delay time, t_{AO}	—	2.5	3.5	μs	1 TTL, 16pF load
Reset to Output delay time, t_{RES}	—	2.5	5.0	μs	T_A = 25°C
Forward/Reverse to Output delay time, t_{FRO}	—	2.5	3.5	μs	
Output Enable delay time, t_{OEO}	—	1.5	2.5	μs	
Power Consumption, P_D	—	250	—	mW	T_A = 25°C

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAMS

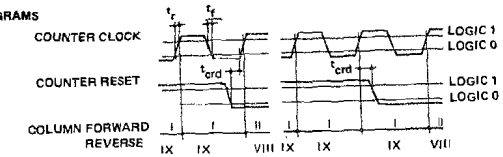


Fig.1 CLOCK TO RESET DELAY TIME

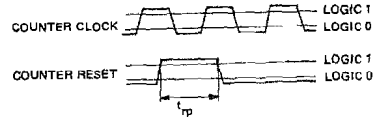


Fig.2 RESET PULSE WIDTH

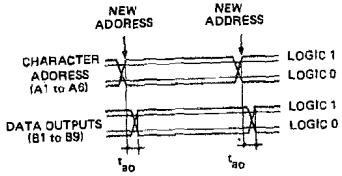


Fig.3 ADDRESS TO OUTPUT DELAY TIME

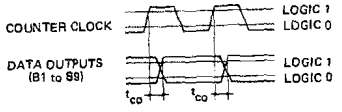


Fig.4 CLOCK TO OUTPUT DELAY TIME

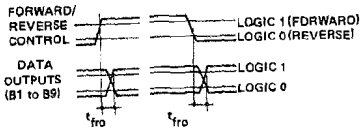


Fig.5 FORWARD/REVERSE TO OUTPUT DELAY TIME

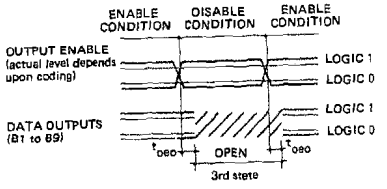


Fig.6 OUTPUT ENABLE TO OUTPUT DELAY TIME

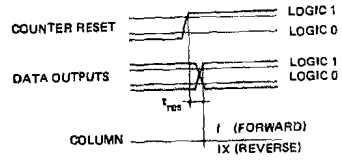


Fig.7 RESET TO OUTPUT DELAY TIME

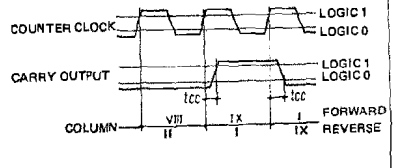


Fig.8 CLOCK TO CARRY DELAY TIME

14

OPERATION

CHARACTER SELECTION

Six address inputs are provided for selection of the 64 different characters. The address inputs are binary weighted (A_1 is the LSB).

COLUMN SELECTION

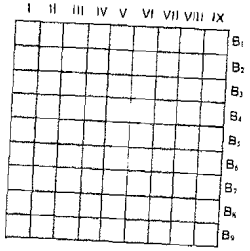
Column selection depends upon Forward/Reverse Control which permits the scanning of characters either from the first (I) to the last (IX) or from the last (IX) to the first (I) column as shown in fig.9. By changing line by line the logic value of Forward/Reverse control printing alternatively left to right or right to left is possible (see fig.10).

This feature allows faster printing by eliminating the fly back dead time between lines. The logic level of Forward/Reverse Control has to be constant "1" for left to right scanning and constant "0" for right to left scanning.

Fig.9 COLUMN SELECTION

FORWARD				REVERSE			
Count Reset	Column Count. State	Charact. Column	Carry Outp.	Count Reset	Column Count. State	Charact. Column	Carry Outp.
0	1	I	0	0	1	IX	0
0	2	II	0	0	2	VIII	0
0	3	III	0	0	3	VII	0
0	4	IV	0	0	4	VI	0
0	5	V	0	0	5	V	0
0	6	VI	0	0	6	IV	0
0	7	VII	0	0	7	III	0
0	8	VIII	0	0	8	II	0
0	9	IX	0	0	9	I	0
0	1	I	1	0	1	IX	1
0	2	II	0	0	2	VIII	0
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
0	8	VIII	0	0	8	II	0
0	9	IX	1	0	9	I	1
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0
1	1	I	0	1	1	IX	0

CHARACTER MATRIX



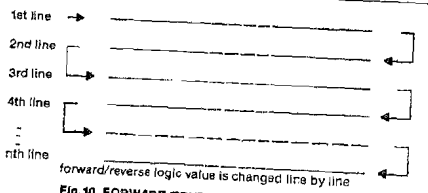


Fig.10 FORWARD/REVERSE PRINTING

OUTPUT ENABLE DECODER

Two Output Enable lines are provided for chip selection, when a chip is not selected the outputs are disabled (high impedance).

Output Enable signals are internally decoded by a mask programmable decoder to minimize logic for memory expansion.

The output enable code assigned to different RO-5-5184 is permanently programmed into the ROM at the same time as the custom data pattern.

A system of $4 \times 5184 = 20736$ bit character generator needing no external enable logic is easily obtained wiring the outputs of four different RO-5-5184 together as shown on fig.11.

OUTPUT ENABLE CODING						
RO-5-5184	Output Enable 1	Output Enable 2	DEVICE SELECTION A	B	C	D
A	0	0	selected	—	—	—
B	1	0	—	selected	—	—
C	0	1	—	—	selected	—
D	1	1	—	—	—	selected

COLUMN COUNTER

This counter operates on the positive going edges of the Counter Clock.

Each counter cell is implemented with a cross coupled flip-flop so that the counter position is fully static.

Carry Output is active (logic '1') when the counter is in the last position, to indicate that a character has been fully scanned.

When active (logic '1') the Counter Reset Input resets the counter in the first position to initialise the scanning.

The counting length is mask programmable, it is possible to program any length between five and nine.

OUTPUT STAGES

Nine TTL compatible Outputs (B_1 to B_9) are provided to show the memory content.

The Tri-state configuration of output stages allows bus structure for memory expansion under the control of Output Enable signals.

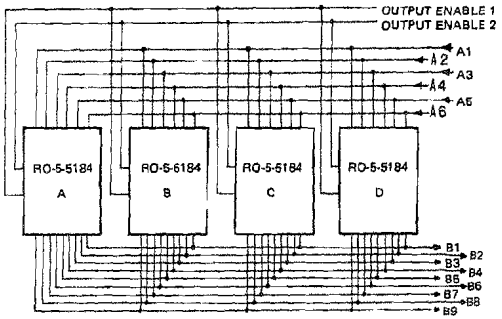
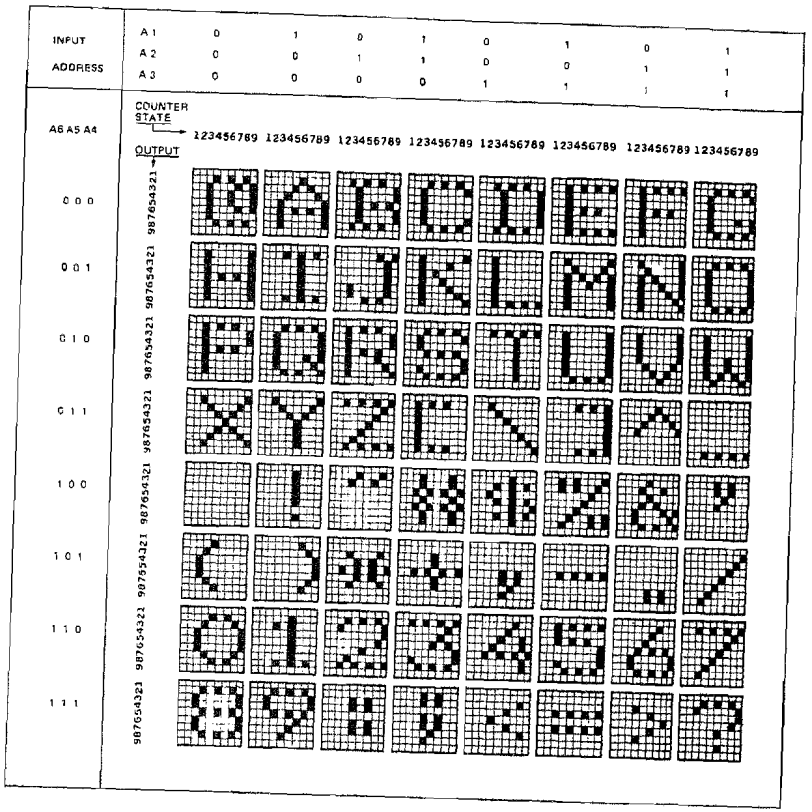


Fig.11

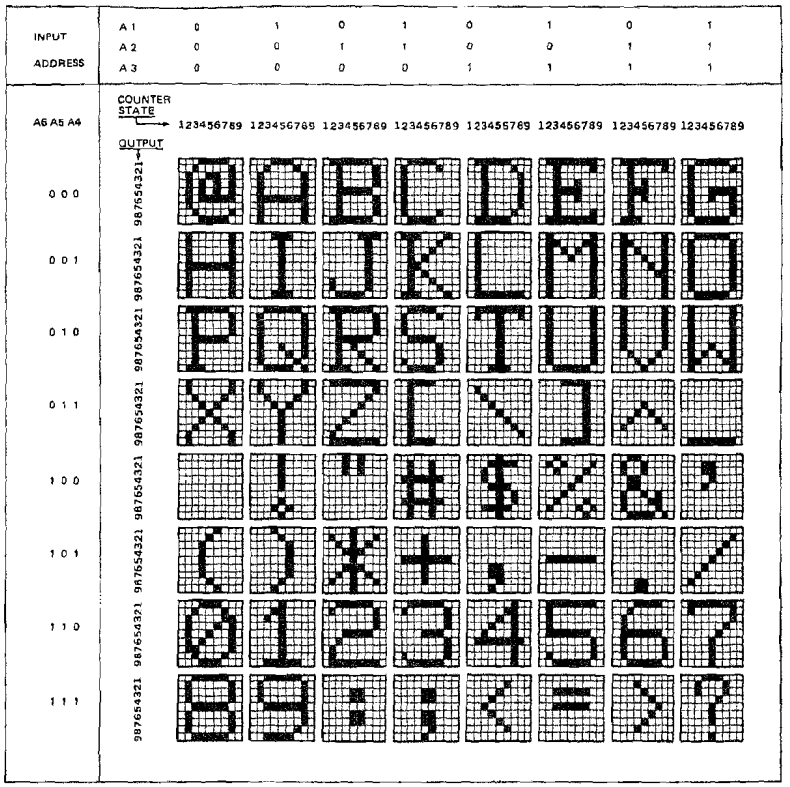
RO-5-5184-050 STANDARD PATTERN CHARACTER FORMAT



SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE	X	

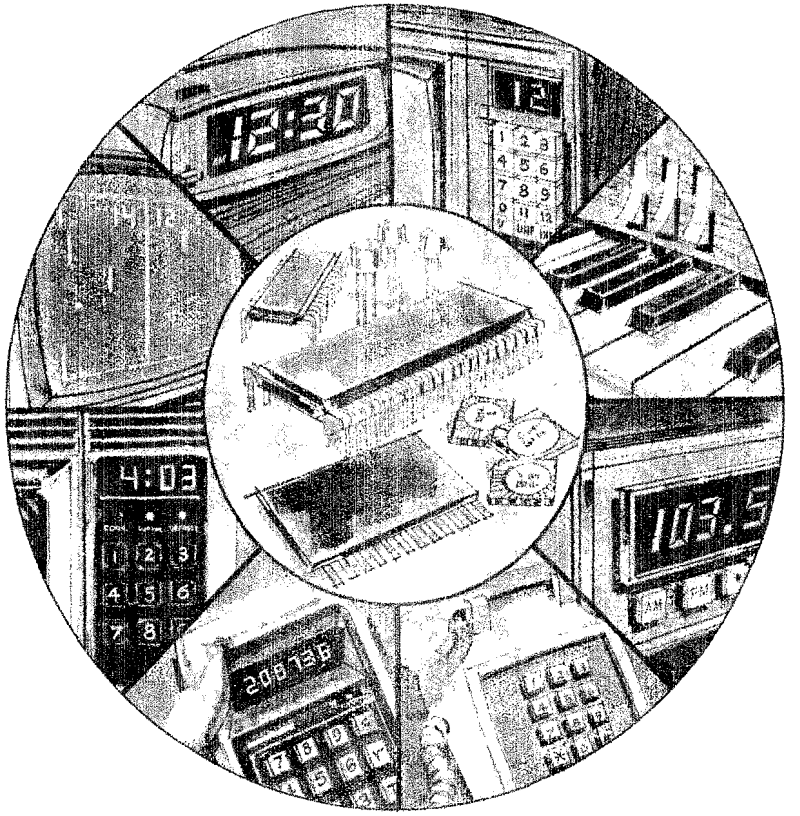
OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED	X			

RO-5-5184-3000 STANDARD PATTERN CHARACTER FORMAT



SHADED SQUARE	+5	0
BLANK SQUARE	0	+5
DESIRED OUTPUT VOLTAGE		X

OUTPUT ENABLE 1	0	+5	0	+5
OUTPUT ENABLE 2	0	0	+5	+5
DEVICE SELECTED				X



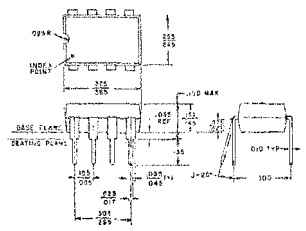
PACKAGE OUTLINES/ SALES OFFICES

MICRO ELECTRONICS

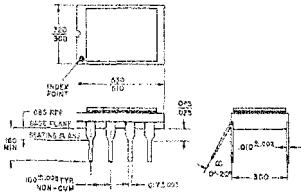
A

PACKAGE OUTLINES

PACKAGE OUTLINES (All dimensions in inches)
8 LEAD DUAL IN LINE

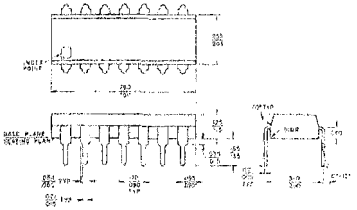


PLASTIC

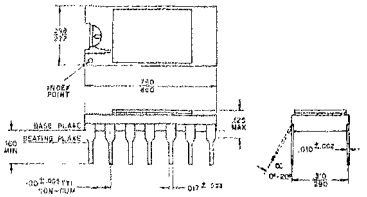


CERAMIC

14 LEAD DUAL IN LINE

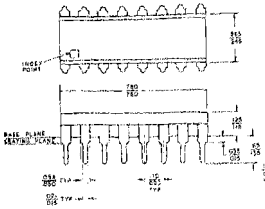


PLASTIC

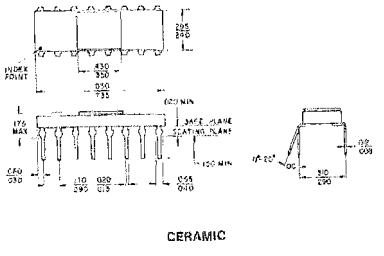


CERAMIC

PACKAGE OUTLINES (All dimensions in inches)
16 LEAD DUAL IN LINE

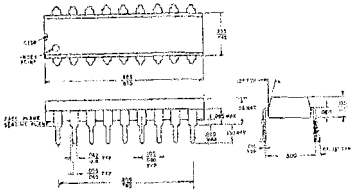


PLASTIC



CERAMIC

16 LEAD DUAL IN LINE



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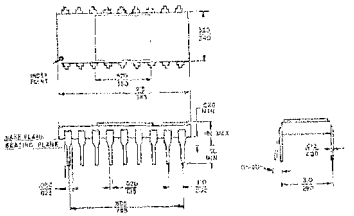
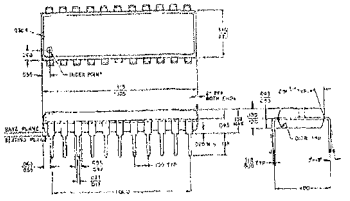


CERAMIC

22 LEAD DUAL IN LINE



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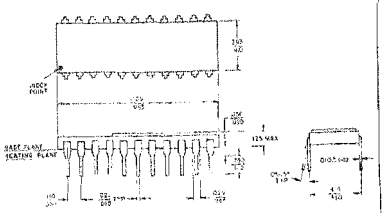
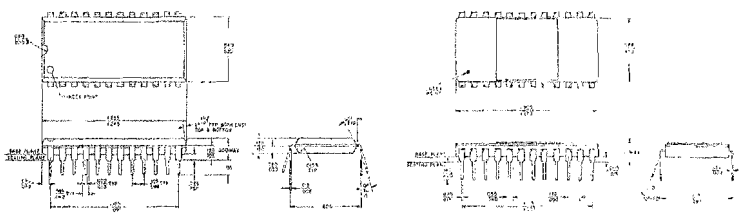


CERAMIC

A

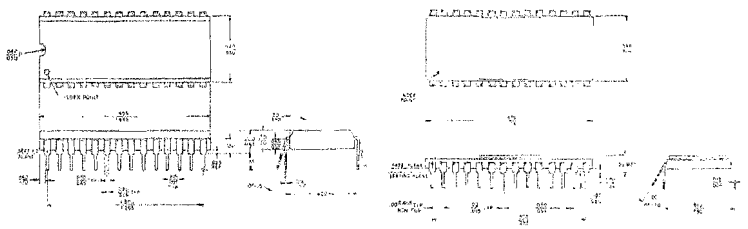
PACKAGE OUTLINES (All dimensions in inches)

24 LEAD DUAL IN LINE



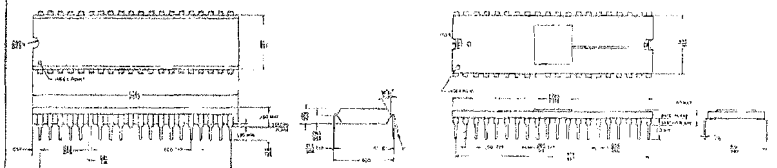
PLASTIC CERAMIC

28 LEAD DUAL IN LINE



PLASTIC CERAMIC

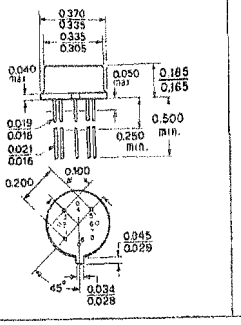
40 LEAD DUAL IN LINE



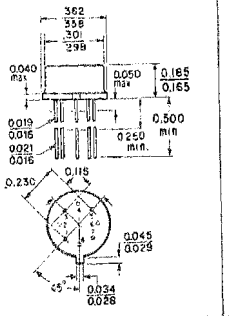
PLASTIC CERAMIC

PACKAGE OUTLINES (All dimensions in inches)

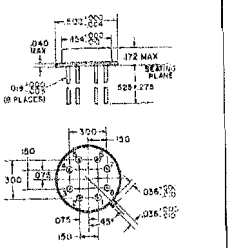
8 LEAD TO-78



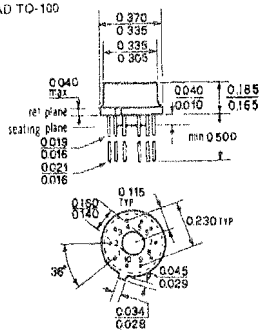
8 LEAD TO-99



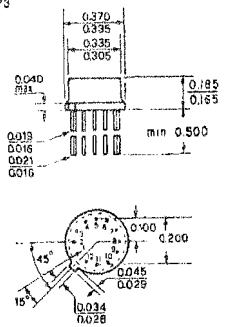
8 LEAD TO-8



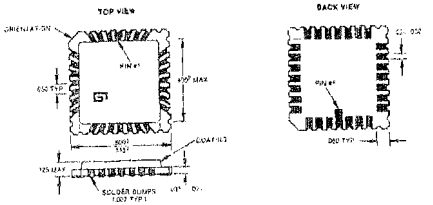
10 LEAD TO-100



12 LEAD TO-73



28 LEAD MINI-PAK



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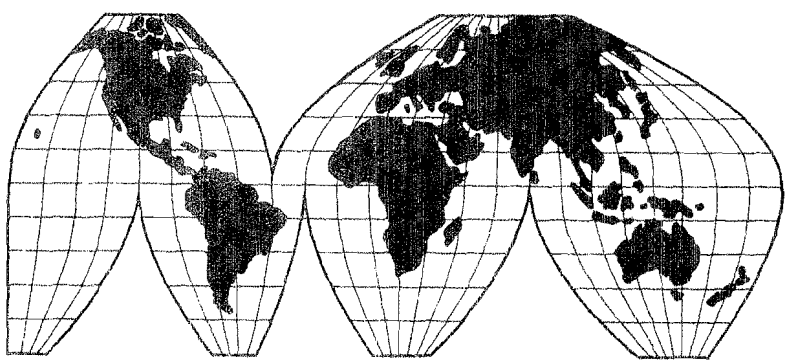

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Suite 219
Southfield, MI 48076
Tel. (313) 559-3660
TWX: 810-299-2535

MINNESOTA

Quantum Sales
7710 Computer Avenue
Minneapolis, MN 55435
Tel: (612) 831-8583
TWX: 910-576-2988

MISSOURI

P M A
140 Weldon Parkway
Maryland Heights, MO 63043
Tel (314) 569-1220

NEW JERSEY

R.T. Reid Assoc.
706 Cedar Lane
Teaneck, NJ 07666
Tel (201) 692-0200
TWX. 710-990-5086

NORTH CAROLINA

Component Sales
P.O. Box 18821
Raleigh, NC 27609
Tel: (919) 782-8433
TWX: 510-928-0513

OHIO

Bear Marketing
3623 Brecksville Road
Richfield OH 44286
Tel (216) 659-3131
TWX 810-427-9100

OREGON

Jas. J. Backer Co.
2035 S.W. 58th Street — Rm. 207
Portland, OR 97221
Tel (503) 297-3776

PENNSYLVANIA

Foster-McClinton
2867 Washington Road
Bridgeville, PA 15017
Tel: (412) 941-4800
Telex: 866477

Foster-McClinton
2131 W. 8th Street
Erie, PA 16505
Tel: (814) 455-9111
Telex: 914462

Knowles Assoc.
1 Fairway Plaza, Suite 30
Huntingdon Valley, PA 19006
Tel: (215) 947-5641
TWX 510-665-5303

TEXAS

Oeler & Menelaides
6065 Hillcraft
Houston TX 77035
Tel. (713) 772-0730
TWX 910-867-4745

Oeler & Menelaides
558 S. Central Expressway
Richardson, TX 75080
Tel (214) 234-6334
TWX: 910-867-4745

WASHINGTON

Jas. J. Backer Co.
221 West Galer Street
Seattle, WA 98119
Tel (206) 285-1300
TWX. 910-444-1646

WEST VIRGINIA

Foster-McClinton
17 Pembrooke Lane
Huntington, W VA 25705
Tel (304) 763-5161

CANADA

ONTARIO

Pipe-Thompson, Ltd.
83 Cumberland Drive
Mississauga, Ontario
Tel (416) 274-1269

A

UNITED STATES

ARIZONA

MIRCO
2005 W. Peoria Ave
Phoenix, AZ 85029
Tel: (602) 997-6194

CALIFORNIA

SEMI COMP
4029 Westerly Place
Newport Beach, CA 92660
Tel: (714) 833-3070

INTERMARK
4040 Sorrento Valley Rd
San Diego, CA 92121
Tel: (714) 279-5200

INTERMARK
1802 E. Carnegie Ave.
Santa Ana, CA. 92705
Tel: (714) 540-1322

DIPLOMAT
1118 Elko Dr.
Sunnyvale, CA. 94086
Tel: (408) 734-1900

INTERMARK
1020 Stewart Dr.
Sunnyvale, CA. 94086
Tel: (408) 738-1111

SEMICONDUCTOR CONCEPTS
20201 Oxnard St.
Woodland Hills, CA 91364
Tel. (213) 884-4560

COLORADO

CENTURY
8155 W. 48th Ave
Wheatridge, CO. 80033
Tel: (303) 424-1985

CONNECTICUT

ARROW
295 Treadwell St.
Hamden, CT. 06514
Tel: (203) 248-3801

FLORIDA

DIPLOMAT
1771 N. Hercules Ave.
Clearwater, FLA. 33515
Tel: (813) 443-4514

ARROW
1001 N.W. 62nd St.
Ft. Lauderdale, FLA. 33309
Tel: (305) 776-7790

ILLINOIS

HALL-MARK/CHICAGO
180 Crossen Ave.
Elk Grove Village, ILL. 60007
Tel: (312) 437-8800

INDIANA

FT. WAYNE ELECTRONICS
3606 E. Maumee Ave
Ft. Wayne, IN. 46803
Tel: (219) 423-3422

KANSAS

HALL-MARK/KANSAS CITY
11870 W. 91st St.
Shawnee Mission, KS 66214
Tel: (913) 888-4747

MARYLAND

ARROW
4801 Benson Ave
Baltimore, MD. 21227
Tel. (301) 247-5200

PIONEER
1037 Taft St.
Rockville, MD. 20850
Tel: (301) 424-3300

MASSACHUSETTS

DIPLOMAT
559 East Street
Chicopee Falls, MA. 01020
Tel: (413) 592-9441

DIPLOMAT
Kuniholm Dr.
Holliston, MASS 01746
Tel: (617) 429-4120

CRAMER
85 Wells Ave
Newton, MASS. 02159
Tel: (617) 964-4000

GREENE/SHAW
70 Bridge St.
Newton, MASS. 02158
Tel: (617) 969-8900

ARROW
960 Commerce Way
Woburn, MASS 01830
Tel: (617) 933-8130

MICHIGAN

DIPLOMAT
32708 W. Eight Mile Rd.
Farmington, MI. 48024
Tel: (313) 477-3200

MINNESOTA

ARROW
9700 Newton Ave. So.
Bloomington, MN. 55431
Tel: (612) 888-5522

HALL-MARK/MINNESOTA
9201 Penn Ave. So.
Minneapolis, MN. 55421
Tel. (612) 884-9066

MISSOURI

HALL-MARK/ST. LOUIS
13789 Rider Trail
Earth City, MO. 63045
Tel: (314) 291-5350

DIPLOMAT
2725 Mercantile Dr.
St. Louis, MO. 63144
Tel: (314) 645-8550

NEW JERSEY

ARROW
Pleasant Valley Rd.
Moorestown, N.J. 08057
Tel: (609) 235-1900

ARROW
285 Midland Ave.
Saddlebrook, N.J. 07662
Tel: (201) 797-5800

DIPLOMAT
490 S. Riverview Dr.
Totowa, N.J. 07511
Tel. (201) 785-1830

NEW MEXICO

CENTURY
121 Elizabeth N.E.
Albuquerque NM 87108
Tel: (505) 292-2700

NEW YORK

SUMMIT
916 Main St.
Buffalo, N.Y. 14202
Tel: (716) 884-3450

ZEUS
500 Executive Blvd.
Elmsford, N.Y. 10523
Tel: (914) 592-4120

ARROW
900 Broad Hollow Rd.
Farmingdale, N.Y. 11735
Tel: (516) 694-6800

ARROW
Old Route 9
Fishkill, N.Y. 12524
Tel: (914) 896-7530

SEMICONDUCTOR CONCEPTS
145 Oser Ave.
Hauppauge, N.Y. 11787
Tel: (516) 273-1234

DIPLOMAT
303 Crossway Park Dr
Woodbury, N.Y. 11797
Tel: (516) 921-9373

UNITED STATES

NORTH CAROLINA

PIONEER
2906 Baltic Ave
Greensboro, N.C. 27406
Tel. (919) 273-4441

OHIO

ARROW
23500 Mercantile Rd
Cleveland, OH. 44122
Tel. (216) 464-2000

ARROW
3160 Plainfield Rd.
Dayton, OH. 45404
Tel (513) 253-9176

OREGON

UNITED RADIO
123 N.E. 7th Ave
Portland, OR. 97214
Tel: (503) 233-7151

PENNSYLVANIA

PIONEER
203 Witmer Rd
Horsham, PA. 19044
Tel (215) 674-5710

HALL-MARK/PHILADELPHIA
458 Pike Rd
Huntingdon Valley, PA. 19006
Tel (215) 355-7300

TEXAS

HALL-MARK/DALLAS
9333 Forest Lane
Dallas, TX 75231
(214) 231-6111

HALL-MARK/HOUSTON
8000 Westglen
Houston, TX 77063
(713) 781-6100

UTAH

CENTURY ELECTRONIC
2150 So. 300 West
Salt Lake City, UT. 84115
Tel (801) 487-8551

DIPLOMAT
2260 So. Main St.
Salt Lake City, UT. 84115
Tel (801) 486-7227

WISCONSIN

ARROW
2925 South 160th St
New Berlin, WI. 53151
Tel: (414) 782-2601

HALL-MARK/MILWAUKEE
237 South Curtis
West Allis, WI. 53214
Tel: (414) 476-1270

CANADA

BRITISH COLUMBIA

RAE Industrial Electronics Ltd.
1629 Main Street
Vancouver, B.C.
Tel: (604) 687-2621
TWX. (610) 929-3065

MANITOBA

Cam Guard Supply & Service Ltd
1777 Ellice Avenue
Winnipeg, Manitoba
Tel: (204) 786-8481
Telex: 07-57622

ONTARIO

Downsview
Cesco Electronics Ltd.
24 Martin Ross Avenue
Downsview, Ontario
Tel (416) 661-0220
Telex: 02-29697

Ottawa
Cesco Electronics Ltd
1300 Carling Avenue
Ottawa, Ontario
Tel: (613) 729-5118
Telex: 053-3684

Rexdale
Future Electronics Corp
44 Fasken Drive, Unit 24
Rexdale, Ontario
Tel: (416) 667-7820

Willowdale
Electro Sonic Inc.
1100 Gordon Baker Road
Willowdale, Ontario
Tel: (416) 494-1666
Telex: 06-22030

QUEBEC

Montreal
Cesco Electronics Ltd.
4050 Jean Talon Street West
Montreal, Quebec
Tel: (514) 735-5511
Telex: 05-25590

Future Electronics Corp.
5647 Ferrier Street
Montreal, Quebec
Tel. (610) 421-3251
Telex: 05-827789

A

EUROPE

AUSTRIA
Elbatex GmbH
Breitenfurter Str. 381
A-1235 Wien
Tel 0222/869158
Telex: 013128

BELGIUM
C.P. Clare International N.V
102 Gen Gratty
Bruxelles 4
Tel: 02-736.01.97
Telex. 24157

DENMARK
A/S Nordisk--Elektronik
Transformervej 17
DK-2730 Herlev
Tel: 84.30.00
Telex 19219

FINLAND
Jorma Sarkkinen Ky.
Keikintori, P.O Box 19,
SF-02100 Tapiola
Tel: 46.10.68
Telex. 122028

FRANCE
P.E.P
4 Rue Barthelemy
92120 Montrouge,
Tel: 735.33.20
Telex: 204534

GERMANY
Frankfurt/Main
Berger Elektronik GmbH
Am Tiergarten 14
Tel: 0611/490311
Telex. 04-12849

Heilbronn
Elbatex GmbH
Cecilienstr. 24
Tel: 07131/89001.
Telex: 728362

Lehrte
Aitron
A.E. Chronicle KG
3160 Lehrte
Postfach 1280
Tel: 05132/53024
Telex: 922383

Munchen
Electronic 2000
Vertriebs-GmbH
Neumarkter Str. 75
8000 Munchen 80,
Tel: 0 89/43 40 61
Telex: 02-2561

GREECE
Elfon Ltd.
Konstantinoupoleos 18-20
Nea Smyrni Athens
Tel: (021) 93 48 912,
Telex. 214150

HOLLAND
Curijn Hasselaar
V Utenhoeveweg 100
P.O. Box 37 Geldermalsen
Tel. (0) 3455-3150
Telex: 40259

IRELAND
Neltronic Ltd.
John F Kennedy Road
Naas Road, Dublin 12
Tel: (01) 501845,
Telex: 4837

ITALY
Milano
Adelsy S.p.A.
Via Domenichino, 12
20100 Milano
Tel: 4985051-2-3-4-5
Telex: 39423

Genova
Adelsy S.p.A.
P.zza della Vittoria, 15/25
16121 Genova
Tel: 010/589674

Roma
Adelsy S.p.A
P.le Flaminio 19
00196 Roma
Tel: 06/3606580/3605769

Torino
Adelsy S.p.A
C.so Matteotti, 32/A
10121 Torino
Tel: 011/53914

Udine
Adelsy S.p.A
Via Marangoni, 45/48
33100 Udine
Tel: 0432/26996

Calderara di Reno
I.C.C. S.r.l.
Localita Lippo
Via Crocetta, 38
40012 Calderara Di Reno
Tel 051/726186

NORWAY
J.M. Fering A/S
Box 101, Bryn, Oslo 6
Tel: (02) 19.62.00
Telex: 16435

SWEDEN
Algers Elektronik AB
Box 7052
S-172-07 Sundbyberg
Tel 08-985475,
Telex: 10526

SWITZERLAND
Ellyptic AG
Postfach 174, 8036 Zurich
Tel. 33.05.89
Telex. 56835

TURKEY
EFG Inc
Buyukdere cad Hayat
Ap 28/1
Mecidiyekoy, Istanbul
Tel: 66 73 67,
Telex: 22562

UNITED KINGDOM
Keighley
Semicomps Northern Ltd
Ingrow Lane
Keighley, W. Yorks
Tel: Keighley 65191,
Telex: 517343

Kelso
Semicomps Northern Ltd.
East Bowmont Street
Kelso, Roxburghshire
Tel: Kelso 2366,
Telex: 72692

EUROPE

Kenilworth
Semicomps Ltd.
3 Warwick House, Sta. Rd.
Kenilworth, Warwickshire
Tel: 0926-59411,
Telex: 31212

Manchester
GDS (Sales) Ltd
24 Broughton St
Cheeton Hill, Manchester
Tel. 061 831 7471
Telex 668304

Portsmouth
SDS Components Ltd.
Hilsea Industrial Estate
Portsmouth,
Hants PO3 5JW
Tel: 0705 65311,
Telex: 86119

St. Albans
Semicomps Ltd.
Wellington Road
London Colney
St. Albans, Herts
Tel: Bowmans Green 24522
Telex 21108

Slough
GDS (Sales) Ltd.
380 Bath Road
Slough SL1 6JE
Tel: 06286-63611, Telex: 847571

West Drayton
Semiconductor Specialists Ltd.
Premier House, Fairfield Road
Yiewsley, West Drayton
Middlesex.
Tel. West Drayton 46415
Telex: 21958

YUGOSLAVIA
Ellyptic AG
Postfach 174, 8036 Zurich
Tel: 33.05.89, Telex: 56835

MIDDLE EAST

IRAN
A. Ardehali
138 Vozara Avenue, Tehran
Tel: 621583

ISRAEL
Alexander Schneider Ltd
44 Petach Tikva Road
Tel-Aviv
Tel. 320.89-346.07
Telex: 33613

ASIA

HONG KONG
Astec International Ltd.
Oriental Centre -- 14th Floor
67-71 Chatham Road, Kowloon
Tel: 3-694751, Telex: 780-74899

INDIA
SDM and Associates
A-3/9 Janakpuri
New Delhi -- 100 058
Tel: 393349 or 391225

KOREA
Dongyoung Trading Company
CPO Box 7336, Seoul
Tel: 794-4812, Telex: 27335

PHILIPPINES
Astec Philippines
Makati Stock Exchange Bldg
2nd Floor, Room 233
Ayala Ave., Makati Rizal 3117
Tel: 89-99-81, Telex: 07563553

SINGAPORE
Astec Singapore Pte Ltd.
1704, Golden Mile Towers
Beech Road, Singapore 7
Tel: 2-920-826,
Telex: 08723489

TAIWAN
Astec Taiwan
Room 803, 8th Floor
282 Lin Shinn Road, Taipei
Tel: 522-4800. Telex: 08523800

AUSTRALIA

New South Wales
G.E.S. (Pty) Ltd
99 Alexander Street
Crows Nest, N.S.W
Tel. 439-2488, Telex 25486

Victoria
R and D Electronics (Pty) Ltd.
23 Burwood Road
Burwood, Victoria
Tel: 288-6232, Telex. 33288

SOUTH AFRICA

Bramley
Mellonics (Pty.) Ltd
P.O. Box 39690
Bramley 2018
Tel 40-7746, Telex: 8-4852

Dunswart
Pace Electronic
Components (Pty) Ltd
P.O. Box 8054
Dunswrt 1508
Tel 52-7025, Telex. 8-7823

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TERMS OF SALE

1. INVOICE TERMS

(a) All orders are subject to the final acceptance by Seller's credit department.

(b) All shipments are F.O.B., Seller's plant, unless otherwise stated hereon.

(c) The Seller reserves the right to make shipments in part or in whole, and the Seller's invoices for such shipments shall be accepted and paid as rendered without regard to whether or not the balance of the order is shipped.

2. PRICES

(a) Prices are based upon shipments being made F.O.B. Seller's plants.

(b) Prices do not include any Municipal, State, or Federal sales, use, excise or similar taxes. Consequently, in addition to the prices specified, the amount of any present or future sales use excise or any other tax that may be imposed shall be paid by the Purchaser or in lieu thereof the Purchaser will provide the Seller with a tax exemption certificate acceptable to the taxing authorities.

(c) The price of the merchandise covered by this order is based upon the Seller's interpretation of the Purchaser's specifications.

(d) The Seller reserves the right to invoke a minimum billing charge of $100.00.

(e) Seller reserves the right to invoke a minimum cancellation charge of $50.00.

3. DELIVERY SCHEDULE

(a) Dates of shipment are approximate and are subject to the Seller's ability to conform to same, but Seller shall not incur any liability, consequential or otherwise, due to delay or failure to deliver for any reason. All orders are accepted subject to delays occasioned by labor disputes, fires, war or floods, accidents at factory or any causes whatever beyond the Seller's control. Delivery schedules are predicated upon the Seller's ability to acquire materials, tools, dies and equipment, where necessary. In the event of any such delay beyond the Seller's control, the date of delivery of this order shall be extended by a period approximately equal to the time lost by reason of the delay.

(b) If the Seller does not receive a schedule from the Purchaser promptly, the rate and schedule of shipments will be set by the Seller.

(c) Subject to change based upon delay in prompt receipt of approval of sample.

(d) Subject to change upon any modification of specifications previously agreed upon or delay in submission of specifications acceptable to Seller.

(e) Seller reserves the right to overship or undership a quantity totalling 5% of the last scheduled release of any order for non-standard parts.

4. SHIPMENT

(a) Unless specified the Seller will select the mode of transportation and the Seller will not be responsible for differences in cost between one mode and another.

(b) The Seller is not responsible for damage or loss in transit and any such claims are to be placed by the Purchaser with the carrier, where shipment is made F.O.B. Seller's plant.

5. INSPECTION AND ACCEPTANCE

(a) It is understood that the conditions of the Purchaser's inspection or test of the material covered by this order shall be mutually agreed upon and the Seller reserves the right to inspect any material which the Purchaser claims to be defective on the Purchaser's premises and decide whether or not it should be replaced. Any required repairs which the Seller's inspection determines to be the Purchaser's responsibility will be made at the Purchaser's expense and at the Seller's option on the Purchaser's premises.

(b) If the material covered by this order is proven defective and the Seller was notified of such defects in writing within twenty days from the date of shipment, the Seller will be responsible only for the costs of repair or replacement of the Seller's product, and in no event will Seller be liable for any damage consequential or otherwise or for an amount in excess of the price (at the time of adjustment) of the defective item(s). The Seller will not be responsible for any charges resulting from the use of defective material.

(c) No material may be returned for credit and no material may be returned to the Seller for correction without the Seller's prior written approval, but if such unauthorized return shipments are made to the Seller, the Seller reserves the right to refuse the shipment or to accept it, and in the latter case, the shipment will be held as the Purchaser's property and without responsibility to the Seller.

(d) All claims, including claims for shortages must be made within five (5) days after receipt of shipment except as otherwise contained in this Terms of Sale.

6. TOOLS

Payment of the Seller's charges for tools, dies, jigs, fixtures, etc. and/or equipment required for the production of this or other orders does not convey ownership of such items to the Purchaser nor the right to remove them from the Seller's plant, as such charges do not represent prices that would be charged for the sale of such items and oftentimes represent the costs of modifications and/or additions to standard tools or equipment.

7. CANCELLATION

Cancellation of this order for any reason whatsoever will be accepted only upon terms that will fully indemnify the Seller.

8. REMEDIES OF THE SELLER

(a) If, at the Purchaser's request or for any other reason for which the Purchaser is responsible, production or shipment of this order is held or delayed, the Seller reserves the right to immediately invoice the Purchaser for same in accordance with the provisions of Clause 7 above and payment is to be made promptly in accordance with this Terms of Sale. Should the Purchaser release the hold or remove the cause for delay and the Seller agrees to reinstate the order, the schedule of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(b) If, in the Seller's judgment, the Purchaser's financial condition at any time does not justify continuance of production or shipment of the material covered by this or any other of the Purchaser's orders, the Seller reserves the right to require full or partial payment in advance and/or to withhold further shipments and stop production, in which case the conditions of Cancellation Clause 7 above will apply.

(c) If payment of the Seller's invoice(s) for shipments in part or in whole is not made promptly and in compliance with this Terms of Sale above, the Seller reserves the right to withhold further shipments and/or stop production and at the Seller's option, to require full payment in accordance with Clause 7 of this Terms of Sale. If, as a result of the purchaser's failure to pay the Seller's invoice(s) promptly, the Seller stops production of this order and later agrees to reinstate it, the scheduled rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(d) If at any time prior to the date of initial production and/or shipment of the order or at any subsequent time during the course of this order, there shall be filed by or against the Purchaser in any Court, pursuant to any statute either of the United States or of any State or Municipality a petition of bankruptcy or insolvency, or for reorganization, or for the appointment of a receiver or trustee of all or a portion of the Purchaser's property, or if the Purchaser makes an assignment for the benefit of creditors, this order shall ipso facto be cancelled and terminated and, in which event, neither the Purchaser nor any person claiming through or under the Purchaser or by virtue of any statute or an order of any Court shall be entitled to any rights of the Purchaser's order and the Seller reserves the right to impose all applicable conditions of this Terms of Sale, including Cancellation Clause 7 above, as well as to retain as partial liquidated damages any payments, security, deposits or monies received by the Seller from the Purchaser or others in the Purchaser's behalf against this order. Should the receiver, trustee, the operating committee, or other similar agency desire to reinstate this order or any uncompleted portion thereof, the Seller reserves the right to either refuse or accept such requests for reinstatement and, in the latter case, to determine what appropriate credits, if any, are to be issued to offset charges previously made as herein above in this clause provided for. If the Seller elects to reinstate the order it is subject to this Terms of Sale and the schedule and rate of delivery will be set by the Seller in accordance with the requirements of the Seller's then existing factory schedule.

(e) If the Seller accepts notes, trade acceptances or other paper as part or entire payment for this order, all shall become due at the Seller's option, upon default in the payment of any one of them, and the Seller reserves the right to impose the conditions of Cancellation Clause 7 above.

9. The terms and conditions of this order acknowledgment supersede the Purchaser's order, and no variation of this agreement shall be valid unless same be in writing signed by a duly authorized officer of the Seller.

10. General Instrument Corporation, warrants its devices against defects in material and workmanship for a period of ninety (90) days in the case of entertainment type devices, or one (1) year in case of all other devices, from the date of shipment provided they are used within their voltage and current limits and under conditions specified by General Instrument Corporation. Adjustments if any are subject to clauses 5(b), (c), and (d) of the Seller's Standard Terms of Sale, and devices returned to factory for adjustment must be shipped with all transportation charges prepaid.

GENERAL INSTRUMENT CORPORATION
MICROELECTRONICS