NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD

C5 (DIS #2) 47Ω

T5 (DIS #4) 64K VLC INVIO NTSC

E5 LS257 A0-A3 → RA0-RA3

D5 LS257 A4-A15 → RA4-RA7

E3 LS00 P∅ 9 10 Q3+PRAS

F3 LS00 C8-FXXX 9 10 C8-7XXX → CXXX 6

F4 LS156 A11 A12 A13 → FXXX EXXX DXXX C8-FXX C0-7XX

F3 LS00 A14 A15 → F4

D4 LS08 FXXX EXXX → E-FXX

F3 LS00 E-FXX DXXX → D-FXXX

M3 LS08 A14 9 64K 10 → M4 LS32 A14/A8 11

M3 LS08 A8 12 16K 13 → M4

D3 LS04 13 12 MC3XX

J4 LS138 A8 A9 A10 A11 → MC∅XX

J5 LS138 A4 A5 A6 A7 S5 6 → MC∅XX MC∅8X MC∅9X MC∅AX MC∅BX MC∅CX MC∅DX MC∅EX MC∅FX

P3 LS138 A4 A5 A6 Φ1 A7 → DEV∅ DEV1 DEV2 DEV5 DEV6 7

T7 TC 12 13 PΦ1 → S5 9 8 10

S5 6 5 4 POC

A3 (DIS #2) 2.2M .1µ 3.3K 1K 3.3K 2N3904 2N3904 +5 VTR 64K → IRQ RESET IRQ

P4 MC∅XX 9 10 A7 Φ1 → P4 12 13 11

M3 LS08 DEV5 DEV6 → R3 DEV1 DEV2 → PSELIO

RDROM D-FXXX R/W → D2 LS10 6

WRPROT D-FXXX R/W → B5 LS10 8

C3 LS04 R/W 9 8 → C3 10 11

D2 6 F3 LS00 3 C4 LS32 6 ← CXXX 5

B5 8 P7 LS00 8 ← CXXXOUT 9 10 11

INTIO 13 C3 LS04 12 → P7

P9 LS00 11 ← R/W 13 12

C4 LS32 11 ← DMA 12 13

C3 LS04 1 2

L4 LS08 3 ← 1 2

L4 LS08 6 ← 4 5

MC∅∅X 15 12 13 J3 LS08 11 INTIO → MC∅1X

N4 LS32 3 ← R/W 1 2

N4 LS32 6 ← Φ1 4 5

+5 25

E6 MMU

A0 2		6	ORA0
A1 40		7	ORA1
A2 39		8	ORA2
A3 38		9	ORA3
A4 37		10	ORA4
A5 36		11	ORA5
A6 35		12	ORA6
A7 34		13	ORA7
A8 33		18	KBD
A9 32		22	R/W245/C07X
A10 31		23	CASEN
A11 30		20	ROMEN1
A12 29		19	ROMEN2
A13 28		16	DMA/C06X
A14 27		15	INH/SC0
A15 26		5	PRAS
R/W 14		4	Q3
CXXX/SELIO 24		3	Φ∅
		17	EN80
		21	MD7

PU27

VLC R6 LS125 ← CXXXOUT

PSELIO R6 LS125 ← VLC

R8 LS04 5 6 → R/W

VLC R8 LS04 1 2 → VLC

R/W245 P6 LS125 ← 2 3

MC07X Φ1 P5 LS32 1 2 3

P6 LS125 4 5 6

MC06X Φ1 P5 LS32 4 5 6

P6 LS125 10 9 8

P5 LS32 9 10 8 → DMA

PCASEN

OCASEN

SELMB 4 5 E2 LS32 6 ← PCASEN

INH 1 2 E2 LS32 3 → OCASEN

H3 LS10 Φ∅ 8 9 10 L4 LS08 8 → R/W245

INH H3 LS10 12 13 11 → PRW245

DMA 12 R/W 13 E2 LS32 11

K4 LS04 INH 3 4

A0 A1 H4 LS86 3

D3 LS04 1 2 5 12

A0 R/W D4 LS08 4 5 6

D4 LS08 9 10 8

FST ACC WREN A0 → C4 LS32 9 10 8

E3 LS00 12 13 11

PWR PROT 13

E4 LS175 A3 (C08) → Q BANK1 (C089-F) Q̄ BANK2 (C089-7) Q RD RAM (C088-B) Q̄ RD ROM (C088-3) Q̄ FST ACC (C08E, C08F) Q WRPROT (C08D) Q̄ WREN (C08D) 9 1 → MPON DEV∅

+5 VTR → B3 S55 4 8 2 6 3

C3 LS04 11 10 → POC

POC

A4 (DIS #1) 3.3K SIP 3.3K SIP

+5 1		16	+5
ENIO 2		15	S5
PU27 3		14	NTSC
RESET 4		13	FXXX
INVIO 5		12	EXXX
VLC 6		11	DXXX
PRW245 7		10	C8-FXX
8		9	C0-7XX

OCASEN Φ∅ 64K → L5 LS32 1 2 3 → L2 LS08 9 10 8 CASEN

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ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
MATERIAL: N/A
NEXT ASSY. FINISH: N/A

DRAWN BY Dave North DATE 1/83
CHECKED BY Dave North DATE 2/83
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE SCHEMATIC, CUSTOM EMULATOR LOGIC-MMU
SIZE D DRAWING NUMBER SK3519-00
SCALE: NONE SHEET 1 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER SK3519-00 SH 1 OF 2

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